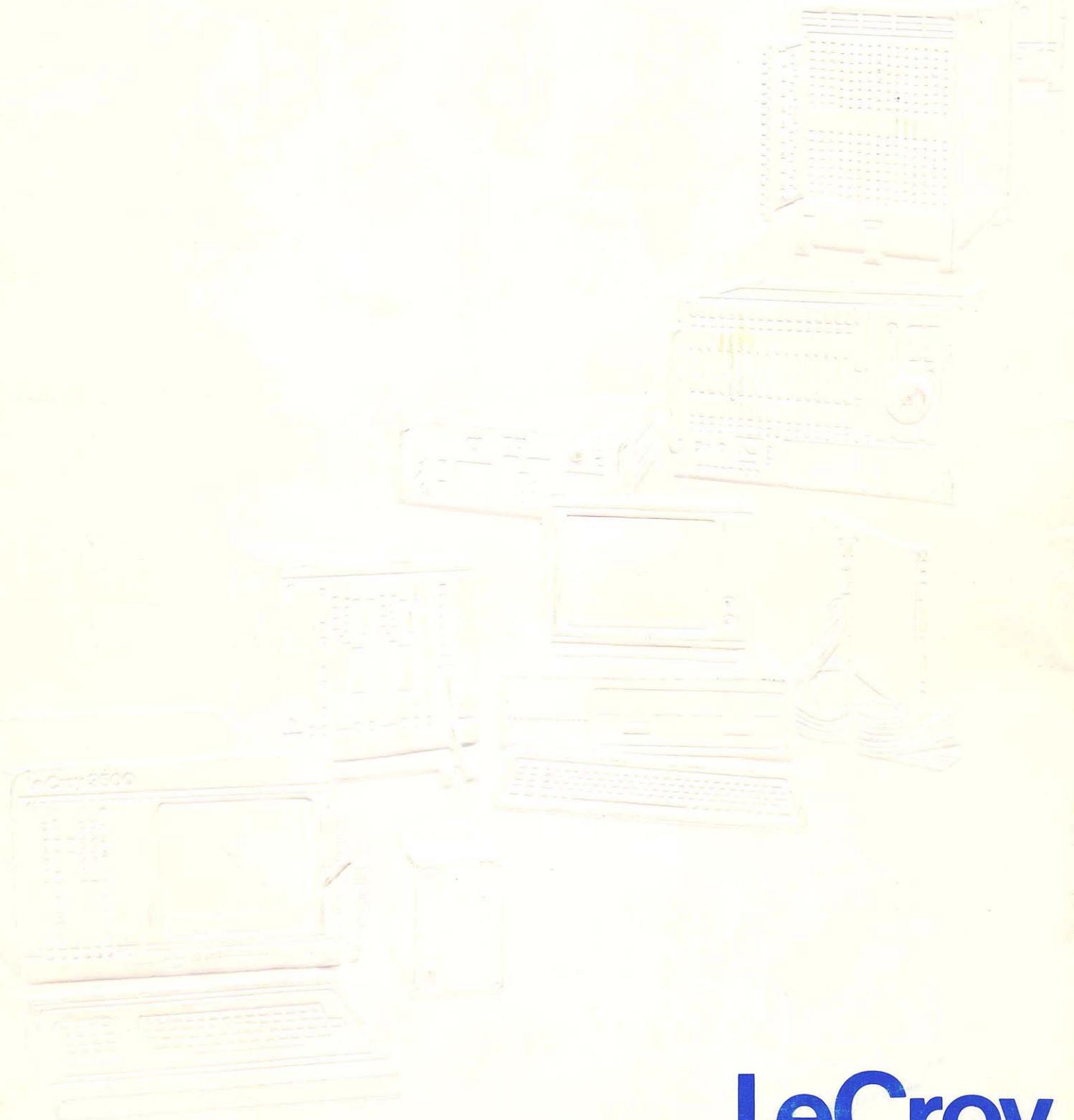
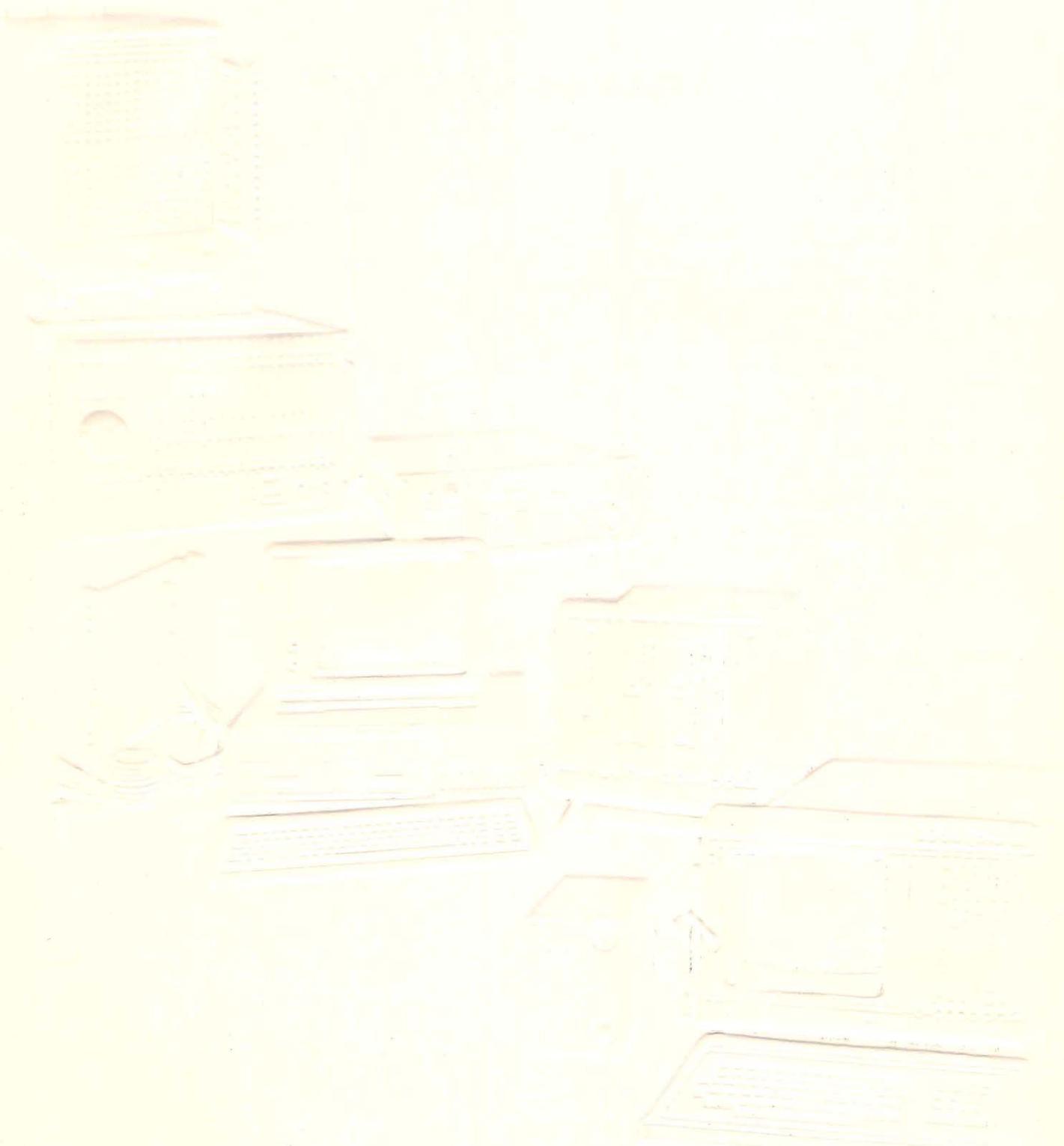


1985 Catalog



LeCroy

Innovators in High-Speed Instrumentation



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LeCroy Facilities

LeCroy — In Brief

Founded on the need by the High Energy Physics Research community for reliable state-of-the-art electronics to instrument its experimental activities, LeCroy has been closely attuned to these specific requirements since 1964. Expertise developed over the years for this marketplace has yielded advanced technological capabilities in the areas of small pulse measurement, high rate pulse counting, fast sampling transient recording, and high voltage power supplies. Diversification has expanded LeCroy's experience to microprocessor-based data acquisition instruments, multi-channel analyzers, fiberoptic systems, and digital oscilloscopes.

Innovators in Instrumentation

LeCroy maintains a strong devotion to the concept of INNOVATION. Its major market areas strongly manifest that direction, all prime research areas in the forefront of technology. These include High Energy Physics, Fusion, Synchrotron Radiation, Nuclear Physics, X-Ray Materials Analysis, Electric Power Generation and Fiberoptics. The emphasis of several working groups within the LeCroy organization is dedicated to applying LeCroy innovation to industrial applications. In addition to market expansion, LeCroy has also observed its mandate of INNOVATION in design and production technology, depending heavily upon hybrid circuit and monolithic development capabilities.

The LeCroy Organization

The LeCroy Organization currently consists of Corporate Headquarters, Product Divisions dedicated to specific market areas, and several sales and service subsidiaries. Design and manufacturing are centered in Spring Valley, New York (Adtec and HEP Divisions), and Geneva, Switzerland (European Products Division). Direct sales and service centers are located in Paris, France; Heidelberg, West Germany; Oxford, England; Albuquerque, New Mexico; Livermore, California; Oak Park, Illinois (Chicago area); Annapolis, Maryland;

Princeton, New Jersey; and Manchester, NH (Boston area) in addition to the main facilities.

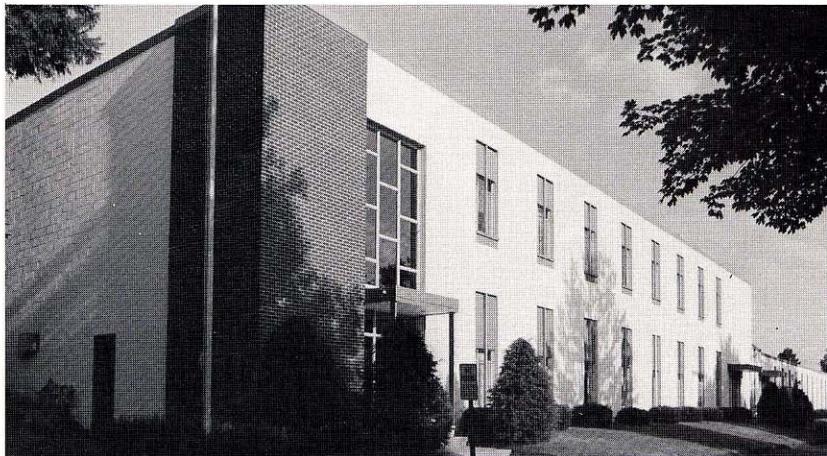
The primary market areas served by the LeCroy Product Divisions follow:

New York Location/ Corporate Headquarters

High Energy Physics, Spectroscopy, Fusion and Weapons Research, Signal Averaging, Transient Recording, Electric Power Generation, Nuclear Physics, Fiberoptics.

Geneva Location

High Energy Physics, Synchrotron Radiation, X-Ray Materials Analysis, Digital Oscilloscopes.



SPRING VALLEY, NEW YORK



GENEVA, SWITZERLAND

Quality Assurance

The key to LeCroy quality and reliability is the company's comprehensive Quality Assurance Program. QAP begins with original component selection for a new circuit design. Research & Development, Engineering, and Production work in close coordination investigating and evaluating latest state-of-the-art advances in hybrid circuits, IC's, and discrete components. In this regard, LeCroy is its own toughest competitor. Circuits are constantly updated to incorporate latest component advances in order to improve instrument speed, performance, and reliability.

Before any active component qualifies for assembly onto a LeCroy printed circuit board, it must pass not only a close initial visual inspection, but rigid electrical, environmental, and accelerated life tests as well. Typical of this type of component quality assurance check is the company's exhaustive transistor screening procedure patterned after the stringent requirements of NASA's semiconductor reliability program. This program weeds out infant failures by stressing all transistors — *i.e.*, by active "burn-in" of all devices at elevated temperature for a controlled period of time. The devices are then screened by two automatic transistor test systems designed and built at LeCroy,

first for d-c parameter limits, and then for bond continuity under thermal cycling. These procedures, whose development and implementation represented a major effort on the part of LeCroy engineering and production groups, are primarily responsible for the low incidence of product failures on established products.

As the instrument moves through the various states of assembly, it is given thorough inspection of solder joints, lead dress, and other details to assure quality of workmanship meeting highest scientific instrument standards.

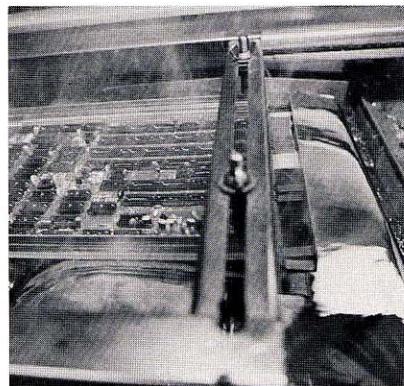
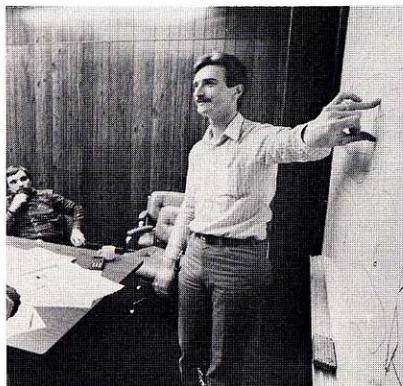
The assembled and inspected instrument receives its initial calibration and operational check in the Test and Calibration Department. The unit is then "burned in" under power in precisely controlled environmental testing chambers for 72 hours, cycling between ambient temperature and 70°C to accelerate any electrical component failures. This temperature cycling subjects all components to mechanical stress to eliminate any borderline components which might conceivably result in field failure. Finally, after the components have "settled in," the instrument is recalibrated and system-tested under full operational conditions. For most new LeCroy products, this rigorous final test and calibration is done under full computer assistance. All

LeCroy Product Divisions are equipped with computer test stations, the most recent based upon LeCroy's System 3500 CAMAC-based data acquisition system. Most LeCroy service facilities are similarly equipped. Standard software, distributed to all test and service locations, insures that the LeCroy products represented cannot fall subject to human limitations, yielding an uncompromised product for delivery or return to the field.

As an example, each LeCroy ADC and TDC is exercised over its entire dynamic range and the information is used to generate calibration results indicating slope, intercept (pedestal), and non-linearity. These results are carefully analyzed by the Test personnel to assure strict adherence to the performance standards required of LeCroy instruments.

A further level of scrutiny is added at LeCroy distribution facilities in areas outside the USA, where newly-released items are again reviewed by a computer-assisted Customer Simulation Group before final delivery to the customer.

The authenticated Tested, Calibrated, and Customer Serviced sticker attached to a completed instrument certifies that it has met the demanding requirements of LeCroy/QAP and should provide long and dependable operation in the field.



Advanced Hybrid Circuit and Custom Monolithic Design

The use of special-purpose hybrid circuits represents a major step forward in the reliability, compactness, and performance of LeCroy modular products. Built in the Spring Valley facility, the hybrid circuits are miniaturized counterparts of conventional printed circuit cards.

Hybrid circuits offer enhanced product reliability by minimizing the number of discrete components and solder connections, permitting simpler layouts and, as a result of their small size, allowing better ventilation. In addition, hybrid circuits undergo extra stages of quality assurance before insertion into LeCroy products. Serviceability is enhanced because the hybrids are mounted in sockets and can easily be replaced for diagnostic or repair purposes.

Hybrid circuits contribute to improved circuit performance by their effect upon circuit size, stray capacitance and inductance. By minimizing these parameters, hybrid circuits improve bandwidth, reduce cross talk, and lower propagation delays in comparison with their printed circuit equivalents.

LeCroy's in-house Monolithic Design Group enables the

company to increase the packing density of its modules and systems and reduce their cost to customers. The group has facilities for design, computer circuit simulation, layout, computer-design rule checking and pattern generation of the integrated circuit. An ultrafast bipolar process available to LeCroy allows circuits to be designed with propagation delays as short as 75 psec, thereby enhancing the performance of LeCroy products. The end result of the design process is a magnetic tape that can be used by a selected silicon foundry to produce the desired wafers.

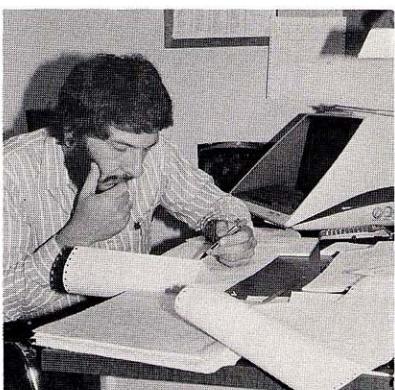
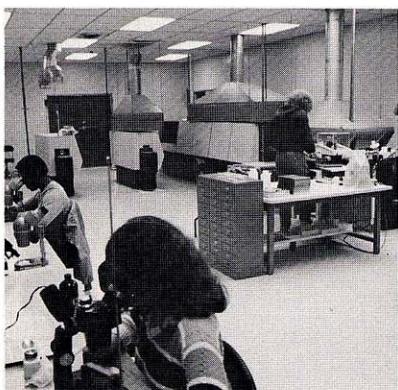
The Monolithic Design Group is aided by two extremely useful tools for IC development. In addition to the Applicon graphic system, a VAX-based circuit simulation program called SPICE (Simulation Program for Integrated Circuit Engineering) is extensively used. A circuit simulation program is essential. Unlike a discrete or IC version of a circuit, which can be breadboarded to study its performance, a monolithic device breadboard displays extraneous results due to stray capacitances that would not be present in the chip. Moreover, since any circuit simulation program is only as accurate as the models for the circuit devices, LeCroy has developed superb models for the fast IC process. As a result, the prob-

able need for an iteration of a new Integrated Circuit is diminished, along with the consequent doubling of the development time.

Maintenance, Modification, and Repair Services

Each LeCroy instrument is accompanied by a Warranty Card which, when returned to the factory, registers the instrument in the name of the user. Modification kits for updating the performance of older instruments, revised Technical Information Manuals and other information pertaining to a specific instrument are periodically made available through this registry service.

Assistance in maintaining your LeCroy equipment is available from both field and factory personnel. Where local facilities do not exist, your instrument should be returned to the appropriate LeCroy Product Division for proper repair and recalibration. It is suggested that you address the shipment to the LeCroy Repair and Recalibration Department and include a complete description of the problem or service you wish performed. This is extremely important in minimizing repair time and charges. If the unit is out of warranty, the Repair Department will advise you of estimated charges before pro-



ceeding if major work appears to be required. In many cases, such as with large rack-mount or tabletop instruments, repair is accomplished quickly by local facilities through board replacement. Charges for such repairs are a minimal ten percent of the board value, if the unit is out of warranty.

Under normal circumstances, two weeks should be allowed for completion (at the factory) of the work. In emergency situations, LeCroy will attempt more rapid service, or, if possible, provide temporary replacements for instruments requiring maintenance. Your local field engineer can assist you in making such an arrangement, should it be required. Please call for a Return Authorization Number (RAN) before sending anything back to the factory.

Location of Major Service Facilities

In addition to factory repair at a Product Division, the following corporate-wide service facilities are available for your convenience:

France — Les Ulis:

LeCroy Research Systems
SARL
Avenue Du Parana
Z.A. DeCourtaboeuf
F-91940 Les Ulis, France



Germany — Hamburg:
LeCroy Research Systems
GMBH
Alte Volksparkstrasse 24,
D-2000 Hamburg 52,
West Germany

Germany — Heidelberg:
LeCroy Research Systems
GMBH
Werderstrasse 48
D 6900 Heidelberg,
West Germany

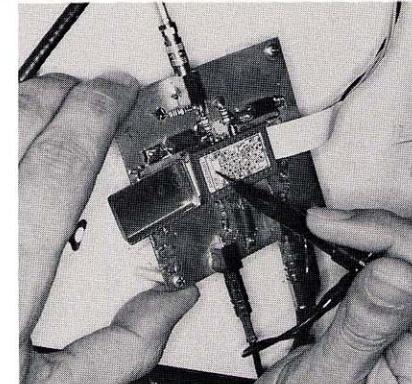
United Kingdom — Oxford
LeCroy Research Systems Ltd.
Elms Court
Botley, Oxford OX2 9LP
England

United States — California
LeCroy Research Systems Corp.
1816/1824 Holmes St. - Bldg. E
Livermore, California 94550

United States — New Mexico
LeCroy Research Systems Corp.
14800 Central Ave. S.E.
Albuquerque, New Mexico
87123

LeCroy Sales Offices And Representatives

See United States and International Sales Representatives Map.



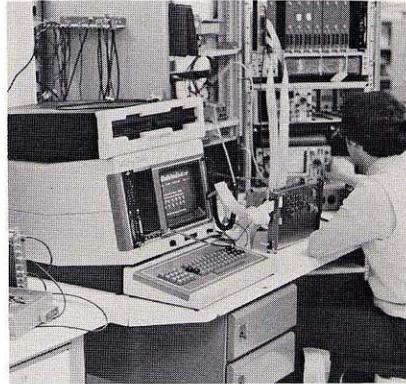
Other Information Available from LeCroy

In addition to this catalog, LeCroy offers additional literature for your information. A condensed version of the catalog along with special product brochures, technical data sheets, and application notes are available on request from your local sales representative or via regular mailings.

To be included on the mailing list, simply fill out the appropriate postcard in the back of this catalog and put it in the mail. Be sure to identify your discipline (physicist, engineer, etc.) and application interests (Spectroscopy, High Energy Physics, Nuclear Physics, etc.).

Newsletters

Two newsletters are issued periodically to keep you informed of the latest news and product developments. FAST-PULSE INSTRUMENTATION NEWS covers the high energy and nuclear physics fields. TRANSIENT NEWS is a publication dedicated to waveform recording. Simply drop us a line for the latest copy and you'll be added to the mailing list.



Ordering Information

How To Order

When placing an order, please specify the Model Number as well as the name of the instrument. Many Model Numbers include letter designations such as the TR8837F or the 1885N. Some Models are offered with several options designated by a slash followed by a number such as 4300/210. Special care should be taken to include these alphanumeric designations on your order.

All purchase orders are subject to a \$100.00 minimum.

If LeCroy has agreed to supply an instrument which has been modified to satisfy your specific requirement, please be certain that the performance specifications of this modification are specified on your order.

When the exact Model Number, including the alphanumeric designation, does not appear on the Price List it is advisable to consult your local sales office or the Product Division Headquarters in either Geneva, Switzerland or Spring Valley, New York before placing your order.

Where To Order

Purchase Orders may be forwarded to your local sales office or to the Product Division Headquarters in Geneva, Switzerland or in Spring Valley,

New York. A list of the Sales offices is given on pages 8 and 9.

Acknowledgment

When a purchase order is accepted by LeCroy Research Systems Corporation, an acknowledgment is issued immediately confirming the equipment type, quantity, and price and indicating an estimated delivery date. Please read this acknowledgment carefully. Any discrepancy between the purchase order and the acknowledgment should be reported immediately to the local sales office or to the Product Division Headquarters in Geneva, Switzerland or in Spring Valley, New York.

Shipping

The standard FOB point for all orders placed in the United States is Spring Valley, New York. The standard shipping method for most products is via two-day parcel service. Some products require either Air Freight or Motor Freight.

Special shipping instructions should be arranged before placing a purchase order so that any additional shipping charges are properly taken into account.

Terms

Payment Terms are "Net 30 Days, acceptance period included" for all orders

originating within the United States. The 30-day period begins on the actual shipping date. Any exception to these payment terms should be requested before placing a purchase order.

Warranty

Equipment manufactured and sold by LeCroy Research Systems Corporation is generally covered by a 1-year warranty. A full statement of the warranty policy is contained in the product manual. Components (hybrids and monolithics) are warranted for 90 days.

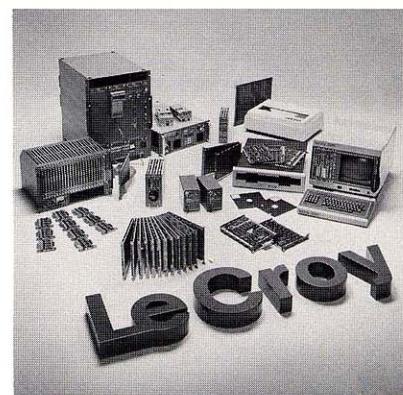
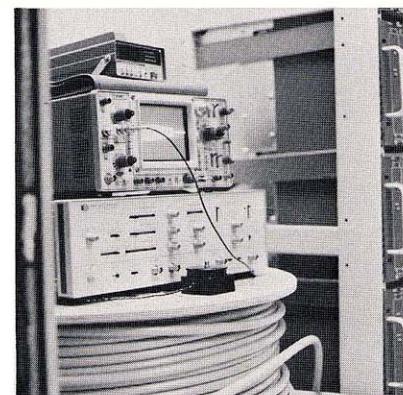
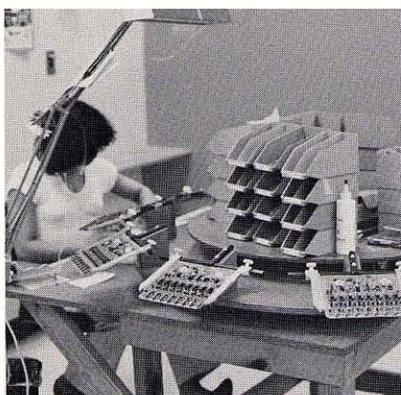
Returns

Any goods returned to the Product Division Headquarters in Spring Valley, New York must be accompanied by a Return Authorization Number. This number may be obtained from the Engineering Services Department in Spring Valley, New York.

Any returned goods should be shipped in the original packing material.

Returned goods that have not been packed in the original packing material and have been damaged in shipping will not be repaired under warranty.

Any goods returned for credit are subject to a 20% restocking charge.



SALES OFFICES

United States and Canada

N. CA, OR, WA, ID, UT, N. NV, GenAtom, TRIUMF

LeCroy Research Systems Corporation
1816 Holmes Street-Bldg. E
Livermore, California 94550
Phone: (415) 449-8226

S. CA

Beckrep, Inc.
5838 Irving Avenue
LaCrescenta, California 91214
Phone: (213) 957-1111

AZ, S. NV, NM, CO,

El Paso County, TX

LeCroy Research Systems Corporation
14800 Central Avenue S.E.
Albuquerque, New Mexico 87123
Phone: (505) 293-8100

TX (Ex El Paso Co.), OK, RS, AR, LA

LeCroy Research Systems Corporation
Phone: (505) 293-8100

NC, SC, FL, GA, AL, MS, TN, Ex. ORNL

LeCroy Research Systems Corporation
410 Ware Blvd., Suite 705
Tampa, Florida 33619
Phone: (813) 626-1818

DC, MD, DE, VA, W. VA, and ORNL

LeCroy Research Systems Corporation
4660 Kenmore Avenue, Suite 1018
Alexandria, Virginia 22304
Phone: (703) 751-4148

Metro NYC, NJ, E. PA

LeCroy Research Systems Corporation
178 Pennington-Harbourton Road
Pennington, New Jersey 08534
Phone: (609) 737-1162

Up NY, VT, NH, MA, ME, RI, CT

LeCroy Research Systems Corporation
176 Walnut Street
Manchester, New Hampshire 03104
Phone: (603) 627-6303

IL, WI, MN, IA, MO, ND, SD, (Ex. FermiLab)

LeCroy Research Systems Corporation
9401 West Beloit Road #304
Milwaukee, Wisconsin 53227
Phone: (414) 545-6505

KY, IN, OH, MI, W. PA

LeCroy Research Systems Corporation
410 Fairway Drive
Springboro, Ohio 45066
Phone: (513) 748-2696

Midwest (FermiLab Related)

Corlett and Associates
110 West Madison
Oak Park, Illinois 60302
Phone: (312) 386-3628

Quebec, Maritime Provinces

Radionics Scientific Inc.
9490 Trans Canada Highway
St. Laurent, Quebec H4S 1R7
Canada
Phone: (514) 335-0105

Western Ontario

Radionics Scientific Inc.
585 Canarctic Drive
Downsview, Ontario M3J 2P9
Phone: (416) 736-1600

East Ontario and Manitoba

Radionics Scientific Inc.
2487 Kalader Avenue
Suite 205/206
Ottawa, Ontario K1V 8B9
Phone: (613) 521-8251

Saskatch, Alberta, BC (Ex. TRIUMF)

Radionics Scientific Inc.
4506 Dawson Street
Burnaby, BC V5C 4C1
Phone: (604) 293-1854

**NOTE: If unable to reach a Local Sales Representative, please call
the numbers listed below.**

LeCroy Research Systems Corporation
700 South Main Street
Spring Valley, N.Y. 10977, USA
(914) 425-2000

LeCroy Research Systems SA
Route du Nant-d'Avril 101
1217 Meyrin 1-Geneva, Switzerland
(022) 82 33 55

International Representatives

ARGENTINA

Search SA
Corrientes 617, tº piso
1043 Buenos Aires
Argentina

AUSTRALIA

ETP-Oxford Pty. Ltd.
P.O. Box 105
Ermington, N.S.W. 2115
Australia
Phone: 61-2-858-5122

BRAZIL

Antonio A. Santos
Rua Da Quitanda
194-Sala 404
ZC 05, Rio De Janeiro
Brazil
Phone: 55-21-233-5590

DENMARK, NETHERLANDS, BELGIUM

Datalog 82
Acacialaan 9
5581 HB Waalre
The Netherlands
Phone: 31-4904-5856

ENGLAND

LeCroy Research Systems Ltd.
Elms Court
Botley, Oxford OX2 9LP
England
Phone: 44-865-727275

FINLAND

Labtronic Oy
Sarkatie 2
P.O. Box 34
01661 Vantaa 66
Finland
Phone: 358 0847 144

FRANCE

LeCroy Research Systems Sarl
Avenue Du Parana
Z.A. De Courtabœuf
F-91940 Les Ulis, France
Phone: 33-6-907-3897

GREECE

Hellenic Scientific
Representations Ltd.
11 Vrassida Street
Athens 612, Greece
Phone: 30-1-721-1140

INDIA

Electronic Enterprises
Post Bag No. 6367, Unit 216
Regal Industrial Estate
Acharya Donde Marg, Sewri
Bombay-400 015, India
Phone: 882-7096

ISRAEL

Ammo
60 Pinkas Street
P.O. Box 21362
Tel Aviv 61213
Israel
Phone: 972-3-453157

ITALY

Giovanni Burgada
Via Roccaporena 58
00191 Roma, Italy
Phone: 39-6-320-0646

JAPAN

Toyo Corporation
Daito Bldg. 2, 1-Chome
Hongoku-Cho, Nihonbashi
Chuo-ku, Tokyo T103
Japan
Phone: 81-3-279-0771

KOREA

Samduk Science and Ind. Co., Ltd.
28-36 Inyie-Dong, Jongro-Ku
Seoul, Korea
K.P.O Box 1253
Phone: (02) 763-7447

MEXICO

Nucleoelectronica, SA
Calz. Las Aguilas 101-2
Col. Las Aguilas
Delegacion Alvaro Obregon 01710
Mexico 20, D. F.
Phone: (905) 593-6043

NORWAY

Laborel AS
Ole Deviks Vei 38
Box 109 Alnabru
Oslo 6, Norway
Phone: 47-2-647130

PAKISTAN

Electronuclear Corporation
1st Floor, 16 Kazi Chambers
Bahadurshah Zafar Road
Karachi-5
Pakistan
Phone: 92-21-418087

SOUTH AFRICA

Willistin Elin
P.O. Box 39491
Bramley 2018
South Africa
Telex: 4-24206 SA

SPAIN

Anadig Ingenieros, SA
Amado Nervo 3
Madrid 7, Spain
Phone: 34-1-4332412

SWEDEN

Alnor Instruments AB
S-61182 Nykoping
Sweden
Phone: 46-155-68050

SWITZERLAND

LeCroy Research Systems SA
Route du Nant-d'Avril 101
P.O. Box 341
1217 Meyrin 1-Geneva
Switzerland
Phone: 41-22-82-3355

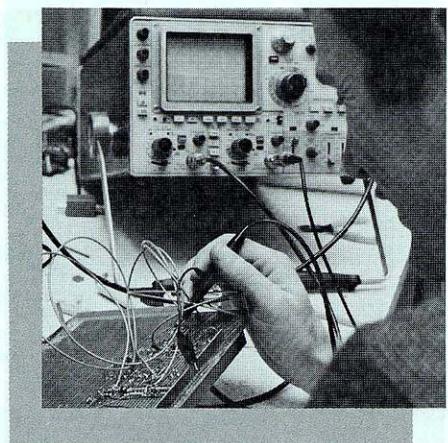
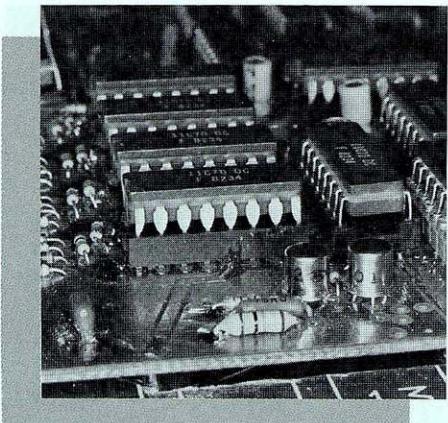
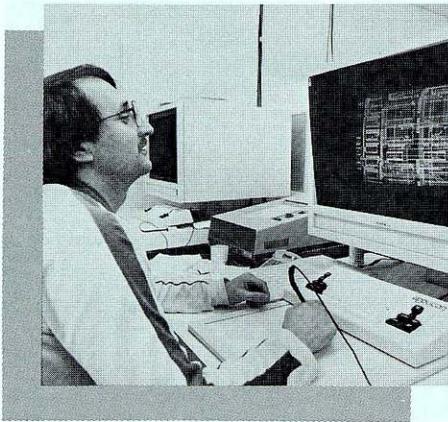
WEST GERMANY

LeCroy Research Systems GmbH
Postfach 10 37 67
Werderstrasse 48
6900 Heidelberg
West Germany
Phone: 49-6-221 49162

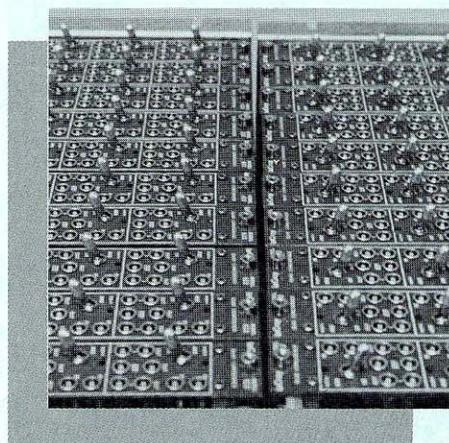
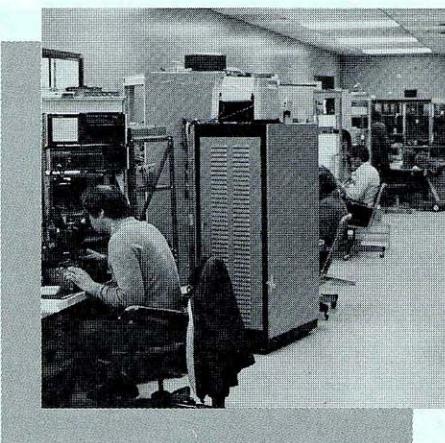
TAIWAN

Allied Winners Corporation
P.O. Box 7-825
11-F, 169 Hoping E.Rd., Sec. 1
Taipei, Taiwan 106
Republic of China
Phone: 886-2-3416026 or
886-2-3412708

Fast Pulse Instrumentation Concepts



Amplifiers
Fan-Ins and Fan-Outs
Discriminators
Coincidence or Logic Units
Registers
Trigger Logic in ECL
ECLLine Configurations
Sample Applications
Third Level Triggers-Trigger Processors
Time Interval Measurement
Data Transmission Sources & Sinks
Time Interval Measurement
Scalers
Latching Scalers
Preset Scalers
Analog Measuring Instruments
Image Chamber Analyzers
Quasidifferential Inputs
Dynamic Range
High Voltage
Wire Chamber Electronics
Proportional Chamber Circuits
Drift Chambers
Readout Electronics
Time Projection Chamber Readout
X-Ray and Neutron Physics
Position-Sensitive Detectors
Fiberoptic Systems



Amplifiers

Wideband pulse amplifiers are used to provide gain for the fast transient signals provided by photomultiplier tubes and other high speed detectors. Historically, experimenters relied upon costly photomultipliers which could provide gains as high as 10^7 . Modern amplifiers, providing excellent economy and pulse fidelity, can now be used in conjunction with lower gain photomultipliers. This configuration offers a number of advantages. Operated at lower gain, photomultipliers require lower voltage and lower bias currents. They also offer better linearity, especially at high counting rates. Use of lower gain photomultipliers with amplifiers provides an overall advantage in price and, owing to the small size of modern hybrid circuit amplifiers, allows simpler mounting schemes.

The amplifiers are non-inverting and contain no shaping circuits so that the output retains the shape of time information of the input signal. Bipolar amplifiers offer linear performance for pulses of both polarities.

The complexity and power dissipation of practical bipolar circuits is greater than that of negative- or positive-only amplifiers. For photomultiplier anode signals which are always negative, LeCroy offers the VV100BTB single channel hybrid amplifier card, the VV100B hybrid circuit, and the 612A NIM multichannel amplifier, all of which produce negative outputs only.

For applications involving a large duty cycle, amplifiers must have direct coupled inputs and outputs. This eliminates the possibility of baseline (zero level) shifts. Special compensation circuitry must be employed to minimize drifting of the output DC level with temperature. Although LeCroy's direct-coupled ampli-

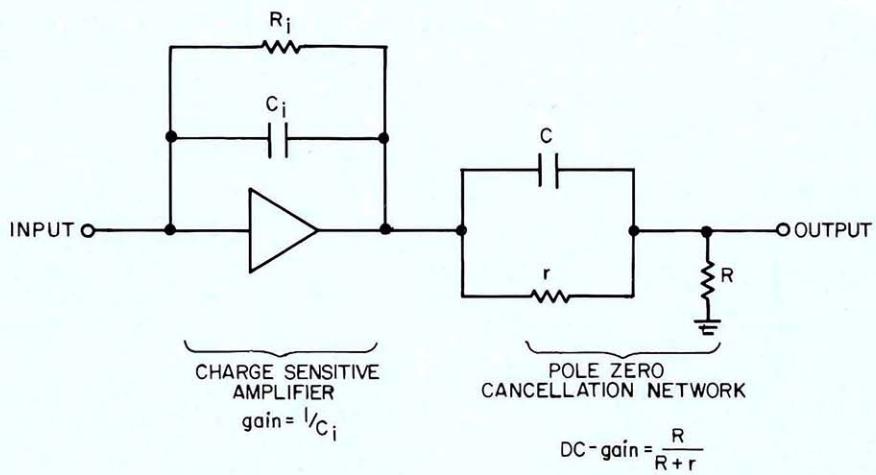


Figure 1

fiers are particularly stable with temperature, AC coupling should be used whenever the operating conditions permit.

Input protection to fairly high voltage levels (± 100 V) is necessary to protect the circuit from damage caused by spurious overloads characteristic of many detectors. The input signal may be from either a voltage or current source. An example of a voltage source is a signal which has propagated down a long transmission line, like a coaxial cable. In this case, a voltage amplifier is used. Typically, the circuit has an input impedance set to terminate the coaxial input cable. The gain of a voltage amplifier is a dimensionless quantity (voltage out/voltage in). A gain of only 10 is common to preserve the fast risetime of input signals. To achieve higher gain, multiple channels can be cascaded with corresponding loss of bandwidth.

Transimpedance amplifiers are often used when the signal comes from a current source, such as a PMT anode. These amplifiers have a low input impedance (typically less than $1\text{ k}\Omega$), and produce an output voltage proportional to the input current. In this current-to-voltage mode, the transfer gain of the device has units of resistance ($\text{mV}/\mu\text{A} = \text{k}\Omega$).

Charge sensitive amplifiers are similar to transimpedance amplifiers except that the dominant feedback element is capacitive. The gain of the device is specified in units of V/pC (or pF^{-1}). The device produces a peak voltage output proportional to the charge received. It has a risetime corresponding to the integration and a long decay time constant (given by $R_i C_i$).

Charge-sensitive amplifiers usually are followed by shaping circuits. For high rates, pole zero cancellation often is used. The overall time constant is $(1/R + 1/r)^{-1} C$ if $R_i C_i = rC$. See figure 1.

A shaping circuit is used for optimum noise performance. Typically it is made of multiple stages of integrators and differentiators, producing a symmetrical output pulse. The time from the beginning of the pulse to its maximum amplitude is called T_m , often referred to as peaking time or shaping time. There is an optimizing value of T_m for every application. It depends upon the amplifier and the detector source capacitance. In general, larger detector capacitance requires larger T_m . Often practical considerations, such as rate, force the user to employ shaping times shorter than the optimum for lowest noise.

Fan-Ins and Fan-Outs

The function of a pulse fan-in is to add analog signals or to perform logical OR of digital signals. Like an amplifier, it may offer either bipolar or single polarity operation. For high duty cycle operations, direct coupling is important to prevent baseline shifts.

A linear fan-in is often used to provide a sum signal from calorimeters. This allows a fast total energy trigger to be configured. Also by routing the sum signal to a discriminator, the signal may also be applied to an ADC for more accurate measurements. A linear fan-out is used to distribute a fast signal to several 50Ω loads with no loss in signal amplitude. Because it is linear, it may be used with either logic or photomultiplier pulses. Direct-coupling is recommended if high-rate conditions are expected. Stability is important to prevent any interaction with other direct-coupled circuits. Reverse-termination of the outputs should be provided to prevent reflections at one output from being introduced into the other outputs.

Logic fan-ins and fan-outs perform the same functions as the linear devices, but operate with logic signals only. A logic fan-in gives the logical (as opposed to algebraic) sum of the input signals. Logic fan-ins and fan-outs deliver output pulses which are restandardized to normal logic levels with pulse widths equal to input signal duration.

The functions of fan-in and fan-out can be combined in a single unit, as in the Model 428F for linear signals and Model 429A for logic signals. Such units are very efficient for the many applications in which signals must first be mixed and then distributed to multiple points in a system (e.g., photomultiplier signals from a large

counter to be first linearly added and the sum delivered to both a discriminator and an ADC).

Discriminators

The function of the discriminator is at once the simplest and the most demanding in fast-pulse instrumentation. The discriminator accepts detector pulses, generally from photomultipliers, wire chambers, or streamer chambers and for each input pulse that is large enough to trigger it, delivers a standardized logic pulse.

The discriminator is the interface between the real analog world of the detector and the more ideal digital world of the logic system. At its input, it contends with signals having all the vagaries that random rates, shapes, amplitudes, and cabling techniques can produce. At its output, it delivers standard pulses related as closely as possible in time to the leading-edge threshold crossings of the input signal. These output pulses should be of standard amplitude and duration, completely independent of all characteristics of the input signal except time of occurrence.

Early discriminators were little more than gated oscillators, which challenged the user to maintain input pulses short enough to produce only one oscillator cycle. To do this, shorted clipping stubs generally were used on all discriminator inputs. These clipping stubs also served to eliminate rate-dependent shifts in the discriminator threshold, since these discriminators were also capacitively coupled.

Modern discriminators contain circuitry which assures that only one output pulse is produced regardless of the duration of the input pulse,

thus eliminating that need for clipping stubs. Direct-coupled inputs avoid the rate problems that earlier circuits would have experienced using unclipped inputs.

Eliminating the need for input clipping provides the experimenter the very desirable option (seldom utilized in practice) of terminating the photomultiplier at the anode to sharply reduce multiple-pulsing due to reflections. Reverse termination becomes increasingly attractive with newer discriminators offering low enough thresholds to compensate for the factor-of-two attenuation that it entails.

The input sensitivity or threshold of a discriminator is generally specified by a single number, typically 15 to 30 mV in modern circuits. In an ideal device this single number would be sufficient, but in real discriminators the threshold may vary with temperature, input signal risetime, and input signal duration. DC coupling has eliminated threshold dependence upon rate. In current LeCroy discriminators, temperature and risetime dependence of the threshold are negligible, and width dependence, though present, is noticeable only with photomultiplier signals <3 nsec in duration. For these very short input signals, characteristic of only the fastest photomultipliers, the measured threshold will be higher than nominal.

Input reflections probably account for the majority of multiple-pulsing problems encountered in an experiment, especially when a low threshold is employed. Unless the magnitude of input reflections is reduced along with the minimum threshold value, multiple-pulsing can negate the usefulness of a lower threshold. The input reflections of a discriminator effectively determine the allowable dynamic range of event or noise input signals.

On the experimental floor, a limited dynamic range may mean that minimum threshold values will have to be set higher to prevent multiple-pulsing on noise or large (shower) event signals. In addition, high input reflections also limit the ability of a discriminator to be used to restandardize logic signals which have been degraded by long cables.

The speed of a discriminator is usually defined in two ways, most usefully in terms of its double-pulse resolution (DPR) and also in terms of the maximum frequency of operation for continuous pulse train. The DPR of a discriminator is defined as the time between the leading edges of the most closely spaced pulse pair for which the discriminator produces two distinct output pulses. Most current discriminators have specified DPR's in the 5 to 10 nsec range.

The DPR of a discriminator is a strong function of the duration of the first pulse in an input pair, since this width effects the recovery time which is allowed for the discriminator input state between the two pulses. Where achievement of the best possible DPR from scintillator pulses is an overriding consideration, clipping cables are sometimes used at the photomultiplier anode to shorten the body of the pulse and to eliminate the slowly decaying tail.

DPR also depends upon input amplitude and is larger for pulses very near threshold. The continuous pulse train (or CW from RF terminology) response of a discriminator is usually somewhat slower than the reciprocal of the DPR. It is a more conservative number, but the DPR figure is more representative of the practical performance under random input conditions where nothing approaching a maximum rate CW signal exists.

At input rates which do not tax the double-pulse resolution of the discriminator, a class of characteristics comes into play which defines the fidelity of the discriminator output to the time information in the input signal. The most important of these, and the most difficult to strictly define and to measure, is time slewing. This is variation in the input-to-output time delay of a discriminator with input amplitude. The net slewing yielded by a discriminator has two components, one contributed by the discriminator itself (intrinsic slewing) and the other dependent upon the input risetime (walk).

Intrinsic slewing might be defined as the slewing measured with a delta function input. Risetime-dependent slewing arises from the fact that the discriminator fires earlier on the leading edge of a large pulse of finite risetime than on one of smaller amplitude. For an extreme range of pulse heights, the maximum contribution is equal to the 0 to 100% risetime of the pulse. This slewing folds in with the intrinsic slewing of the discriminator in quadrature.

No commonly accepted standard exists for measuring the intrinsic slewing characteristics of discriminators. LeCroy slewing specifications are based on measurements made with pulses having a 300 psec rise and a 3 nsec exponential decay.

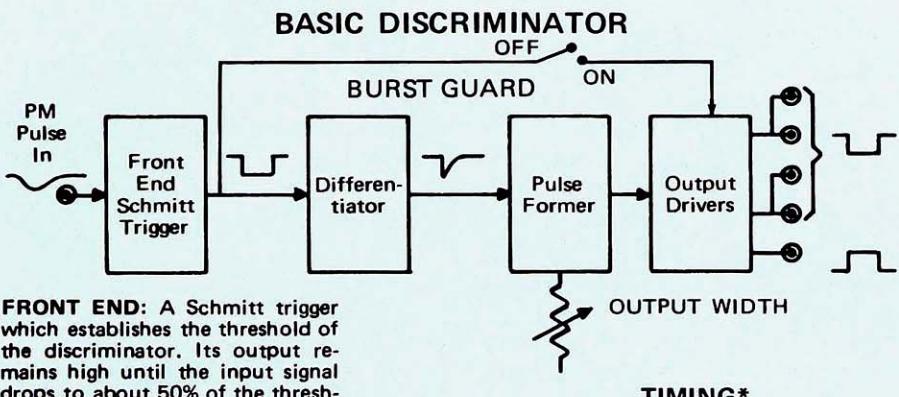
With most discriminators, by far the largest portion of the slewing occurs in the amplitude region just above threshold, threshold being defined as the input amplitude that produced 50% triggering. Slewing specifications are frequently given over an input amplitude range from threshold to a specified overload factor (such as 10 \times threshold).

Jitter, the short-term dispersion in discriminator delay for inputs of constant amplitude, is negligible on the order of a few tens of picoseconds in LeCroy discriminators.

General-purpose discriminators are provided with some means of setting the output pulse width. Early discriminator circuits used external cables or internal switched inductors to do this. Both of these techniques produced deadtime after each output pulse while the timing component (cable or inductor) recovered. Today, virtually all commercial general-purpose discriminators utilize a capacitive discharge pulse-forming technique which permits continuous front-panel control of output pulse width and which for most pulse widths introduces no deadtime after the pulse. This section is called the Timing Stage.

Two types of Timing Stages are common: updating and non-updating. Each type is most suitable for certain applications. The updating circuit resets its output timer each time a threshold crossing is detected. If an updating discriminator is triggered while it is producing a logical 1 state, the output is extended in time by the selected output duration. Updating is not the same as deadtimeless. If two threshold crossings occur closer together in time than the double-pulse resolution of the discriminator, the timing stage will be triggered only by the first one. The updating configuration is most useful when the discriminator is used for DC coincidence logic. The discriminator output width may be set rather wide without causing appreciable deadtime.

The non-updating timing stage cannot be retriggered until the output stage has returned to its logical zero stage and recovered.



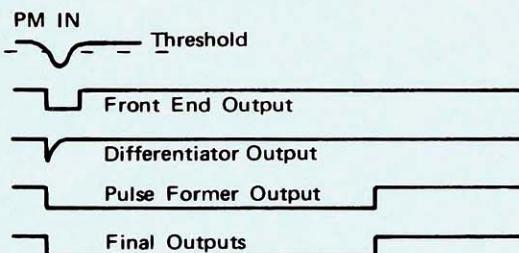
FRONT END: A Schmitt trigger which establishes the threshold of the discriminator. Its output remains high until the input signal drops to about 50% of the threshold level.

DIFFERENTIATOR: Delivers a short spike (typically 1-3 ns) at the leading edge of the front end output.

PULSE FORMER: Determines duration of output pulse; usually in accordance with front panel control setting. Updating type now standard in general-purpose discriminators.

OUTPUT DRIVERS: Amplify and shape pulse former output to drive required number of cable loads.

BURST GUARD: See text.



*Internal Stage delays not shown; amplitudes and polarities arbitrary.

Figure 2

The deadtime of this type of discriminator is greater than the updating type for all but minimum width. Nonetheless, for high input rates the non-updating discriminator offers advantages in counter and timing applications. The counting rate (i.e. the rate of output pulse leading edges) of a non-updating discriminator is monotonic with input rate. In contrast, the updating discriminator "locks on" under high input rates.

Burst Guard: When a discriminator receives an instantaneous burst rate at its input that exceeds the bandwidth of its input stage, it is unable to resolve the individual pulses in the burst and in effect, internally integrates the burst into a single pulse of duration equal to the burst duration. The discriminator provides a single output pulse at the beginning of the burst and is then paralyzed until the burst is over. To minimize deadtime due to this effect, LeCroy has introduced an operating feature called Burst Guard. In the Burst Guard mode the discriminator front end is OR-ed with the

pulse-former stage to drive the output stage (see diagram). The output duration is then the preset duration or the input pulse duration, whichever is longer. The discriminator thus gives an output throughout the time the input stage is held on by a high-rate burst, and discriminator efficiency in critical veto applications is preserved even under such severe rate overload conditions.

Inhibit: A discriminator inhibit represents an input which is used to disable the input to the discriminator's timing stage. It is used to allow complex triggers of downstream counters by those upstream. In addition, it may be used in an "enabling" mode by supplying complementary logic signals to it. This technique is especially useful to serve as a crossing gate at pulsed-colliding beam machines.

Summing Output: A multiplicity trigger is one which defines the simultaneous firing of a number of detectors. This can be configured easily using a discriminator summing output which produces an out-

put proportional to the number of discriminators whose outputs are in the logical 1 state. The summing output applied to another discriminator produces a multiplicity trigger.

Coincidence or Logic Units

A coincidence or logic unit generates an exactly timed output signal whenever the time overlap of input signals satisfies a preselected coincidence requirement.

The **majority logic** unit is the most flexible and useful type of coincidence circuit. Unlike the simple AND (NAND) or OR (NOR) circuits, it permits any logical combination of input signals to be required for an output. For example, the functions available from a 4-fold majority logic unit with inputs A,B,C,D are shown in Figure 3.

Additional logical flexibility is provided if the **majority logic** circuit will accept **complementary logic**. A logic signal which is quiescently at the logical "1" state and switches to the logical "0" stage during a pulse interval is called complementary. Many discriminators and logic units provide one or more of these outputs. When used to drive a logic unit, a complementary signal will serve as an inhibit for that input, effectively increasing the coincidence requirement by one.

An **inhibit** input serves as a second stage of logic after the coincidence level logic. Receipt of a veto signal at any time will inhibit the output of the logic unit regardless of the state of the other inputs. To be effective and to eliminate any unnecessary system dead-time, it is important that the inhibit input and subsequent logic be as fast as the coincidence logic stage.

A slower but frequently used form of inhibit is provided by

INPUTS CONNECTED OR ENABLED	FUNCTION	COINCIDENCE LEVEL	DESCRIPTION
4	A + B + C + D	1	4-fold OR
3	A + B + C; B + C + D; A + C + D; B + A + D	1	3-fold OR
2	A + B; B + C; C + D; D + A; A + C; B + D	1	2-fold OR
1	A, B, C, D	1	Pulse Standardizer
4	A•B + A•C + A•D + B•C + C•D + B•D	2	2-fold majority, any 2 of 4
3	A•B + C•A + B•C; B•C + C•D + D•B; A•C + C•D + D•A; B•A + A•D + B•D	2	2-fold majority, any 2 of 3
2	A•B, A•C, A•D, B•C, C•D, B•D	2	2-fold AND
4	A•B•C + B•C•D + A•C•D + B•A•D	3	3-fold majority, any 3 of 4
3	A•B•C, B•C•D, C•D•A, B•A•D	3	3-fold AND
4	A•B•C•D	4	4-fold AND

Notation + = OR, • = AND

Figure 3

the NIM standard **bin gate**. This input, connected to the module via pin #36 of the rear power connector, will inhibit the entire unit whenever the quiescently positive voltage level is clamped to ground. The rise- and falltimes of the bin gate are 30-50 nsec and it is generally used to inhibit an entire logic system between beam spills of a particle accelerator or to record background between spills.

The performance of a majority logic unit is defined by four characteristics: double-pulse resolution; coincidence width; coincidence overlap; and time resolution. As with a pulse amplitude discriminator, the double-pulse resolution defines the ability of a logic unit to respond to two or more closely spaced input signals. It is important that this definition also include the unit's maximum response to logic decisions of the highest order (i.e., 4-fold coincidence with veto.)

The coincidence overlap is the minimum input overlap required before the logic unit will acknowledge the simultaneous presence of input signals and produce an output. This specification generally also defines the minimum width of the input signals.

The coincidence width of a logic unit is the FWHM of the narrowest coincidence curve and together with time resolution indicates the unit's ability to distinguish simultaneity. The time resolution defines the effective slope of the coincidence curve. For good coincidence units, the time resolution should be such that the transition from 100% counting efficiency to 1% efficiency is made in a few tens of picoseconds.

Two different kinds of outputs are available from logic modules: time overlap and updating preset outputs. A time overlap circuit (often called a logic gate) produces an output pulse whose width is equal to the time over which the input signals satisfy the coincidence requirements. Better circuits of this type also provide a fixed-width output for use where it is desired to have a known coincidence width in subsequent logic. Deadtimeless coincidence circuits generate an output whose duration is independent of input conditions and is preselected by a front-panel control. In all cases, only one output pulse should be generated regardless of the duration of the input signals.

Registers

A coincidence register or latch is used to record 2-fold coincidences between a common gate input and any one or more of n input signals. The time coincidences, which represent the pattern of counter pulses existing at the time of the gate, are stored as DC levels in a fast buffer register for later readout to computer or other digital input device. Two common applications involve latching of signals from hodoscopes and from multiwire proportional chambers.

While the coincidence section of a register seldom encounters high rates, it is important that the preceding discriminator exhibit good speed characteristics so as not to compromise the data with excessive deadtime. Since the counters used are often small and far removed from the discriminator inputs, a lower threshold should be provided. The output width of the discriminator should be matched to the coincidence circuit and kept under 3 nsec if optimum timing accuracy is required.

The gate signal for a register is generated by conventional logic modules. The duration of the gate input pulse determines the coincidence width and is typically set to cover jitter in the counter inputs.

Coincidence registers can also provide fast logic outputs in addition to the digital output. These may be prompt outputs from each 2-fold coincidence indicating that the respective latch has been set or a majority logic function output indicating that one, two, or more coincidences have been detected. These prompt outputs are generally used for prefiltering the data prior to firing wire chambers or other counters which have substantial deadtime.

Another example of fast logic outputs is the summing output. It is a current which is proportional to the number of hits latched in the register. The summing output applied to a discriminator produces a multiplicity trigger.

Trigger Logic in ECL: A New LeCroy Standard

Most modern NIM and CAMAC fast logic modules make extensive use of ECL integrated circuits. To make NIM modules compatible with current practice requires adapters for NIM to ECL at the input, and ECL to NIM at the output, adding unnecessary cost and power consumption. The use of ECL levels as the standard for input and output is an obvious advantage.

There are several other major advantages to an ECL approach to modern logic systems:

- ECL inputs and outputs can be complementary, permitting high-density connectors and cheaper twist-pair cable.
- Better noise immunity with no appreciable loss in bandwidth.
- Elimination of ground currents and ground loops which frequently cause problems in single-ended circuits.
- ECL input impedance is intrinsically high, permitting much greater fan-out, with termination needed only at the last circuit fed.

The CAMAC standard offers the additional advantage of adding remote programmability to a logic system which is quite meaningful in the new generation of high energy physics experiments involving extremely high counting rates and/or large detector arrays. These new needs impose severe limits on cost and space per channel and require

the most extensive, flexible computer control obtainable.

LeCroy recognizes these needs and has, therefore, developed a new line of ultra-fast, high density, programmable modules. ECLline allows the experimenter to achieve full computer control, automated test and monitoring of the data acquisition system within a single instrumentation standard.

ECLline Configurations

LeCroy has established standards and protocol for ECLline as follows:

Connectors and Pin Allocations

Lemo connectors are used to input signals appropriate to coaxial cables, such as the low-level inputs of the 4416B Discriminator and for logic bus signals such as strobe, test, or veto inputs.

Lemo connectors and NIM levels are used for outputs which usually go to a simple logic gate, such as majority outputs and synchronization outputs.

To maximize the logic elements in each ECLline module, all other signals are routed via 34-pin (2×17) connectors. Mating connectors are available from a number of manufacturers, including AMP, 3M, and Berg. Pin allocation is shown in Figure 4. An arrow on the front panel points to

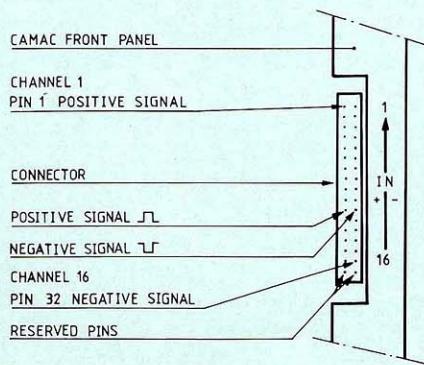


Figure 4

channel 1. Pin allocation is compatible with the CERN "Specification for ECL Front Panel Interconnections" (CERN, EP Electronics Note 79-01).

Front Panel Organization

ECLline Modules are, by definition, single-width CAMAC modules. The front panel is organized in four sections, each housing either a 34-pin connector, or such components as Lemo connectors, LED displays, or trimmers. Connector groupings are shown in Figure 5, and are arranged to make modular interconnection as easy as possible.

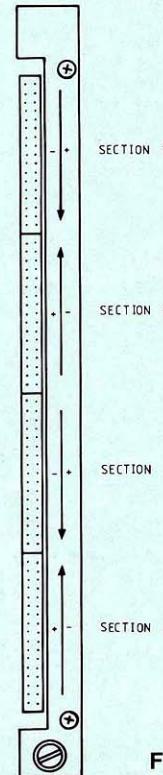


Figure 5

Interconnections between Modules

Either single twisted-pair cables and connectors or flat multiwire cable may be used. The non-twisted flat cable is suitable for distances less than a few tens of centimeters, or when higher crosstalk is acceptable. For maximum performance, use twisted-pair cables of nominal $100\ \Omega$ impedance.

Input connectors are routed within the module to a stan-

dard resistor terminating array, which may be removed to provide a high input impedance when several modules are driven from a common bus. The last module in the bus is the only module to use the termination. A sample bus configuration is shown in Figure 6, with Module 1 the signal source, and Modules 2 and 5 requiring termination.

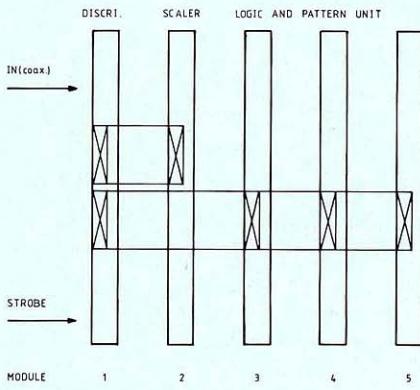


Figure 6

Interconnections with Old Standards

ECLine includes modules with NIM-to-ECL and ECL-to-NIM translation to interface where necessary with classical NIM circuits. There is also a specially designed differential active probe for this purpose. Where frequency response is not critical, the user may fabricate the very simple translator shown in Figure 7.

Sample Applications

ECLine provides a major advancement in logic flexibility and adaptability to experimental needs, permitting the solution of any logic problem with compact, computer-controlled hardware. The best way to gain familiarity with the potentiality of this new tool is to present us with your logic problems, and let us propose a solution. The following representative samples are given to help you understand the range of problems ECLine can solve.

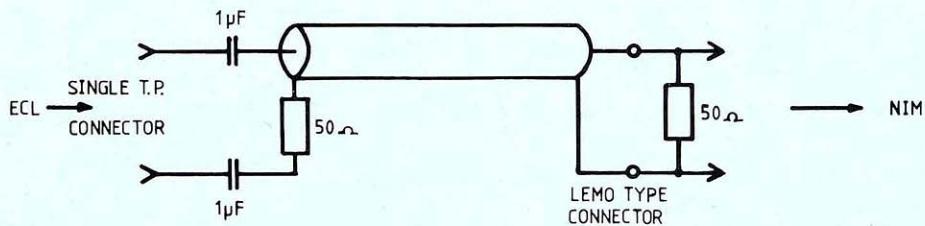


Figure 7

Automatic Coincidence Curves

A typical application for the Model 4416B Discriminator and Model 4418 Programmable Logic Delay is shown, with two different topologies for the interconnecting cables, in Figures 8A and 8B. This application presumes a unique light source for the photomultipliers, triggered by a common strobe generator.

Mixed Logic

The logic block diagram shown in Figure 9 is a typical example of a trigger built with eight counters plus a strobe. ECLine offers two ways to implement it. The first (slower) way uses four sections (1/4 module) of 4516 3-Fold Logic Unit, and includes all circuits shown in the dotted box, except for the dotted output connections. The fanout of two,

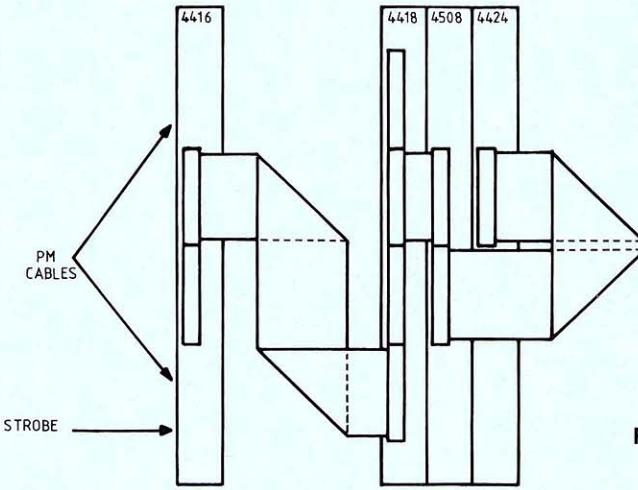


Figure 8A

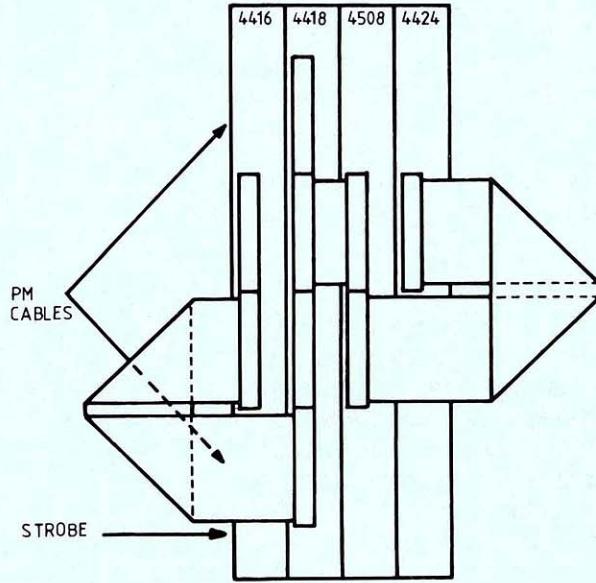


Figure 8B

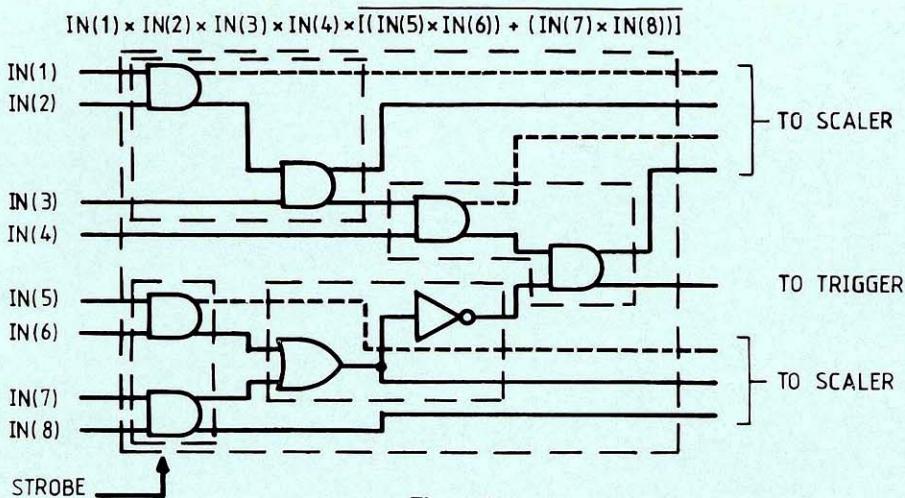


Figure 9

not provided in this case, can be made by using a bus connection; the complementary output can be obtained by inverting the cable connection. Delay from input to final output will be in the order of 22 nsec plus the delay of the interconnecting cables.

The alternate way is to use one section (1/2 module) of the 4508 Fully Programmable Logic Unit (or Memory-Look-Up). This represents the ultimate in simplicity and flexibility. Connect the inputs and program the Boolean expression via CAMAC. All eight outputs will be available, plus a strobe. Input/output delay is in the order of 20 nsec. Another nice feature is that the input pattern is latched upon strobe arrival, permitting an off-line reconstruction of the trigger.

For applications involving more centers, a wider memory-based logic unit, such as the LeCroy 2365 or 2372, may be used at an increase in propagation delay. This will be compensated for by eliminating the need for Logic Fan-In.

Coincidence Matrix

Another typical application for High Energy Physics is the correlation of two counters of hodoscopes to produce a trigger only when collinearity criteria have been respected. The arrangement in Figure 10 uses two 4508 Fully Programmable Logic Units and one

4516 3-Fold Logic Unit. For a given pattern on the first hodoscope plane, the system predicts a pattern for the second plane. A bit-by-bit comparison can then be made between the predicted pattern and the real one. The resultant output will be a 16-bit word containing 1's where collinearity has been respected. This word can either be sent to a pattern unit, or the 16 bits can be ORed to provide a trigger.

Each 4508 section produces an 8-bit predicted output. Each group of eight counters in the

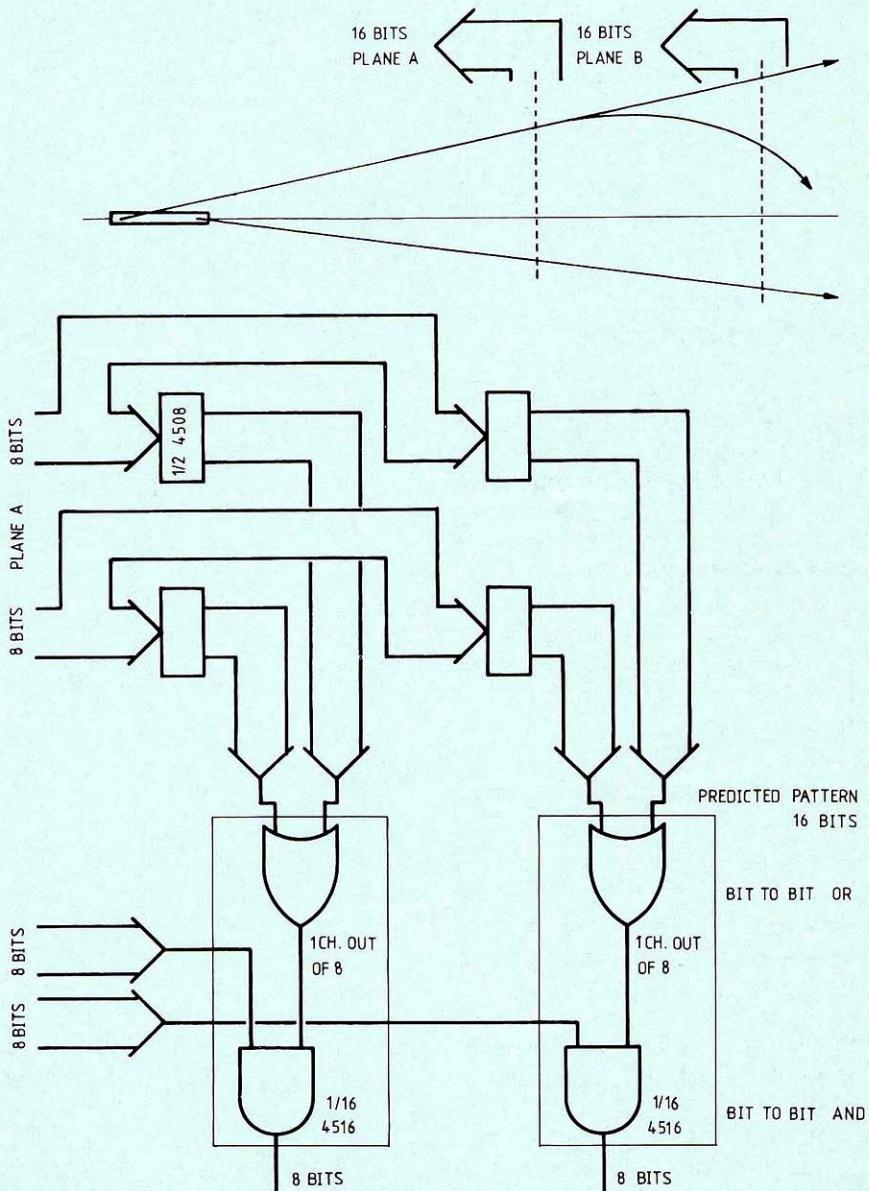


Figure 10

A-plane can influence, a priori, each of the 16 counters in the B-plane. The exact relationship is controlled by the set-up geometry and/or the use of a bending magnet between the two planes. The bit-to-bit OR compares this relationship. The predicted pattern must allow for the fact that the shadow of each A counter may cover more than one B counter.

All logic operations may be programmed into the 4508 from the CAMAC computer. The bit-to-bit AND is formed in the second half of the 4516. The 4516 output will provide both the 16-bit final pattern and the 16-bit general OR. The total decision time will be less than 40 nsec. Any number of hodoscope tracks may be accommodated by this scheme, and the principle may be extended to any number of counters.

Digital Majority

Analog techniques are neither convenient nor reliable for obtaining majority information from a set of counters reading more than 16 hits. Digital techniques provide unambiguous information and are easier to use, as shown by the following examples.

1) Figure 11 is a majority logic system for 32 inputs, using four 4508 Fully Programmable Logic Units (eight sections). Each section in the first level is programmed to provide a binary coded output on a convenient number of bits, as indicated. The remaining 4508 sections perform the sum of the two binary numbers present at the input, and provide an output.

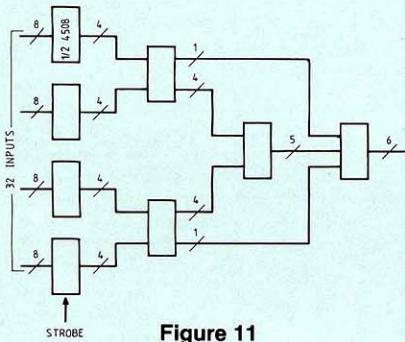


Figure 11

The last 4508 section can be programmed for an output that represents any multiplicity. It could be coded, for example, on six bits (for six of the eight outputs). An additional output could be programmed to provide an output when the multiplicity exceeds some preset value. The same program could be loaded to give the last output a higher fanout.

Two 4416B Discriminators may be used to generate any desired pattern to test this logic system. This will provide a very powerful way to exercise the logic through all possible combinations.

Since the 4508 latches the input pattern, the pattern may be reconstructed for detailed off-line investigation.

Since the system works with levels as well as with pulses, timing problems between different logic levels are completely avoided by the 4508. Once the 32 inputs of the first level are timed, a strobe can be applied, permitting all succeeding operations to be carried on with levels.

The total decision time of this arrangement is in the order of 80 nsec.

2) A system consisting of one or more Majority Logic Units (MALU's), a Flash ADC, and a Memory-Look-Up (MLU) provide an elegant and fast solution for applications requiring majority information up to 16 hits from more than 32 inputs. It is also suitable for applications that deal with clusters as opposed to single hits.

The LeCroy Model 4532 Majority Logic Unit may be used either in single hit or cluster mode providing single hit multiplicities (up to 16) or non-adjacent hit multiplicities respectively. In cluster mode, provisions have been made for Cluster Carry In/Out signals so that clusters may logically ex-

tend over more than one MALU module. Furthermore, the analog outputs of several units may be cascaded permitting majority information to be generated from an arbitrary number of inputs.

The analog outputs of the MALU's are fed to a LeCroy Model 4504 Flash ADC where they are converted to a 4-bit digital word. This digital word can be then passed to a Model 4508 Fully Programmable Logic Unit used as a Memory-Look-Up. The latter is capable of making complex trigger decisions on both the multiplicity and other logic conditions permitting almost any logic configuration.

Since the hit pattern of the MALU's may be read via CAMAC, the entire logic chain may be checked off-line. In addition, LeCroy ECLine discriminators may be used to simulate any input pattern for beam-off testing.

The timing of the system is greatly simplified through the use of the Self Triggering Mode of the MALU and the free running Sample Mode of the Flash ADC. The transit time of the system is about 60 nsec and the entire chain can be run at 65 MHz.

Third Level Triggers — Trigger Processors

Multilevel triggers are a composite of several successive triggers, each of increasing restrictivity. The combination allows complex and selective trigger with much lower dead time than a comparable single level trigger. Each level of trigger provides a filter for the next level so somewhat slower sophisticated triggers can be employed.

These types of decisions can include computer calculations. In fact, a fourth level

trigger is often based upon a fast microcomputer such as the LeCroy Model 4800 CAB. In many applications, however, the milliseconds required for such a decision are too great. To perform an analysis in a much shorter time requires a special hardwired computer called a trigger processor.

The 2300 series of ECLline-compatible data handler modules can be used as a trigger processor providing the equivalent of 50-100 nsec execution time per line of Fortran Code. This results in 1s to 10s of μ sec to make high level decisions. Formally, the system is an asynchronous data handler consisting of sequencing and data processing modules.

First- and second-level trigger logic employs discriminator and coincidence pulses wired from module to module in order to form a trigger. Trigger processors employ the same logic levels but the meaning of the signals is not the same. These signals form words just as they are used in digital computers. These words represent physical quantities like momentum, mass, energy or angle.

Data Transmission

The system employs a 16-bit data field. Digital words are transmitted between modules as differential ECL signals. Twisted-pair ribbon cables are used. The standard pin-outs of the ECLline are used throughout.

The system also employs data strobes to time the data-flow. Each module provides a logic transition (edge) to indicate that a new data word is valid at the output. This signal is called Output Ready. It and the output word remain valid until the next request is made of the module. A timing diagram is shown in figure 12.

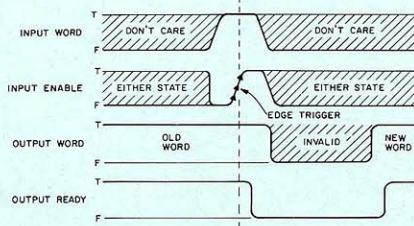


Figure 12

Modules also accept Input Enable signals. These are used to latch a Dataword or a Read Request into a module. Datawords may be comprised of several fields. Thus, the Trigger Processor modules accept multiple Input Enable signals and latch their input word only when all used inputs are valid.

Datawords are transmitted out of the processor modules along with Output Ready strobes. Both the data and the strobes are applied to the next module in the trigger processing chain. The Output Ready signals are applied to the Input Enable input of the next module. A typical interconnection is shown in figure 13.

The Memory-Look-Up Unit

The fundamental unit used in the LeCroy trigger processor is the Memory-Look-Up unit, Model 2372. The device is a large (64K bits) memory with ECL inputs and outputs via the front panel. The memory can be written into via CAMAC. Any function may be written into the MLU, limited only by the memory size. In many applications, a collection of MLU's can be used as a trigger processor. Several examples are given below.

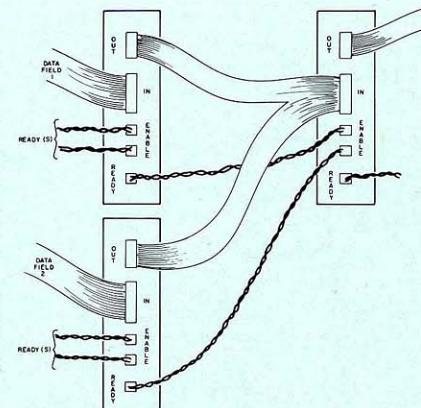


Figure 13

Calibration of ADC's: The MLU is large enough to contain all of the calibration constants for 32 8-bit ADC's such as the LeCroy 4300 Series. Rather than loading 32 pedestals and 32 values of gain into a computer, the MLU is loaded with the number of GeV that each possible output value represents for each ADC. The input word then consists of 8-bits of ADC value and 5 bits of ADC number. This 13-bit word serves as the input to an MLU, resulting in an 8-bit ENERGY output. See figure 14.

Note that the above scheme works well even when ADC's with nonlinear transfer characteristics are used (e.g., logarithmic or quadratic). Operation requires only loading the proper table within the MLU.

If the number of ADC channels is large or a higher resolution ADC trigger is required, a wider MLU input is needed and the number of MLU's increases. For example, with 10-bit ADC's the system could operate as shown in figure 15.

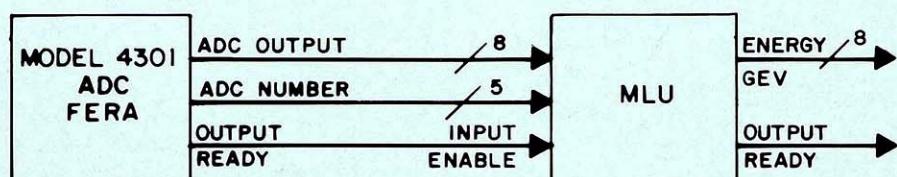


Figure 14

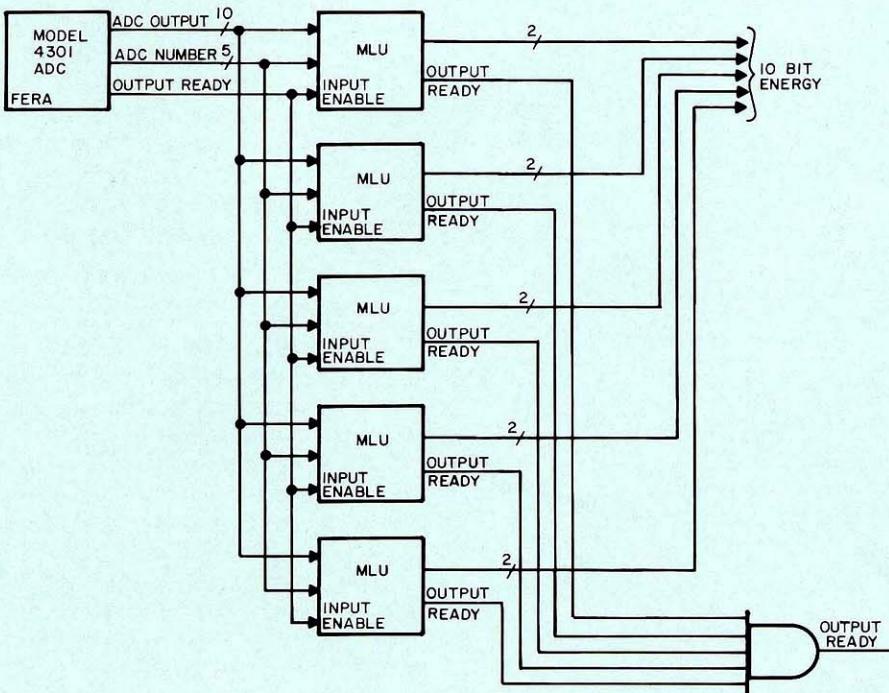


Figure 15

Because each input bit to the MLU in excess of 12 costs a factor of two in the number of output bits, it is necessary to employ tricks to keep the number of input bits to a minimum. For example, logarithmic coding can be useful. Also, calculations which may be broken into steps can be done with several cascaded MLU's.

As an example, the same ADC calibration calculation above can be done in steps. Assuming that the response of the ADC's is linear, the MLU's can be used to provide simple arithmetic. See figure 16. In

this example, the pedestals and gains from up to 4096 ADC's can be stored in a single MLU called the Constant Table.

The pedestal can be characterized by a 6-bit number and thus may have 63 values. If the pedestal values are 40-100, they may be represented by 6 bits even though their absolute values require 7 bits, i.e., the value recorded is pedestal minus 40.

The pedestal word from the Constant Table and the ADC output comprise the input to the second level of MLU which

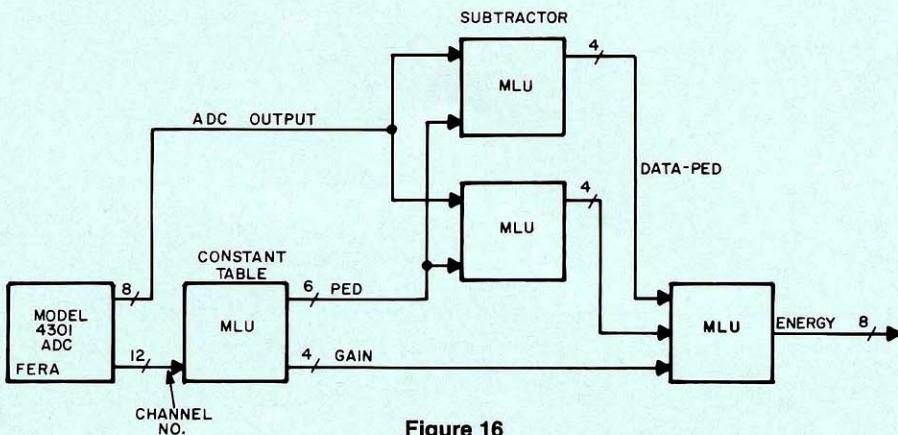


Figure 16

provides the subtraction operation. Because the input is 14 bits wide, two MLU's are required to provide an 8-bit wide output, DATA-PED.

The result of the subtraction and the 4-bit gain word from the Constant Table allows conversion to energy units. A 4-bit gain word allows the unit to perform the multiplication operation to $\pm 1\%$ even though the gain of the channels only match to $\pm 8\%$.

The system described above employs 4 MLU's to provide calibration of up to 4095 channels of ADC. This is to be compared with the system in Figure 14 which requires one MLU for 32 channels.

Calculate Momentum: Often an experiment involves measuring the momentum of a particle by passing it through a magnet and measuring the amount that bends. The momentum can be calculated in terms of the bend angle and the magnitude of the magnetic field. As above, the MLU's produce no calculations but rather, are down-loaded with the results of the calculation for all possible input words.

For an idealized experiment which involves no multiple tracks, a system as shown in figure 17 could be used. In fact, multiple hits complicate the trigger. The more realistic multihit case is discussed below.

The position of the track is recorded using MWPC's. The addresses are encoded by a system such as PCOS III and transmitted to 2 MLU's. The ECLport output of PCOS III is pin-for-pin compatible with the MLU. Also, the Data Ready Output on the 2738 may be used to drive the Input Enable of the 2372.

As shown in figure 17, the first-level MLU's are used to calculate the angles Θ_B and Θ_A before and after the magnet. Note that both MLU's receive

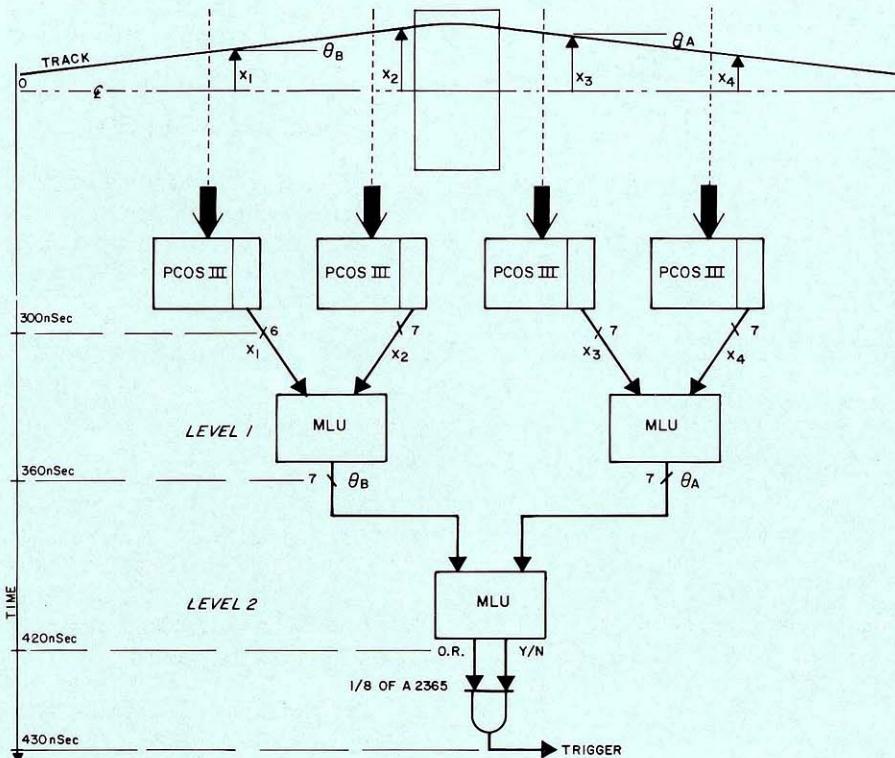


Figure 17

their input word from two sources. The Θ_B MLU has a 13-bit input which allows up to 8 bits of output. In this case, 7 bits are employed.

The Θ_A MLU has 14 bits of input. Under this condition each 2372 can provide 4 bits of output. Thus, two MLU's are required, one operating in the Hi Z input mode. This allows 14 inputs plus 8 outputs. Seven outputs are used.

As shown in figure 17, the first level MLU's produce a composite 14-bit dataword which is applied to the second level MLU. This device can be used to complete the momentum calculation or to provide a 1-bit trigger output.

The timing of the data transfer through the trigger processor above is done using the Output Ready/Input Enable strobe system. Strobes are not shown in figure 17.

The Stack

The example above is based upon single tracks. If there are multiple tracks through the apparatus or multiple hits per

plane, additional electronics are required to STORE and SEQUENCE the datawords. Model 2375 Data Stack module is designed for this purpose.

The Stack shown in figure 18 is a dual-ported memory which can be written into sequentially from the front panel. It can be accessed from the front panel, either at random or se-

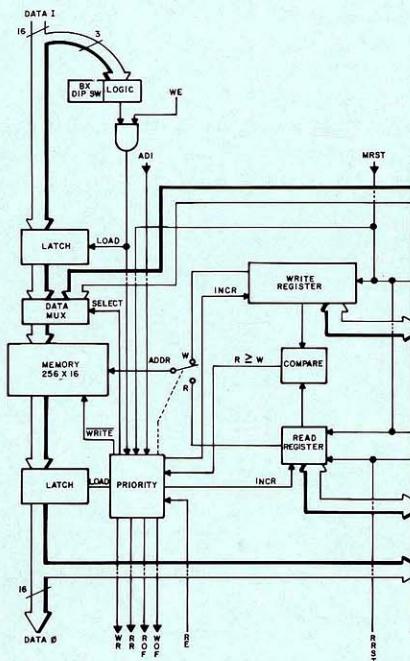


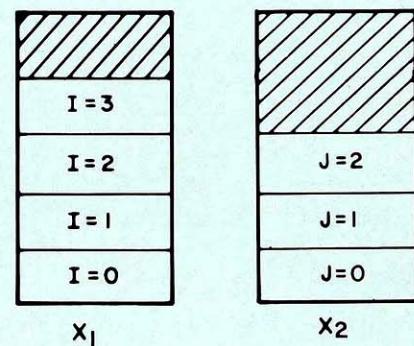
Figure 18

quentially. Its most common use is in dealing with data lists of unspecified length. Its Sequential readout mode allows it to act as a data sequencer similar to a Fortran DO Loop. Stack modules can also be nested just as would be done with software.

Each successive Sequential Read Enable (SRE) pulse initiates a fetch of the next word written into the Stack. Reading the last word causes a Read Overflow (ROF) output to be asserted. The next ROF trailing edge resets the read counter to the first address within the Stack. The combination of this wrap-around feature and the ROF signal allow for the NESTING of stacks.

Suppose for simplicity that in the example above the beam is well collimated and of a very small size. Then only the angle after the magnet need be considered. If it is necessary to calculate the momentum of all tracks which intersect the beam, a stack and several MLU's may be used. See figure 19.

In the example above, the forward chamber produces four hits and the rear chamber three. The two stacks are operated in the sequential write, sequential read mode. Before the event is recorded, a write reset (WRST) pulse is applied. This sets the read and write pointers to address zero. The encoded hit wire numbers are loaded into the two stacks one-by-one. The result is that the stacks are loaded as shown below.



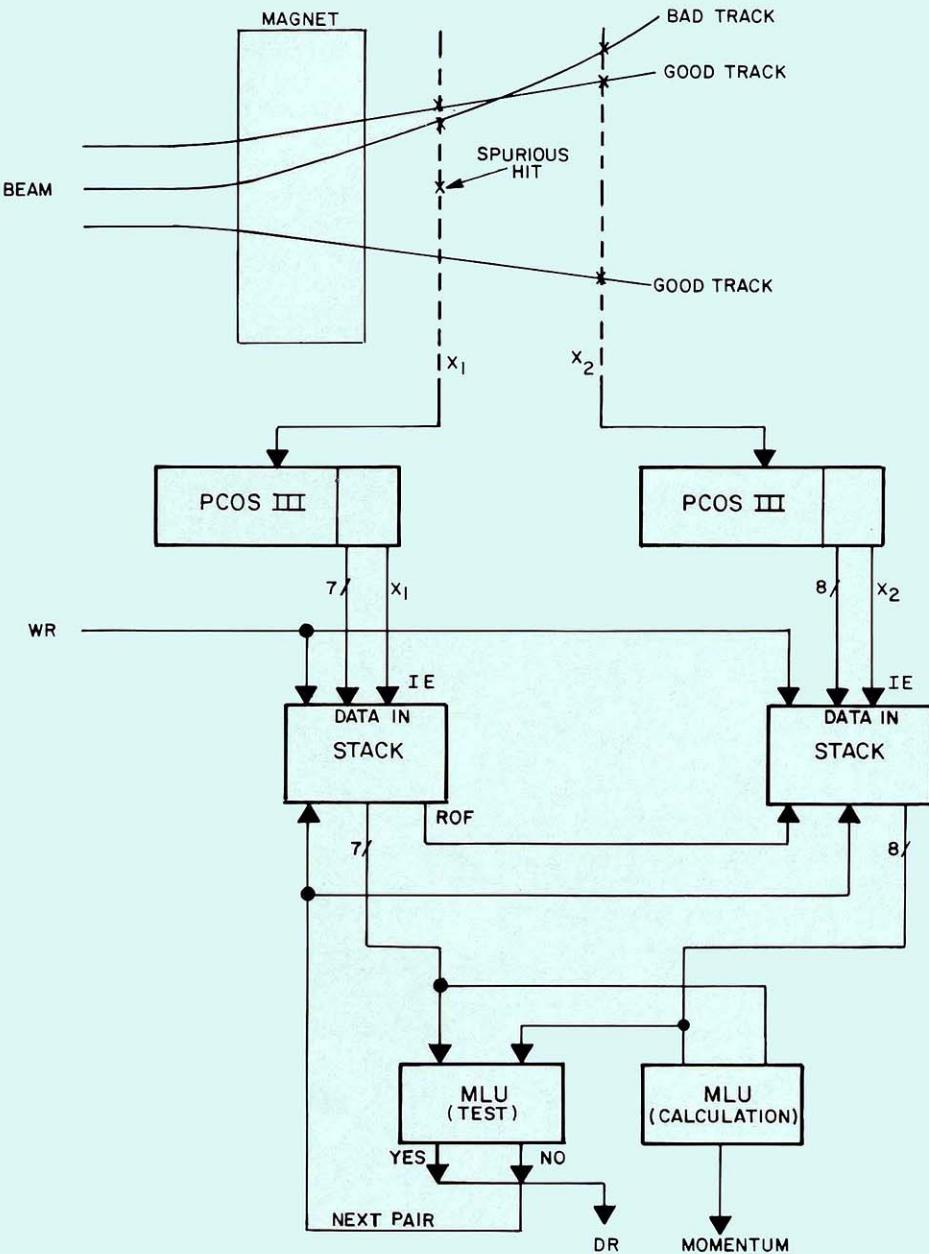


Figure 19

As soon as a word is loaded into the Stack, it provides the zeroth word at its Data Output. Thus, the two stacks produced a composite output word $I = 0$, $J = 0$. This results in a word applied to the Test and Calculation MLU's. The purpose of the Test MLU is to determine that a fit has been achieved by the combination (I_1, J_1) and the loop should be exited or that the next pair should be tried.

The next pair signal is applied to both stacks. However, the ROF signal (complement of end of data) inhibits the next signal at the X_2 stack. Thus,

the following pairs are applied to the MLU's by the stacks:

$$\begin{array}{ll} X_1 & X_2 \\ I = 0 & J = 0 \\ I = 1 & J = 0 \\ I = 2 & J = 0 \\ I = 3 (\text{ROF} = 1) & J = 0 \end{array}$$

The subsequent next pair causes the X_1 stack to wrap to $I = 0$ and owing to the $\text{ROF} = 1$ condition, advances the X_2 stack. The next two pairs are:

$$\begin{array}{ll} I = 0 & J = 1 \\ I = 1 & J = 1 \end{array}$$

The latter pair is the "good track" which causes the loop to be exited with the calculated

momentum at the output of the Calculation MLU. The "yes bit" and the Data Ready strobes may be used to latch the dataword into the next level of the trigger processor.

The Data Handler System allows a variety of high level triggers to be achieved with ease. The system is compatible with the ECLports of the FERA and PCOS III Systems.

Complex triggers such as particle identification, track recognition and vertex location are among the applications.

Data Transmission Sources and Sinks

The system used for data transfer between trigger processor modules is called ECLbus. It involves separating data words as a set of parallel differential ECL levels on a twisted pair cable. A differential ECL strobe signifies that data is ready (DR). This system can be used to transfer data over 30 m at 10 megawords/sec.

The ECLbus is a general method for data transfer. It allows data words of any width to be transferred between modules. Data sources employ an ECLport to provide parallel words and a DR strobe. The Fast Encoding and Readout ADC (FERA), the PCOS III and 1821 FASTBUS Segment Manager Interface have ECLports.

Standard trigger processor techniques can be used to restructure the data as it pipelines through the ECLbus. Common applications include logical address assignment, calibration and data list reordering.

Data, either new or restructured, is presented to one or more of a variety of data destinations. Presently available are two multiple-port data memories. The CAMAC Model

4302 16K \times 16-bit memory accepts data words at a 10 megaword/sec rate and may be read either via CAMAC or via the 4800 Series CAMAC processor. The FASTBUS Model 1891 256K \times 32-bit memory accepts 16- or 32-bit data words at up to 10 megawords/sec. The 1891 is a true multiple-event buffer. It organizes data event-by-event and may be read via FASTBUS simultaneously with data write via the ECLport.

Time Interval Measurement

Time measurements typically involve the use of a pulse discriminator and a time-to-digital converter (TDC). Applications involving low level signals, may require an amplifier preceding the discriminator. Although the properties of the detector limit the time resolution, the electronics can also contribute. The jitter and slewing properties of the amplifier and discriminator as well as that of the TDC can, however, be made negligible for most applications.

In practical applications, timing can be degraded by noise. Pickup induced on the input signal results in time jitter. This is particularly important for drift chamber or other applications involving low-level signals. In many cases, AC coupling of the amplifier/discriminator input can be helpful in reducing low-frequency noise, pickup from powerlines. At high rates, however, AC coupling can result in baseline shifts which yield timing errors.

Long cables between the discriminator and the TDC may be required either for geometrical reasons or to account for the delay in forming an event trigger. Dispersion in the cable causes the logic pulse to be degraded in amplitude and in risetime. As a result, sensitivity to noise in the cable is

increased. For long cable runs, low loss cable is required. Double amplitude, 32 mA NIM pulses offer a factor-of-two better noise immunity over single NIM levels. The stop inputs of some TDC's like the LeCroy 2228A offer high sensitivity. By triggering at approximately half NIM amplitude, the unit can accommodate cable losses. Also, the faster edge-speed at half amplitude offers better noise immunity.

For drift chamber applications, very long cables are usually required. However, the time resolution rarely must be better than 2 nsec. Several other error sources in the detector (such as gas dispersion) besides the "quantum" error of the electronics combine to de-emphasize small improvements in the inherent resolution of the electronics. For these reduced timing requirements, more dispersive cable may be used, offering a cost advantage. The increases in dispersion can be offset by driving and receiving differentially. This offers a factor-of-two increase in effective edge-speed. Also, differential receiving of the logic level offers common mode rejection of noise caused by pickup.

Wide variation in the detector output amplitude can create the greatest degradation in time resolution. If the output range extends from the discriminator threshold to several times threshold, the trig-

gering point will vary according to risetime of the detector, causing shifts of 2 nsec or greater. In addition, wide variations in detector output, particularly in the region of the discriminator threshold, will contribute up to 1 nsec of time smearing due to discriminator slewing.

The effects caused by input pulse risetime (walk) and by discriminator slewing can be minimized either by lowering the discriminator threshold or by employing an amplifier preceding the discriminator. Noise on the input signal may limit this technique.

The dispersion in timing due to the amplitude variations of the analog input are reproducible. As a result, they may be accounted for if an ADC is used to record the analog signal. Data may later be corrected using a simple algorithm. A variety of special timing discriminators has also been developed to directly correct for these effects. However, their jitter limits the resolution they can achieve. Best results are obtained with amplitude correction.

The jitter of a counter assembly depends upon the geometry of the scintillator and the transit time characteristics of the photomultiplier. In general, the fewer paths available for light or electron transmission (as provided by small geometry and limited use of

MEASURING NANOSECOND TIME INTERVALS WITH AN INTEGRATING ADC

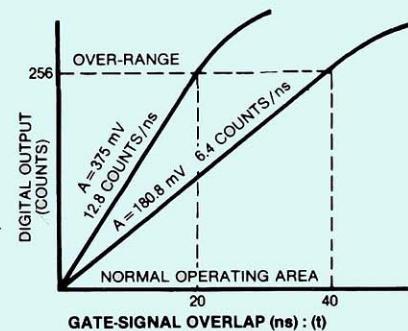
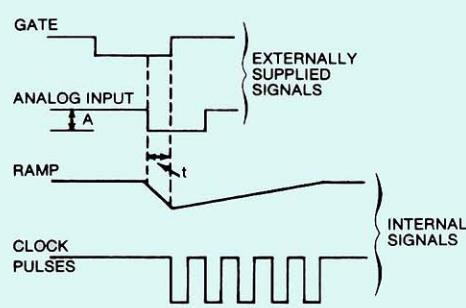


Figure 20

the photocathode surface), the better the timing.

The electronic resolution of the measuring instrument is generally not a practical limitation for time measurements under several hundred nanoseconds. Precise digital measurements of a few tenths of one percent of the full-scale range to be covered may be achieved with either an ADC or a time-to-digital converter.

An ADC may measure nanosecond time intervals from 5 to 50 nsec by integrating the pulse overlap of two standardized timing signals. The maximum time range is determined by the width of fixed-amplitude discriminator output signals applied to both the analog and gate inputs. When both signals are fully coincident, the instrument analyzes a pulse area corresponding to a zero time difference, and, if the amplitude of the analog input has been suitably adjusted, produces an output corresponding to full scale of the ADC. As the input signals are displaced in time, the input overlap is decreased and the reduction in the magnitude of the ADC's output is directly proportional to the relative time displacement. As is true with all overlap techniques, the output is symmetrical around zero.

A time-to-digital converter generates a binary digital output which is proportional to the time interval between start-stop timing signals. The reference points for the time measurement are the leading edge of the input signals. Use of start-stop type inputs with proper internal gating demands that a stop signal be preceded by a start signal and thus eliminates the ambiguity as to the relative time relationships inherent in the overlap technique.

A time-to-digital converter is one of the simplest timing instruments to set up and operate. The input signals are

provided direct from discriminators with no critical adjustments of amplitude or width being required. As soon as a stop pulse is received, the TDC begins an internal cycle which digitizes the time measurement automatically. The output is available on command typically less than 100 μ sec after receipt of the start signal.

The time resolution of a TDC depends upon the full-scale time range selected. If a measurement is digitized to 11 bits, it provides a resolution of one part in 2048, or 0.05% of full scale. On a 100 nsec scale this would correspond to 50 psec per count.

Achievement of system timing approaching this type of resolution necessitates monitoring the phototube pulse heights originally generating the start and stop outputs from the discriminators. Currently available analog-to-digital converters (like the LeCroy 2282B) are normally used in critical time of flight systems to measure the PM pulse height, permitting slewing corrections to be made later.

Fast Conversion Long Range Time Interval Meters

Delay line readout for gas proportional chambers, time of flight spectrometers for neutrons and ions, and laser ranging are some of the applications that require time interval measurements over very long ranges with excellent resolution at very high rates.

For example, a delay line readout of a Position Sensitive Detector may require that the TDC measure up to a microsecond full scale with 157 psec resolution and operate at 1 MHz. In addition it must be able to measure the time difference between the START and the STOP independent of which comes first in time.

START before STOP means a positive time difference, STOP before START means a negative time difference. A neutron time-of-flight spectrometer may require over 1 msec range with 1 nsec resolution and the ability to handle multiple STOPS before or after a common START.

To meet these requirements different techniques than those outlined above must be used.

The result of a START/STOP time measurement consists of three components in the 4201/4204 design scheme. A high accuracy 100 MHz free running crystal-controlled oscillator is gated into a counter during START/STOP time interval. It measures the real time component of the time measurement with an accuracy of 10 nsec. The real time counter is incremented when measuring positive times, it is decremented for negative times.

Two other components of a time measurement are the results of START and STOP analog interpolators. These two 200 MHz 6-bit interpolators measure with a resolution of 156.25 psec the time of arrival of START and STOP pulses with respect to the first and last clock pulse sent to the real time counter respectively. The random nature of START/STOP pulses with respect to the internal free running clock pulse and the two interpolators, yield excellent differential linearity for these modules.

The result of a time measurement is a digital word (24 or 32 bits) which is automatically transferred at the end of conversion into a second level buffer to be read out. Extremely fast conversion time in conjunction with first level output data buffering permits the acquisition of up to a million time measurements per second. The first level of buffering decouples the input stream from the data acquisition and derandomizes the input rate.

Another technique for Time Interval Measurement which results in near-zero dead time is illustrated in the LeCroy Model 4208 8-Channel, Wide Range, Real Time TDC.

The 4208 uses a highly stable, crystal controlled 125 MHz clock. There are actually 9 "time" channels (the 8 STOP channels and the one common START) which are started synchronously and use this clock. To achieve a 1 nsec resolution, digital interpolators are used.

There is no analog conversion step even for the interpolators; the digital conversion of the time interval requires only the very short time it takes to subtract each of the 8 STOP's from the common START. Since the subtraction is performed in a full adder, a STOP before START is reported as a negative (2s complement convention) time. Each of the "time" channels is 24 bits wide and therefore the module has a dynamic range of ± 8 msec.

Scalers

A scaler is a special type of pulse counter which is used to accumulate pulses from discriminator and fast logic modules. For purposes of economy, the modern scaler does not have its own integral display (*i.e.*, it is "blind"), but communicates directly with a centralized display and/or computer. The output of the scaler is a parallel binary data word which is presented to the display or permanent data storage device by commands from a control system. Manual commands to the scaler (start, stop, reset, test, etc.) are also generated through the control system.

The input buffering circuit is one of the most important parts of the scaler. It should have characteristics which enable it to accept NIM pulses

at the maximum rate and the minimum width generated by fast logic modules. Equally important, it should not multiple-pulse when driven with wide input signals.

The most useful type of scaler now in general use provides 24 bits of data storage capable of being loaded at a 100 MHz rate. This capacity corresponds to approximately 17 million counts and usually minimizes any need to monitor scaler over-flow.

A binary ripple counter is basically a countdown circuit with a 100 MHz flip-flop preceding a 50 MHz flip-flop, which, in turn, precedes a 25 MHz flip-flop, etc. With LeCroy 12-channel CAMAC scalers, 100 MHz scalers can be purchased at prices even lower than slower commercially available units, such that optimum flexibility can be obtained with one type scaler for both high and low rate applications.

Latching Scalers

It is often desirable to avoid the dead time of data readout in counting applications. To achieve this, latching scalers are now available, providing a fast internal buffering of the data word to allow the input stage to begin counting again prior to readout of its previous contents.

Preset Scalers

To add fast counting channels to a system of inexpensive, low-rate scalers, it can be cost effective and convenient to precede the slow scalers with high-rate preset scalers. A preset scaler accepts inputs at a high rate, yielding a front-panel output only after a user-selected number of counts. Its effect is to thus divide down the actual input rate for presentation to the subsequent slow scaler. In doing so, it also expands the bit capacity of the

slow scaler. Generally, preset scalers present no binary data word of their own. As an example, the LeCroy 4431 preset scaler operates at rates up to 130 MHz and is compatible with the 30 MHz Model 4434 latching scaler.

Analog Measuring Instruments

Unlike discriminators, which simply indicate that an input pulse was larger than some preset level, analog-to-digital converters (ADC's) and sample and hold (S/H) circuits give a quantitative measure of the size of a pulse. In particle physics, the pulse parameter of interest is generally the total charge contained in the pulse, rather than its peak amplitude.

Most particle detectors liberate or collect electrons in direct proportion to the ionization energy deposited by a transiting particle. One method of measuring charge is the use of an integrating amplifier which produces an output voltage proportional to the integrated current. This method may be used in conjunction with a peak-sensing ADC. This approach allows the recording of a single event even if more than one occurred during a given time interval. Moreover, the amplifier generally produces a peak amplitude delayed by an integration time which may reduce the length of cable required to delay the analog signals until a trigger can be formed.

The second and most common approach involves the use of a current integrating (charge) ADC. This device integrates an input current for a duration of time equal to the width of an applied gate signal and performs an analog-to-digital conversion on the resulting charge. In many applications, the detector can be connected directly to the ADC, eliminating the need for the amplifier.

BLOCK DIAGRAM: ANALOG-TO-DIGITAL CONVERTER

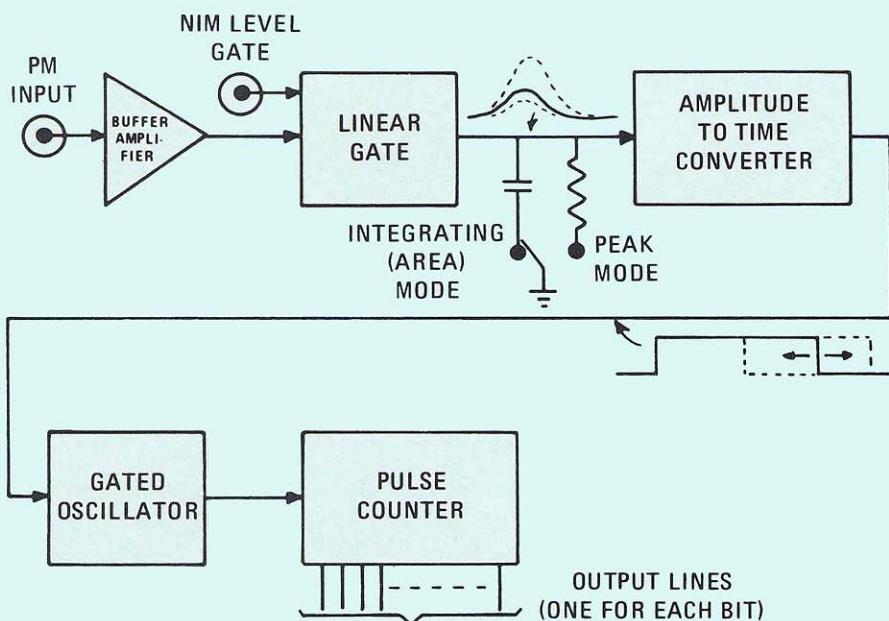


Figure 21

Charge ADC sensitivity may be expressed either in pC or volt-nanoseconds (V-nsec). One V-nsec, in a $50\ \Omega$ system, equals 20 pC. ($Q = V \cdot \Delta t / R$). For compatibility with present high-speed detectors, ADC full-scale inputs are usually in the neighborhood of 1000 pC.

The history of high energy physics ADC's has been an evolution from the single channel 6-bit ADC introduced by LeCroy in 1964 at more than \$900/channel to the present Model 1882N, offering 96 ADC's of 12-bit dynamic range, priced at more than a factor of 25 less per channel.

A block diagram of a typical ADC is shown.

Of primary significance to an ADC's use in high energy physics experiments is the inclusion of the high-speed linear gate which can be opened and closed in a few nanoseconds. This permits the selection in time of the pulses to be analyzed. An ideal linear gate completely blocks all inputs while it is closed, opens without introduction of transients into the signal path, and

when open, passes all inputs without distortion. The linear gate circuits used in modern ADC designs closely approximate this ideal to the precision of the ADC. Limitations generally exist regarding the minimum and maximum duration of gating an ADC.

The conversion technique employed in most commercial ADC's for particle physics is one variation or another of the so-called "Wilkinson rundown" technique. The charge delivered to an integrating capacitor from the line gate is discharged at a constant rate. During the time this rundown is taking place, pulses from an oscillator are gated into a scaler resulting in a final count proportional to the charge originally stored by the capacitor. This technique yields excellent differential linearity with simple circuitry.

Another technique frequently employed involves parallel sample-and-hold circuits for all channels followed by an analog multiplexer to a single ADC. This technique has not been adopted by LeCroy because the high perfor-

mance sample-and-hold circuits offer no price advantage or practical simplification over complete ADC monolithics. Another significant reason is the difficulty of maintaining stable stored voltage levels for long periods of time in experimental environments. Practical constraints which are avoided by separate ADC's include cross talk caused by analog memory in the multiplexer sensitivity and RFI caused by analog busing.

A third technique is one adopted by LeCroy in its 1880 Series ADC's. It parallels the concept of a sample-and-hold technique in that it utilizes one high-resolution ADC for digitizing many analog channels. However, it is charge that is collected, stored, and multiplexed, and current integration is used rather than a peak sensing. All circuit elements preceding the integration are in a custom quad monolithic circuit (QMUX), permitting an inexpensive, simple, and reliable solution to a classically tough problem.

In many applications it is desirable to interrupt analog-to-digital conversion and reenable for a new conversion. Since Wilkinson type ADC's often take several milliseconds to complete digitization, much dead-time or inefficiency can be saved if unnecessary conversion can be aborted. A fast-clear facility on an ADC permits conversion to be aborted and the ADC's to be reinitialized for the next conversion. The performance of the fast-clear of the 1880 Series ADC's is sufficiently rapid to allow operation even under the demanding rates of modern pulsed intersecting storage rings.

The ADC user desires that the instrument provide adequate precision of measurement under actual experimental conditions of widely varying signal amplitude, rate, and temperature. The ADC para-

meters that bear directly on its adequacy are its amplitude resolution, pedestal stability with time and temperature, linearity, and rate sensitivity.

The resolution of an ADC required in a particular application is closely related to the dynamic range of the input signal. In high energy physics, an absolute accuracy in the neighborhood of 1% is usually adequate and consistent with the amount of information available from the detector. For measurements of 1% accuracy, a resolution of 1% of the smallest signal is required. If the largest signal is 20 times the minimum, the ADC must offer a range of 2000:1 or 11 bits. To allow for channel-to-channel variations in detector gain, an ADC with a cushion factor of two in dynamic range is recommended. For calorimeters collecting data with high energy cascades yet calibrating with single minimum ionizing particles, 12 bits may not be adequate.

One method of extending the dynamic range of an ADC involves tailoring a non-linear response to the application. While this approach does extend the dynamic range, it increases the complexity of the circuitry and requires careful calibration. The most serious drawback of non-linear circuits is that they are prone to temperature instability.

A newer method recently adopted for incorporation into the new QMUX monolithic for LeCroy's Series 1880 involves the use of two storage capacitors for each ADC channel. The input signal is split three ways, in an 8:1:1 ratio. The capacitor receiving the 80% signal is normally tied to the integrating ADC and is monitored with a comparator. When the comparator threshold is exceeded, the ADC is switched to the 10% capacitor, which is then used for the measure-

ment. In this way, a dynamic range of 15 bits is achieved. (The remaining 10% signal is used for summing purposes in trigger logic.)

Image Chamber Analyzers

High-performance multi-channel Image Chamber Analyzers which employ the FASTBUS standard are designed to record the amplitude and time evolution of fast analog signals from imaging detectors such as Jet Chambers, Time Projection Chambers, HPC Calorimeters or Ring Imaging Cherenkov detectors. They employ a dual analog shift register — a high-accuracy, fast charge coupled device (CCD).

The Analyzer samples at a software-selectable fixed rate. Each time a new sample is recorded, the oldest one is discarded. In this way, a fixed analog record length is maintained. When a Common Stop Strobe is received, acquisition is terminated and data conversion is begun. Analog data are converted to digital and loaded into memory for FASTBUS readout as described below.

During data conversion, all data from all channels are loaded into memory within the ICA modules. As data are converted, the location of regions of interest are loaded into a Hit Table. For fast readout, this list can be read by the FASTBUS Master and used to address only those regions.

Quasidifferential Inputs

When signals for a charge (current integrating) ADC are transmitted over a long distance on 50Ω coaxial cable, it is possible for errors to be introduced in the analog-to-digital conversion result due to voltage offsets between the signal source reference and the ADC input reference.

For long lengths (even moderate lengths of some cheaper varieties) of coaxial cable, the resistance from one end of the outer shielding to the other end may not be negligible. Voltages may be induced across such shielding from a number of sources (coupling from line-frequency transformers for instance). Equally common, AC power distribution may result in a different "ground" reference for the signal source circuitry than the "ground" reference for the charge ADC. In either case, depending upon the resistance of the cable shielding, voltage differences may be developed across the length of the cable.

If the output impedance of the signal source is not large (for the case of a 50Ω ADC input impedance) a significant error current may be induced in the cable's center conductor by the voltage difference described above.

$$I_{\text{error}} = V/(Z_{\text{out}} + 50\Omega)$$

Assuming the error current to vary slowly compared to the ADC integration time (gate width),

$$Q_{\text{error}} = I_{\text{error}} T_{\text{gate}} = \\ VT_{\text{gate}}/(Z_{\text{out}} + 50\Omega)$$

Thus, depending on the voltage difference, output impedance and gate width, one may or may not have a significant charge error.

Generally, AC coupling (high DC impedance), narrow gates or careful control of offset voltages have served as solutions to this problem in the past. However, in light of the "rate" problems introduced by AC coupling and with the advent of charge sensing DC-coupled ADC's that are stable at wide gates, the need for an easy way of coping with this "noise" problem is evident. Quasi-differential inputs fill this need.

Basically, quasi-differential denotes an input that is not differential in the sense that the input signal is of the type usually transmitted on coaxial cable (single-ended), but the input displays common-mode rejection properties usually attributable to fully differential inputs.

By allowing circuit elements outside the ADC to determine the input signal "ground" reference, the quasi-differential input affords a large amount of immunity to the effects described above. There are limitations to the common-mode performance of the ADC in this configuration, but common-mode rejection ratios (CMRR) of better than 500:1, at 1 kHz, 200 mV are easily obtained.

Dynamic Range

Of some great import, the dynamic range of modern ADC's is a common item of discussion, especially as the number of "bits" available is constantly increasing.

Often the argument is made that non-zero offsets (pedestals) in ADC have an effect on the effective dynamic range of the ADC. This is true. However, in many cases the reduction in dynamic range due to non-zero pedestal is misjudged.

Consider the case of an n-bit ADC, capable at best of producing digital outputs ranging from 0 to $2^n - 1$ (in all 2^n possibilities). If for this ADC there is a "full scale" or maximum digitized input (A) such that one graduation (or count) corresponds to $A/2^n - 1$, then the dynamic range is said to be $A:A/(2^n - 1)$ or $2^n - 1:1$ which is another way of characterizing the full detectable range of the input variable compared to the smallest detectable unit of the input variable.

Since there is nothing special (with regard to ADC's) about the digital number 0, a

constant offset in the conversion will result, that is constant, with equal effect being manifest as a reduction in the full scale conversion value. Therefore if P represents a constant pedestal value, the dynamic range as specified before is modified to $(2^n - 1 - P): 1$.

Note that for the case of the 1882N, which exhibits for 1 msec gates a pedestal of about 250 counts, the nominal 12-bit dynamic range of 4095:1 would be reduced to 3845:1 (roughly 6%). Thus even with such a "large" pedestal, essentially 12 bits (certainly much more than 11 bits) of dynamic range is retained. In this particular case even the nuisance of handling non-zero pedestals may be eliminated by employing the pedestal subtraction feature of the 1821 Segment Manager/Interface.

High Voltage

As particle physics experiments have evolved, the number of channels of detectors has continuously grown. As a result, setting, monitoring, and maintaining detector gain stability has become a major task. Computer controlled high voltage helps solve the problem. Adjustment and monitor of high voltage via CAMAC allows automation and provides additional benefits by locating the HV supplies local to the apparatus. This minimizes high voltage cable runs, providing a major cost and labor savings. Additionally, with the extremely high voltages required by delicate wire chambers, shorter cables provide lower capacitance and result in a minimum of stored electrostatic energy. This provides protection against chamber damage from electrical breakdown.

High voltage is used to bias the anode or the cathode of photomultiplier tubes and wire chambers. For modern detectors, fine voltage resolution is

required to establish accurate channel-to-channel gain matching. This has led to programmable supplies where the user provides a digital demand voltage corresponding to an output voltage. The monitor voltage is an accurately determined fraction of the output voltage, used as a measure of the output voltage.

Interchangeability of high voltage channels is assured by close channel-to-channel matching of output voltages for a given demand voltage. Quantitatively, the accuracy may be specified in terms of both slope and offset accuracies. Production testing of this parameter requires the use of a voltage standard which may be slightly different for various manufacturers. Accuracy of a supply must be trimmed to match the standard at an operating point. Careful design of the unit will assure that the matching specification is met over the specified operating range. The design must allow for non-linearity due to non-ohmic properties of high voltage resistors, voltage drifts with ambient temperature and time as well as position dependence in a multi-channel system.

Digital regulation involves monitoring each output with a highly stable ADC. The result of the measurement is used to verify or modify the digital control value, assuring the output voltage matches the user-supplied demand voltage. This technique yields excellent overall stability and accuracy depending only upon the sense network for monitoring.

Power supplies have internal circuitry to monitor their output voltage and current. Under normal operation as a bias supply, voltage regulation operation is employed. Current monitor serves only as a protection from excessive dissipation. When a fault causes the load resistance to drop, the

supply will current regulate, dropping its output voltage to maintain the output current at the limit value. Certain designs establish a current limit value which depends upon demand voltage and/or temperature. This allows the device to limit its maximum output power and to derate at high temperature.

For photomultiplier applications, the high voltage is used to bias the dynode chain. This bias current must be large compared to the average anode current to assure all dynode voltages are stable. This will minimize gain shifts with counting rate. The disadvantage of high base current is thermal dissipation. A large detector array of high current bases requires careful thermal management to remove the heat. Most bases draw 1 to 2 mA at 1 to 2 kV.

Photomultipliers may operate from either positive or negative voltages, depending upon the application. Positive HV can be applied to the anode with a grounded photocathode, or negative HV can be applied to the photocathode with the anode at ground potential. Use of positive high voltage is the less common way to operate the photomultiplier, because a fraction of the ripple from the supply is applied directly to the PMT anode signal. Positive high voltage is used when the detector geometry makes the photocathode subject to corona, for example, with gas Cerenkov detectors. To achieve sufficiently low ripple with positive HV, it is often necessary to mount additional filter capacitors in the photomultiplier base.

Use of negative HV is most common. Although the sensitive photocathode is run at high voltage, this configuration allows the anode signal to be DC coupled and offers excellent ripple rejection.

Wire chambers require a higher voltage and lower current than do PMT's. The voltage required depends upon the wire spacing and the gas mixture. Because of the very high voltages, it is desirable to use both positive and negative biases for the same chamber. This technique establishes the required potential difference between anode and cathode, yet minimizes the absolute voltage with respect to ground. To allow for this scheme, a wire chamber HV system should be capable of accommodating both polarities in the same chassis.

The electrostatic energy stored in the chamber capacitance and in the cable capacitance is often so large that electrical breakdown can damage a wire chamber. Typically, a chamber has a capacitance of ± 100 pF, but a 30 m high-voltage cable will represent 20 times more. Thus, the energy stored in a long cable is more important.

Because wire chambers are expensive and delicate, they require special protection against damage resulting from arcs. Therefore, a major consideration for a wire chamber HV system is its ability to shut down rapidly in the event of electrical breakdown. A current limit which makes excessive supply current impossible will usually not protect the chamber. An arc will discharge the cable capacitance through the chamber.

Under the influence of the current limit circuit, the cable capacitance will be recharged until the chamber arcs again. In the past, the conventional solution was to rapidly shut off the supply, assuring that only the energy stored in the cable was discharged. The fast trip solution is not effective if the HV cable is longer than a few meters. Typical HV cable has a capacitance of 70 pF/m. Because wire chambers typically

have a capacitance of less than 100 pF, most of the stored energy in a practical system resides in the cable. Since runs of tens to hundreds of meters are typical, the cables typically contain tens of mJ for typical channel voltages, enough to break a wire.

In typical applications, the chamber is isolated from the cable and supply by a large (1 to 10 M Ω) resistor. An arc discharges the chamber extremely rapidly. If the supply trips, the chamber can be recharged many times by the charge in the cable. To avoid this damage mechanism, a crowbar, like that of the LeCroy Series VII (Model HV4032A7) supplies is required. Upon sensing a fault, the supply shuts down and then connects its output to ground. This must be done within several chamber time constants to prevent subsequent arcs. For typical applications, $R = 10$ M Ω , $C = 50$ pF, and $RC = 500 \mu\text{sec}$ a crowbar within ~ 1 msec is required.

Wire Chamber Electronics

Wire chamber detectors, like scintillation counters, and in contrast to spark chambers, are completely untriggered in operation. An array of chamber wires performs the same basic function as an array of scintillation counters with each wire being analogous to a single counter. Wire chamber signals require the same basic treatment as photomultiplier signals, but differences in instrumentation requirements arise because of the much larger number of detectors, the smaller amplitude of the signals, and the poorer time resolution. The large number of wires in a typical system places restrictions on size, power, dissipation, and cost. The small amplitude of the individual wire signals requires substantial amplification before amplitude

discrimination and other operations. The relaxed time requirements allow the use of slower, lower power, less expensive circuitry than that for PM/plastic scintillator systems. Custom monolithic hybrid circuit technology is the technique best suited to these requirements. It provides the needed small physical size, high reliability, and is adaptable to uniform high volume production.

Proportional Chamber Circuits

All proportional chamber systems commonly used in event-oriented experiments are composed of:

- 1) Amplifier/Discriminator front ends capable of low thresholds (e.g. 1 mV, 2 μ A);
- 2) Delays, either active or passive; typically, 200-600 nsec;
- 3) Latch circuitry with approximately 10 nsec resolution;
- 4) Readout, usually via CAMAC.

The input threshold of proportional chamber discriminators should be low enough to give very high (99%) efficiency, yet a good signal-to-noise ratio, over a reasonable range of chamber operating voltages. The sensitivity required depends upon chamber size, wire diameter, and the gas mixture. LeCroy offers 2 μ A threshold on its TRA402/MVL407 Quad units. Inputs are differential to provide common mode rejection of AC pickup.

The combination of very low input threshold, wide dynamic range of input signals, and the small size and close physical proximity of the discriminator circuits can lead to severe cross-talk problems. Cross talk between adjacent channels is minimized by careful optimization of layout, internal bypassing, and ground separations. Similar attention must be paid

to the connection of electronics to the chamber if low cross talk is to be maintained in the operating system. Almost all difficulties experienced by users are caused by improper layout, grounding, bypassing, and shielding problems.

In operation, the discriminators fire independently in response to signals above threshold. This includes valid events, background, and noise. External trigger definition logic, operating from scintillation counters or prompt outputs of the proportional chamber system itself, identifies event patterns. This selection process eliminates the majority of unwanted events. The delay time of a cable, monostable, or LeCroy's deadtimeless "Ripplethru" delay monolithic is chosen to cover the propagation time of the logic system. The event trigger gates the latching circuits, which store the condition of the wires for subsequent readout. After each event, the latches are read out and reset.

The inherent time resolution of an MWPC is determined by the time required for the ionization to drift to the sense wire. This time dispersion is proportional to wire spacing, being typically ± 15 to ± 30 nsec. Thus, the time slewing of the discriminator, the channel-to-channel variations of the delay element, and the coincidence resolving times may be an order of magnitude greater than those characteristic of scintillation counters.

Two MWPC readout schemes are commonly used. One system employs chamber-mounted amplifier/discriminators with remote latches and readout. The LeCroy Model 2731A is a typical latch circuit. The monolithic MVL407 amplifier/discriminator, 2735A or 2735B 16-channel chamber cards may be used at the MWPC. The cable between the

latch and the chamber card serves as all or part of the delay. Such a system offers the greatest flexibility because the latched data from all chambers are in one location.

The other commonly used system employs chamber-mounted electronics with a serial readout daisy-chain. Such a system typically employs an active delay to account for the trigger logic propagation delay plus the round-trip cable delay from the experimental apparatus to the logic. However, with the electronics relatively inaccessible, maintenance can be a serious difficulty. In addition, serial encoding and data transfer is risky with a large number of data cable connections. Typical MWPC readout schemes include the storage of "hit" wire addresses, or "cluster-compacted" data. In the latter scheme, only the central address of a hit "cluster" of wires is stored along with the width of the cluster.

Recent systems, such as LeCroy's PCOS III, are conducive to prompt triggers as well as subsequent-level triggers. "ECLport" outputs compatibly feed a variety of modern trigger processors and track finding systems.

The use of this type of system eliminates long and costly delay cables which often represent 50% of the electronics cost in some separated latch configurations.

Drift Chambers

Drift chambers record particle position by measuring the time for ionization created along a particle track to propagate across an electric field to a signal wire. Chamber wires are typically several centimeters apart and drift times are on the order of 250 nsec/cm, or 250-2000 nsec. A time reference signal (common start or stop) based upon the trigger

logic or upon the interaction time of a colliding beam accelerator is required.

Wire chamber signals have slower risetimes than do scintillation counters. In order to minimize the time inaccuracy caused by this, low input impedance (several hundred ohms) amplifiers/discriminators are required. Since the signals are charge pulses, low input impedance dictates that the pulse height will be rather small. This requires high sensitivity to ensure that the signals are well above threshold. LeCroy offers 2 μ A threshold in its HIL401 quad chamber discriminator. Also contributing is the resolution of the time digitizer. Analog and digital devices with a synchronous clock have a resolution of $\pm 1/2$ LSB, whereas those with asynchronous clocks have a resolution of ± 1 LSB.

The dimensions of a drift chamber are typically on the order of 1-2 meters. Thus, thermal expansion of the frame can affect the resolution. Also, the temperature stability of a TDC is important. For analog time stretching and for digital vernier schemes, the vernier stability must be considered.

Chamber linearity is limited by the constancy of both the magnitude and direction of the electric field vector throughout the drift volume. Although the drift velocity is rather independent of the voltage gradient, some nonlinearity is introduced by poor field-shaping geometry. In addition, magnetic fields cause severe deviations from linearity for wide wire spacing.

To achieve the best time resolution, the signal wires should be connected to a low-threshold amplifier/discriminator. Wherever possible, the amplifier/discriminator should be mounted directly on the chamber to eliminate the rise-time degradation and the pick-

up that would otherwise be introduced by passing these low-level signals down a transmission line. In a circuit such as the LeCroy MVL407 Chamber Discriminator, input signals are differentially received to reduce noise and DC offsets, while their compact monolithic size makes them ideal for on-chamber mounting. Since the amplifier and discriminators are remote from the timing circuits, some provisions must be made for driving long cables. Differential ECL (Emitter-Coupled Logic) outputs have proved sufficient for driving substantial lengths of inexpensive twisted-pair with minimal cross talk, attenuation, and risetime distortion.

Readout Electronics

LeCroy Drift Chamber Systems employ both analog and digital readout schemes, covering both simple-bit and multi-bit applications, respectively. In the former scheme, a custom monolithic circuit provides all the circuitry necessary to measure drift times and automatically calibrate each channel of the system. A 9-bit-plus overflow TDC utilizing an analog time stretcher and a digital counter is employed. An analog ramp is created by the difference between start and stop inputs. An internal oscillator clocks into the counter for a period dependent upon the slope of the ramp, which is proportional to the start-stop time difference. Both Common Start and Common Stop modes are possible with this technique. Of special relevance is a built in AUTO-TRIM feature, which calibrates the offset and slope of the analog ramp for each channel. This eliminates subsequent corrections usually found unacceptable in an analog technique.

The digital scheme utilized by LeCroy is incorporated into the new Series 1870. It consists of amplifier and dis-

criminator monolithics feeding a high-speed shift register. The "pipeline" clocks at 250 MHz, and two shift registers are used out of phase with each other to achieve an equivalent of 500 MHz operation. This results in a quantum resolution of 2 nsec at its best, covering a range of about 1 μ sec. Slower clock speeds allow measurement over longer drift spaces but correspondingly affect the per-count resolution. Since this scheme records the complete condition of the wire over the whole interval, it is conducive to use in multiple-hit conditions.

Time Projection Chamber Readout

Time projection chamber electronics record the history of each chamber wire within the entire drift length of the chamber. In contrast to digital multihit readout schemes, TPC readout involves the actual analog measurement of the wire condition. Frequent samples over the drift time allow recreating the signal shape on each wire. Thus, total energy as well as position can be determined, making the TPC useful for mass as well as spatial measurements.

Two techniques are generally considered for TPC readout. The first utilizes a charge-coupled device (CCD) for each wire. One or more CCD outputs are digitized by a subsequent ADC. Classical problems with CCD's, such as poor efficiency of charge transfer at high rates, pattern noise inaccuracies caused by the varying CCD geometries, serious temperature dependence of the CCD's, and high output offsets have in the past combined with other factors to make CCD's difficult to use in large systems. Nonetheless, the CCD method is less expensive in hardware cost than other methods. For the FASTBUS System 1800, LeCroy has developed a custom CCD of uniform geometry to

eliminate the need for cell-to-cell corrections. It eliminates the output offset problem, is designed to operate at 50 MHz with 9-bit accuracy, and may be driven with low power clock driver circuits.

The other standard method is simpler to design but very costly to implement. It involves the use of flash converters and large memories. With very high sampling rates, statistics and centroid-determination techniques permit equivalent measurements with low resolution analog digitization. Nevertheless, even low resolution flash ADC's are still quite expensive for the large system, and the high power dissipation of this technique limits one to a low module density and consequently high overhead cost. To handle the fast measurement rate, local memories are often used with on-board microprocessors to reduce the data before transfer to the system processor. This overhead is best amortized over as large a number of channels as possible.

X-Ray and Neutron Physics

X-Ray and neutron detection systems have traditionally used either photographic films or scanning counters. Both techniques require long exposure times and manual intervention for data acquisition, control and analysis.

Recent developments in Position Sensitive Detectors (PSD's) have advanced this technique as a better solution for the detection of scattered X-Rays and neutrons. Since PSD's may detect X-Rays and neutrons over their large active surfaces with high efficiency and negligible noise levels, exposure times are considerably reduced. Advantage can be taken of the enormous experience gained with proportional counters in the Medical,

Nuclear, and Elementary Particle Physics fields to automate the data acquisition and introduce on-line and subsequent off-line analysis.

Applications in the fields of Fusion research, Atomic and Nuclear Physics, X-Ray and VUV Synchrotron Radiation research including Crystallography, Chromatography, Metallurgy, Medical research and Biology are found or can be envisioned.

Position Sensitive Detector Electronics for X-Ray and Neutron Physics

There are many types of position sensitive detectors with several readout methods. Most detectors may be read out or have their data processed into digital form with instruments from LeCroy.

Gas detectors consist of gas proportional tube or chamber with two electrodes sealed in a gas-filled pressurized cell. The anode, held at positive high voltage, is either a thin metal wire as in the linear detector, or a plane of wires for the two-dimensional detector. An ionizing event that penetrates the window liberates electric charges which are amplified by the electric field of the anode.

Rise Time Encoding:

By using an anode with a high resistance per unit length and appropriate electronics, the difference between the signals' rise time, as they arrive at the two ends of the anode, can be encoded into a time interval. This time interval may be accurately measured by one of the Series 4200 Time Digitizers.

Charge Division Encoding:

The position of the ionization may also be encoded by measuring the charge with LeCroy ADC's arriving at the two ends of the anode. This last method is usually less ac-

curate and is only useful in very large detectors.

Delay Line Readout:

The cathode of a PSD can also have a geometry permitting the localization of the ionizing event. It consists of a series of parallel strips or wires, each connected to a common delay line. Electric pulses induced on the cathode are picked up by the delay line and propagate in both directions, finally reaching the ends at different times. The time difference is correlated to the position of the initial ionization and can be encoded with the Series 4200 Time Interval Meters.

Wire-by-Wire Readout:

For even higher data acquisition rates (above 0.5 MHz) the individual wires or strips of the cathode may be read out by LeCroy Amplifier/Discriminator circuits and the digital signals sent to counters or LeCroy Latching Scalers. The PSD can function in a very high flux environments of over 100 million particles per second, with the only reservation being that individual wire or strip rates are limited to 10 MHz.

Fiberoptic Systems Introduction

Fiberoptic technology addresses limitations inherent to conventional coaxial and twisted-pair-cabling data transmission systems as instrumentation bandwidths have increased and user applications have changed. Fiberoptics offers increased bandwidths for higher speed transmission, decreased losses for longer distances and total immunity from electromagnetic interference (EMI). Two decades' experience in high-speed electronics has enabled LeCroy to develop a fiberoptic product line to satisfy even the most demanding applications for data communication, video transmission, and analog signal processing.

Advantages

Consider the following advantages for applications in which analog or digital information is transmitted at high speed over long distances and/or through an EMI environment.

- Fiber optics is functionally superior to conventional coaxial or twisted-pair cabling in wide bandwidth/low loss applications
- Glass fibers offer total immunity from noise pickup and common mode voltage problems at a lower cost than coax cable shielding techniques
- When cable weight or volume is a prime consideration, no alternative exists
- Link (transmitter/receiver pair) developments utilize the high bandwidth fibers presently available:

Digital Links — Data rates of 100 megabits/sec — NRZ (no return to zero), and Analog Links — Data rates of 250 MHz per second

LeCroy's designs are optimized to offer high performance in conjunction with readily available low-loss fiber optic cables (i.e. 8 dB typical for 2 km, terminated lengths) at a fraction of the cost of systems using lasers or long wavelength LED's. A continuing decrease in system cost is anticipated as this relatively new technology expands, resulting in high-volume requirements.

Design Criteria

LeCroy digital links have an Automatic Threshold Control (ATC) which automatically adjusts the receiver threshold for optimum performance at any input signal level. This means there are no adjustments necessary to compensate for different optical power levels due to different lengths of fiber or changes in the optical path.

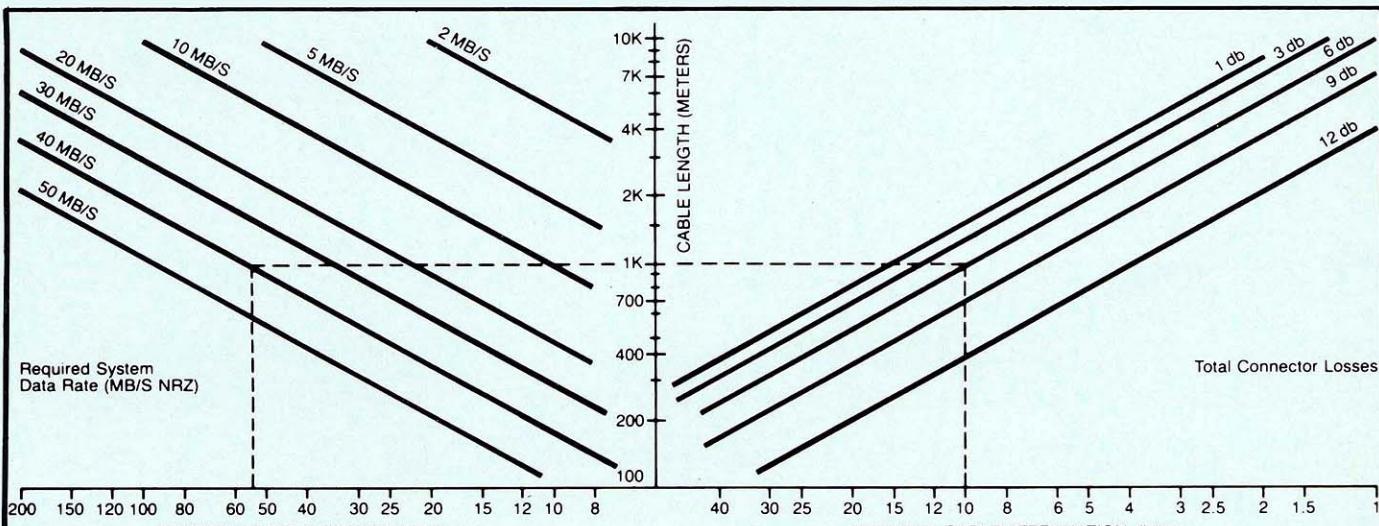
Likewise, the LeCroy analog links have an Automatic Gain Control (AGC) to maintain the same system gain regardless

of the strength of the input optical signal. The only effect of a reduction in signal strength is to reduce the system signal to noise ratio.

LeCroy offers links compatible with both the popular 50 μm and 200 μm fiber core sizes. The 50 μm fiber offers the advantage of lower fiber cost and larger bandwidths than are possible with the larger diameter fibers. The 200 μm fiber offers the advantage of coupling larger amounts of optical power emitted by a LED, thus allowing operation in systems with high losses due to optical couplings, splitters, etc.

LeCroy makes it easy to calculate your optical power budget. We provide the useful output power, which is the measured optical power at the end of 100 m of fiber. This eliminates the guesswork of calculating coupling losses and amount of light that travels through the cladding rather than the core of the fiber.

Model 5310 Link Design Guide



Instructions for use

Draw a horizontal line through the required link length (e.g., 1 km). On left hand side find the point where it intersects the desired system data rate (e.g., 40 MB/S). Read off minimum cable bandwidth (e.g., 55 MHz · km).

On right hand side find the point where it intersects the expected total connector loss (e.g., 6 db). Read off maximum cable attenuation (e.g., 10 db/km). Any cable equalling or bettering these bandwidth and attenuation figures is suitable.

Figure 22

Quick-Reference Chart/Page Guides for Fast Pulse Products

ECLLine-Compatible Trigger Logic Modules

Model	Function	No. of Channels	Front Panel Analog Outputs	Front Panel Digital Outputs	Programmable	Test Features	Transit Times of Front Panel Outputs	Voltages	Page
2323	Dual Gate and Delay Generator	2	No	3 NIM, 1 ECL, 1 TTL	CAMAC	Yes	24 nsec	$\pm 6V, \pm 24V$	129
2365	Programmable Logic Unit	8	1	8	CAMAC	Yes	10 nsec	$\pm 6V$	131
2372	Memory Lookup Unit 64K, 60 nsec throughput	12-16 Programmable Inputs	0	1-16 Programmable	CAMAC	Yes	60 nsec	$\pm 6V, +24V$	135
4415	Programmable Non-Updating Discriminator	16	0	2x16 ECL	CAMAC	Front Panel and CAMAC	13 ± 4 nsec	$\pm 6V, -24V$	199
4416B	Programmable Updating Discriminator	16	0	2x16 ECL	CAMAC	Front Panel and CAMAC	< 14 nsec	$\pm 6V, \pm 24V$	203
4418	Programmable Logic Delay and Fan Out	16	0	3x16 ECL	CAMAC	None	15 nsec plus Programmable	$\pm 6V$	207
4448	Coincidence Register	48	3 Sums		No	None	9 nsec	$\pm 6V$	215
4504	4-Bit Flash ADC	4	0	4x4-Bit and Overflow ECL	CAMAC	None	15 nsec	$\pm 6V, +24V$	217
4508	Programmable Logic Unit	8 Input	0	8 Output	CAMAC	None	21 ± 1 nsec	$\pm 6V$	221
4516	3-Fold Programmable Logic Unit	16	0	16 ECL	CAMAC	Mode check via CAMAC	8 or 11 nsec Depending on Input	$\pm 6V$	225
4532	Majority Logic Unit	32	2	16 ECL (2 by 2 OR's)	No	None	12 nsec Digital 16 nsec for Analog	$\pm 6V, \pm 24$	229
4564	OR Logic Unit	64	0	16 ECL via Rear Panel	via Jumpers	None	12 ± 1 nsec	$\pm 6V$	233
4616	ECL to NIM NIM to ECL Converter	16	0	3x16 NIM 1x16 ECL	No	None	ECL-NIM < 6 nsec ECL-NIM < 10.5 nsec NIM-ECL < 6.5 nsec	-6V	239

N/A Not Applicable

ECLport Data Sources

Model	Description	Output (bits)	Package	Page
1821	FASTBUS SM/I	32	#2 FASTBUS	87
2738	PCOS III Controller	16	#2 CAMAC	161
4300	Fast Encoding and Readout ADC (FERA)	16	#1 CAMAC	187
4301	FERA Controller	16	#1 CAMAC	193
4504	Flash ADC	16	#1 CAMAC	217

ECLLine Data Handlers

Model	Description	Capacity	Access (nsec)	Page
2372	MLU	8 KB	60	135
2375	STACK	2 KB	20	139
4508	PLU/MLU	2 x 256	22	221

See PCOS III, FERA

ECLbus Data Destinations- Memory

Model	Memory Size (KB)	Word Width	Ports	Package	Special Features	Page
1891	256	16 or 32	2	#1 FASTBUS		97
4302	32	16	3	#1 CAMAC	Multiple events accessible by Model 4800	195

Amplifiers and Preamplifiers

Model	612A	612AM	6102	8100	HQV810	VV100B	VV100BTB	TRA402	TRA1000 (2)	TRA403
No. of Channels	12	6	2	2	8	1	1	4	1	4
Gain	10 fixed	2.5-40 variable	0.2-10	0.2-100	0.5V/pC	10 fixed	10 fixed	25 mV/ μ A	2.7 mV/ μ A to 300 mV/ μ A or up to 0.5 V/pC (4)	330 mV/ μ A
Bandwidth (MHz)	175	140	100	1	14	175	175	100	15	60
RMS Input Noise	<50 μ V	<50 μ V	<50 μ V	100 μ V	70aC	<50 μ V	<50 μ V	0.1 μ A	370 μ V	<400 aC with 30 nsec gate
Connector/Size	LEMO/#1	LEMO/#1	BNC/#1	Differential LEMO/#1	24-pin DIP	18-pin DIP	LEMO	18-pin DIP	16-pin DIP	20-pin DIP or 18-pin chip carrier
Package	NIM	NIM	CAMAC	CAMAC	Hybrid	Hybrid	(5)	Monolithic	Monolithic	Monolithic
Required Voltages (volts)	+6, +12, -24 and -12 or -6	+6, +12, -24 and -12 or -6	\pm 6, \pm 24	\pm 6, \pm 24	+6V, -3V	\pm 6 or +6 -12	\pm 6 or +6, -12	+5.0 -2.5	+12 (3)	+3 -1.5
Input Coupling	DC	DC	DC	DC	AC	DC	DC	(6)	DC	DC (6)
Input Impedance (ohms)	50	50	50	1M Ω		>1K	50	75 \pm 25	0.4	300
Risetime (nsec)	<2.0	<3.0	<2.0	350	30	<2.0	<2	4.0	25	7
In/Out Delay (nsec)	4.0	5.5	4.0	—		1.5	<2	3-7	22	15
Maximum Output Amplitude (volts)	(1)	(1)	0.5V into 50 Ω	\pm 10V (HiZ) \pm 2.5V (50 Ω)	6	(1)	(1)	1.5	1V into 50 Ω	\pm 1 V with external pull down resistors
Integral Linearity (%)	0.1	0.2	0.1	\pm 0.05	0.1	0.1	0.1	Usage Dependent	<0.5 typical into 50 Ω	1.0
Page	57	59	357	361	271	335	338	317	327	323

(1) +0.25 V to -2.0 V with -6 V Supply, or +0.25 V to -5.0 V with -12 V Supply

(2) With $R_F = 2.7$ K Ω (i.e. gain configuration of 2.7 mV/ μ A)

(3) Power supplies depend on gain configuration chosen. Standard = +12 V

(4) i mode and q mode gains are determined by external feedback elements

(5) 3" x 3" x 1.5" box

(6) Must be externally AC-coupled

Fan-Ins and Fan-Outs

Model	Mfg. Type	Linear/Logic	No. of Channels	No. of Inputs/Channel	No. of Outputs/Channel	Coupling	Input Type	Output Type	Rise/Fall Times (nsec)	In/Out Delay (nsec)	Required Supply Voltages	Page	
428F	NIM #1	Linear	4	4	4	DC	Bipolar	+0.1 to -2.0 V	2.5/2.5	<6	\pm 12, \pm 24	49	
430	NIM #1	Logic	8	1	4	DC	NIM	NIM	2.5/2.5	<2.5	\pm 6	53	
429A	NIM #1	Logic	4	4	4			NIM/TTL	NIM	2.5/2.5	6.5	\pm 6, \pm 12	51
4418	CAMAC #1	Logic	16	1	3		ECL	ECL	2.5/2.5	Variable up to 128	\pm 6, \pm 24	207	

Scalers

Model	2551	3521A	4431	4434	4604
Function	Counting	Multichannel Scaling	Preset Scaling	Latching Scaler	Counting, Timing, Display
# Inputs	12	1	8	32	4
Rate (MHz)	100	100	140	20	125
Capacity	24 bits	24 bits	N/A	24 bits	8 decimal digits
Size (CAMAC)	#1	#1	#1	#1	#2 NIM
Input Levels	NIM	NIM/TTL	ECL	ECL/TTL	NIM/TTL/ECL/analog
Int. Buffer	No	Yes	No	Yes	No
External Memory	No	Yes (8201)	N/A	Yes	No
Special Features	—	Double Buffer input; <5 nsec deadtime; 1 μsec dwell	Remote, 4-bit programming; (divide by 2, 4, 8, 16)	Output port for independent bus deadtime for raster scan display unit	RS232 port pushbutton control NIM/TTL, or ECL signals
Page	145	469	209	211	235

Analog-to-Digital Converters

Model	No. Ch.	No. Bits	Size	Q or V	Full Scale	Max. Resolution	Gate Width	Conversion Time	Fast Clear Time	Comments	Page
2249A	12	10	#1	Q	-256 pC	-0.25 pC	10-200 nsec	55 μsec	2 μsec		109
2249SG	12	10	#2	Q	-256 pC	-0.25 pC	10-200 nsec	55 μsec	2 μsec		111
2249W	12	11	#1	Q	-512 pC	-0.25 pC	30-10000 nsec	110 μsec	2 μsec		113
2250L	12	9	#1	Q	-248 pC	-0.5 pC	10-200 nsec	10 μsec	1 μsec	32 deep Buffer	115
2259B	12	11	#1	V	-2 V	-1 mV	100-5000 nsec	110 μsec	2 μsec	Upgrade of Model 2259A	117
1882 N/P	96	12	#1F*2	Q	400 pC	0.1 pC	50-2000 nsec	750 μsec	0.6 μsec	Readout via FASTBUS	95
1885 N/P	96	15	#1F*2	Q	1600 pC	0.05 pC	50-2000 nsec	750 μsec	0.6 μsec	Readout via FASTBUS	95
2282B	48	12	#1	Q	-1000 pC	-0.25 pC	50-10000 nsec	1 msec	<2 μsec	Readout via LeCroy Processor in dedicated CAMAC crate	122
(offers 1% gain calibration, wired, tested summing outputs, and quasi-differential inputs)											
2285A	24	12	#1	Q	-400 pC	-0.10 pC	50-1500 nsec	0.65 msec	<2 μsec	Readout via LeCroy Processor in dedicated CAMAC crate	122
3511	1	8-13	#1	V	±8 V	1 mV	N/A	5 μsec	N/A	Spectroscopy ADC	459
3512	1	13	#2	V	±8 V	1 mV	N/A	5 μsec	N/A FIFO	1000-deep	463
4300	16	9-11	#1	Q	-256 pC -256 pC -480 pC	-0.5 pC -0.25 pC -0.23 pC	50-2000 nsec	2.8 μsec 4.8 μsec 8.5 μsec	<2 μsec	Readout via Dataway or Front-Panel ECL Port (100 nsec/word), Pedestal Memory, Zero Suppressed Read Option	187
4504	4	4	#1	V	-2.5 V +2.5 V	—	N/A	15 nsec	N/A	Readout via Dataway or Front-Panel ECL Port	217
LG8252 (1)	32	12	#1	V	10 V	2.5 mV	N/A	2 msec all channels (1)	N/A		383
LG8213 (1)	16	12	#1	V	10 V	2.5 mV	N/A	1 msec all channels (1)	N/A		383

(1) Offers continuous scan or triggered scan modes. (2) FASTBUS

Gate and Delay Generators

Model	Channels	Operation		Range	Resolution	Jitter	Standard Package	Start Input	Output	Output Width	Manual Readout	Dead-time	Insertion Delay	Page
		Manual	Programmable											
222	2	Yes	No	100 nsec-11 sec	0.1% of full scale	<0.2% of setting	NIM/#1	NIM/TTL	NIM/TTL	10 nsec	Test Point	0	14 nsec	43
2323	2	Yes	Yes	50 nsec-10 sec	0.1% of full scale	<0.2% of setting	CAMAC/#2	NIM/TTL/ECL/analog	NIM, 35 V pulse, ECL	10, ..., 300 nsec	LED display	0	24 nsec	129
4222	4/2*	No	Yes	170 nsec-16.7 msec	1 nsec	150 psec**	CAMAC/#1	NIM	NIM, 5 V pulse	5 nsec - 16.7 nsec	CAMAC only		170 nsec	173

*The 4222 may be used as 4 channels of Delay or 2 channels of Gate Generator

**Up to 1 msec delay, 300 psec for longer delays.

CAMAC Time Interval Meters (Time-To-Digital Converters)

Model	Channels	Input Levels	No. of Bits	Size	Time Ranges	Resolution	Time Range	Conversion Time	Programmable	Test Features	Fast Clear	Comments	Page
1878/79	96	ECL	1878-8 1879-9	#1 FASTBUS + Phase Latch	8	4-63 nsec 2-31 nsec	0-1000 to 0-6300	25-400 nsec	FASTBUS	Yes	0 nsec	Multihit	89
2228A	8	NIM	11	#1	3	50 psec 100 psec 250 psec	0-100 nsec 0-200 nsec 0-500 nsec	100 μsec	No	Yes	1.4 μsec		105
2229	8	ECL	11	#1	3	50 psec 100 psec 250 psec	0-100 nsec 0-200 nsec 0-500 nsec	100 μsec	No	Yes	1.4 μsec		107
4201	1	-1.5 to 1.5 V	16	#1	15	156.2 psec to 2.56 μsec	-5.12 to 5.12 μsec -655 to 655 μsec	<0.5 μsec	Yes	Yes	<500 nsec	Programmable Offset	165
4204	1 (16)*	-1.5 to 1.5 V (ECL)*	24	#2	15	156.2 psec to 2.56 μsec	-1.31 to 1.31 μsec -167.77 to 167.77 msec	<0.5 μsec	Yes	Yes	<500 nsec	Programmable offset. Router may be driven by multisource input. Front-Panel Port for memory (3588)	167
4208	8	-1.5 to 1.5 V	24	#1	1	1 nsec	-8.3 to 8.3 msec	None	No	No	50 nsec	May be set to multi-hit via internal straps	171
4291B	32	ECL	9	#1	8	1-4 nsec	512-2408 nsec	35 μsec	Board Pots	Yes	>300 nsec	Autotrim®	179

*The 4204 accepts up to 16 channels of multisource ECL input and performs the time interval measurement on the first hit. Veto on double hit may be programmed.

Discriminators

Model No.	No. of Channels	Updating	Threshold (mV)	Output Width (nsec)	In/Out Delay (nsec)	No. of Outputs [] []	Veto	Max. Rate (MHz)	Summing Output	Remote Control	Burst Guard	HIZ Bridged Input Option	Page
MVL407	4	No	10 to 500	TOT ⁽³⁾	2	1 Dif ECL	No	100	No	No	No	No	301
623B	8	Yes	-30 to -1000	6-150	11.0	3 0	Yes	100	No	No	No	Yes ⁽¹⁾	63
821	4	Yes	-30 to -1000	5-1000	11.0	5 1	Yes	100	No	No	Yes	Yes ⁽¹⁾	69
2735A 2735B	16 16	No No	2 to 20 μ A 2 to 20 μ A	TOT ⁽³⁾ TOT ⁽³⁾	<20 nsec @ 2 x threshold <12 nsec @ 20 x threshold	35	1 Dif ECL	No No	20 10	No No	Yes Yes	No No	157 159
4415	16	No	-30 to -60 (differential)	10-300	13	2 Dif ECL	Yes	50	No	Yes	No	No	199
4416B	16	No	-15 to -1000	4-40 (100) ⁽¹⁾	<14	2 Dif ECL	Yes	150	No	Yes	Yes	No	203
4608B	8	Yes	-30 to -1000	4-40 ⁽²⁾	<12.0	3 1	Yes	200	No	No	Yes	No	238
HIL 401 (for MWPC's)	4	No	2 to 20 μ A	TOT ⁽³⁾	<20 nsec @ 2 x threshold <12 nsec @ 20 x threshold	1 Dif ECL	No	10	No	Yes	No	No	267
HIL 440 (for Drift Chambers)	4	No	2 to 20 μ A	TOT ⁽³⁾	<16 nsec @ 2 x threshold <11 nsec @ 20 x threshold	1 Dif ECL	No	20	No	Yes	No	No	269

(1) High-impedance bridged inputs are available at the expense of one normal output.

(2) 100 nsec output duration possible with restriction that input and output pulse width can not be equal.

(3) TOT — Time-Over-Threshold

NIM Coincidence Units

Model No.	No. of Channels	No. of Inputs	Majority	Updating	No. of Outputs [] []	Output Width (nsec)	Veto/Strobe	Max. Rate (MHz)	In/Out Delay (nsec)	Remotely Programmable	Connector Type/Size	Voltagess Required	Page	
622	4	2	No	Yes	5 1	5-1000	Yes	110	9.5	No	Lemo/#1	± 6 ± 12	-24	61
365AL	2	4	Yes	Yes	4 2	4-50	Yes	160	10.0	No	Lemo/#1	± 12 -24	120V AC	45
380A	1	32	Yes	Yes	4 2**	20 and 25-100**	Yes	100, input 30, output	12***	No	Lemo/#1	± 6 ± 24		47
465	3	4	No	Yes	(preset) 2 1 (overlap) 2 0	5-500 (preset) or overlap	Yes	120	13	No	Lemo/#1	± 6 ± 12	-24	55
624	8	2	N/A	N/A	3 0	Mean	No	Determined by delay	Variable see data	No	Lemo/#1	± 6 ± 12	-24	65

* Not applicable

** On Model 380A, both = N and >N outputs present. The >N output is variable as indicated.

*** 12 nsec for >N output; 8 nsec following end of = N condition for = N output.

Fiberoptic Transmitters and Receivers

ANALOG

Model #	Description	System Gain	Optimum Fiber Diameter	Input (Output)	S/N	Electrical Signal	Power Connector	Voltage Required	Package Type	Page
5403AT	60 Hz to 250 MHz Transmitter		50 μm	800 mV p-p		Coax. Pigtail	Card Edge	-12 V	Link (Box)	259
5403AR	60 Hz to 250 MHz Receiver, AGC(1)	0.1	50 μm	(200 mV p-p) ⁽⁵⁾	30 dB	Coax. Pigtail	Card Edge	± 12 V	Link (Box)	259
5413AT	50 Hz to 50 MHz Transmitter		50 μm	2 V p-p		Coax. Pigtail	Card Edge	± 6 V	Link (Box)	261
5413AR	50 Hz to 50 MHz Receiver, AGC(1)	1.0	50 μm	(2 V p-p) ⁽⁵⁾	40 dB	Coax. Pigtail	Card Edge	± 12 V	Link (Box)	261
5612	DC to 1 MHz Transmitter		200 μm	± 0.2 V to ± 100 V		Triaxial Lemo	Battery Charger or ext.	12 V	Stand Alone (Box)	263
5613	DC to 1 MHz Receiver, AGC(1)	0.01 to 5 Programmable	200 μm	(2.5 V p-p) ⁽⁵⁾	54 dB typical	2-Pin Lemo	CAMAC	± 6 V ± 24 V	CAMAC #2	263

DIGITAL

Model #	Description	Rate	Optimum Fiber Diameter	Input (Output)	BER	Electrical Signal	Power Connector	Voltage Required	Package Type	Page
5211	Byte-Serial Optical Link W/Battery Backup	40 Mbit/sec (5 MByte/sec)	50 μm	IEEE 583 Standard	10^{-12}	CAMAC D-Port. (RS422 or TTL) ⁽⁴⁾	CAMAC	± 6 V ± 24 V (110/220 V AC) ⁽⁴⁾	CAMAC #1 (19") ⁽⁴⁾	253
5312AT	Digital Transmitter	DC-100 Mbit/sec NRZ	50 μm ⁽³⁾	TTL		Card Edge	Card Edge	± 5 V	Link (Box)	256
5310AR	Digital Receiver, ATC(2)	DC-100 Mbit/sec NRZ		(TTL)	10^{-12}	Card Edge	Card Edge	± 5 V	Link (Box)	255
5332AT	Digital Transmitter	DC-100 Mbit/sec NRZ	50 μm	ECL		Card Edge	Card Edge	± 5 V	Link (Box)	258
5330AR	Digital Receiver, ATC(2)	DC-100 Mbit/sec NRZ		(ECL)	10^{-12}	Card Edge	Card Edge	± 5 V	Link (Box)	257

(1)AGC: Automatic Gain Control

(2)ATC: Automatic Threshold Control

(3)200 μm option also available (Model 5310AT)

(4)Planned

(5)Into 50 Ω

HOUSINGS

Model #	Description	Page
Series 5600 1403	NIM Modular RF-shielded enclosure (for housing 5312A, 5332A and 5400 Series Links) NIM-Standard BIN and Power Supply (for powering Series 5600 NIM modules above)	255, 257, 259 71

All LeCroy Fiberoptic Products use optical connector Amphenol-type 906. Card Edge Connector is dual 8" x 0.1" spacing LeCroy Part No. 455-660-016 (TEKA 011-08441-290).

Product Guide for High Energy Physics Applications

APPLICATIONS

BITUBE DETECTOR READOUT

Chamber Card: 4400
Controllers: 4750, 4299

CALORIMETRY

Amplifier Components: TRA403, TRA1000,
VV100B, TRA402, HQV810
Amplifier Models: 612A, 612AM
See "Event ADC's"

CHARGE DIVISION CHAMBER READOUT

Amplifier Components: TRA1000, HQV810,
TRA402
See "Event ADC's"

DRIFT CHAMBER CIRCUITRY

Chamber Components: MVL407, TRA402,
TRA403
Chamber Card: 2735A,
High Voltage: HV4032A7, 2415
Time Digitizers: 2228A, 2229, System 4290,
1878, 1879, MLL400

FIRST LEVEL TRIGGER LOGIC

Discriminators: 623B, 821, 4416, 4608
Miscellaneous Logic and Control: 222,
429A, 624, 688AL, 2323, 4222
Coincidence Logic: 365AL, 380A, 465, 622
Matrix Logic: 2365, 2372, 4508
ECLINE Modules: 4414, 4415, 4416B, 4417,
4508, 4418, 4532, 4564, 4516, 4616, 2365

MULTIWIRE PROPORTIONAL CHAMBERS

Chamber Components: MVL407, TRA402,
TRA403
Chamber Card: 2735B,
High Voltage: HV4032A7, 2415
PCOS III: 2731A
Coincidence Register: 4448

STREAMER TUBE READOUT

Chamber Card: 4200
Controller: 4700

TRIGGER PROCESSORS

MWPC Hit Encoder: 2738 (PCOS III)
Logic Modules: 2365, 2372, 2375
Trigger ADC: 4300, FERA

PRODUCT TYPES

DATA ACQUISITION CIRCUITS

See ADC's
TDC's: 2228A, 2229, 4291B, 1878, 1879
Scalers: 2551, 4434, 4604
Latches: 2731A, 4448
Fast Encoding TDC: 4201
High Precision Wide Range TDC: 4208

EVENT ADC's

2249A, 2249W, 2250L, 2259B, 2282B, 2285A,
1882, 1885, 4300, MIQ401, MQT200F

FASTBUS ACCESSORIES

1810, 1801, 1805, 1822

FASTBUS READOUT DEVICES

1821, 1891, 2891, 1821/DEC

FAST CAMAC PROCESSORS CAB (CAMAC Booster): 4800 Series

FAST LINEAR CIRCUITRY

428F, 612A, 612AM
Discriminators: 623B, 821, 4608

HODOSCOPES

Discriminators: See above
High Voltage: 1443, HV4032A1
Latch Module: 4448
Coincidence Logic: See above
See "Event ADC's"

PROGRAMMABLE HIGH VOLTAGE

CAMAC Interface: 2132
Mainframe: 1449, 1449E, HV4032A/M
Plug-In Modules: 1443N/12, 1443NF/12,
1443P/12, 1443PF/12, HV4032A1,
HV4032A7

TDC's

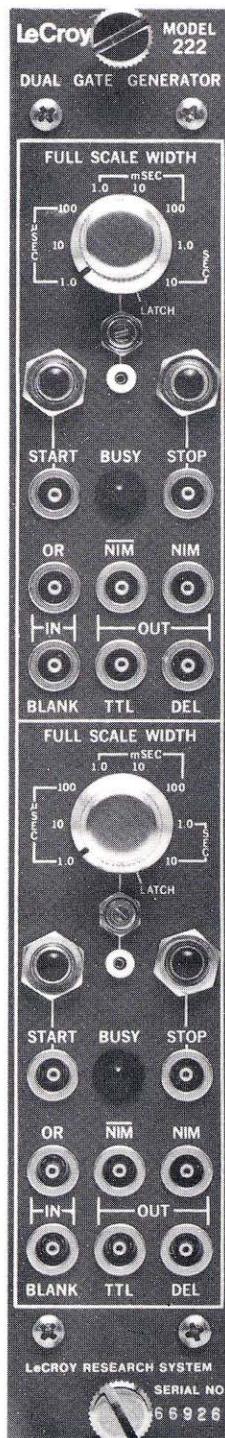
See Discriminators
2228A, 2229, 4291B, 1878, 1879, 4201,
4208

TPC's AND IMAGE CHAMBERS

2261, 1860 Series, MVV200

TIME-OF-FLIGHT SPECTROMETERS

See Discriminators
Time-To-Digital Converters: 2228A, 2229,
4201, 4208



NIM Model 222

Dual Gate and Delay Generator

- No dead time
- Responds to TTL or fast NIM inputs
- "OR" input to permit extending gate with external signal
- Fast NIM (normal and complement) and TTL outputs
- NIM level blanking input
- NIM level delayed output
- Built-in bin gate drivers
- Presettable gate durations from < 100 nsec to > 11 sec
- Front panel monitor point to permit determination of gate duration with standard voltmeter
- Does not require 6-volt NIM bin

The LeCroy Model 222 Dual Gate and Delay Generator provides two complete delay/gate channels in a single NIM module, combining in one compact package many important features formerly requiring separate expensive circuits.

The Model 222 eliminates the problems exhibited by previously available gate generators. There is negligible recovery time associated with the unit at any width setting; it may be retriggered immediately after the gate returns to its quiescent state in all ranges. Each channel of this single module can also be used to provide delays and gate outputs and to drive bin gates in its own bin and several external bins. In addition, an "OR" input for each channel permits the gate and delay interval to be extended by an external input.

The Model 222 provides a range switch and a screwdriver-adjustable potentiometer to permit continuous adjustment of gate durations from less than 100 nsec to greater than 11 seconds. The approximate gate setting may be easily determined without an oscilloscope by means of the front panel monitor point which provides a DC voltage related to the gate duration. A conversion graph is enclosed with the unit. In addition to preset width ranges, the range switch has a "latch" position to provide a continuous gate controllable by either the "Start" and "Stop" inputs or by the "Start" and "Stop" pushbuttons.

SPECIFICATIONS

NIM Model 222

DUAL GATE AND DELAY GENERATOR

EACH CHANNEL

INPUT CHARACTERISTICS

Start Input:

One: responds to both fast NIM-level and TTL-level inputs.

Fast NIM Input Requirements: Greater than -600 mV enables; minimum width 5 nsec; $50\ \Omega$ impedance for any input from $+100$ mV to -5.0 V.

TTL Input Requirements: Greater than $+2.5$ volts enables; minimum width approx. 20 nsec; high impedance for any input from $+400$ mV to $+6$ volts. (Requires $+5$ mA at $+2.5$ V.)

Stop Input:

One: Characteristics same as for "Start" input. Used when range switch is in Latch position. Can be used in Preset position but will cause a "delayed stop".

Blanking Input:

One: Requires fast NIM-level inputs (≥ -600 mV) $50\ \Omega$ impedance; blanks all outputs which occur during its presence, including the delayed output.* Maximum blanking rate, 80 MHz.

"OR" Input:

One: Requires fast NIM-level inputs (≥ -600 mV); $50\ \Omega$ impedance; extends preset gate duration by the portion of its input signal that occurs after the preset output time.

OUTPUT CHARACTERISTICS

Gate Outputs:

One standard fast NIM-level output (quiescently 0 volts; -750 mV during pulse) of approx. 2 nsec risetime; falltime slightly longer on wide widths.

One complementary fast NIM-level output (quiescently -750 mV; 0 volts into $50\ \Omega$ during pulse).

One TTL-level output (quiescently 0 volts; $> +2.5$ volts into $50\ \Omega$ during pulse).

Delayed Output:*

Delivers 10 nsec (FWHM) fast NIM-level signal into $50\ \Omega$. Occurs approximately at the trailing edge of the preset or start-stop gate output (including any gate extension due to input "OR"); ≤ 2.5 nsec risetime.

Presettable Gate Durations:

Continuous from < 100 nsec to > 11 sec. plus latched position; full scale switch determines range. On single width version, screwdriver-adjustment vernier permits fine adjustment from $\leq 10\%$ to $> 110\%$ of full scale (screwdriver included). Front panel test point gives DC voltage related to gate width (in % of range switch setting). Conversion chart included with module. On double width version, front panel locking potentiometer replaces the screwdriver adjust pot and monitor point. Output width jitter, approx. 0.05% of setting.

GENERAL

Recovery Time:

None; unit may be retriggered immediately after gate output returns to its quiescent state.

Input-Output Delay:

14 nsec.

Manual:

Front panel "Start" and "Stop" pushbuttons permit manual operation when full scale switch set on "latch", and single-shot presettable operation when full scale switch is in any other position.

Bin Gate Driver:

Each channel has one rear panel Lemo type connector which switch selectively drives external bins in either normal or inverted direction. Logic 1: < 1 volt at 200 mA; logic 0.5 volts into high impedance ($2\ k\Omega$).

Channel Select Switch:

Rear panel 3-position switch (A/B/OFF) determines which channel drives the bin in which the Model 222 is located.

Busy Indicator:

Front panel LED remains on when gate output is present, even if extended by "OR" input.

Packaging:

NIM-standard single width module; Lemo type connectors.

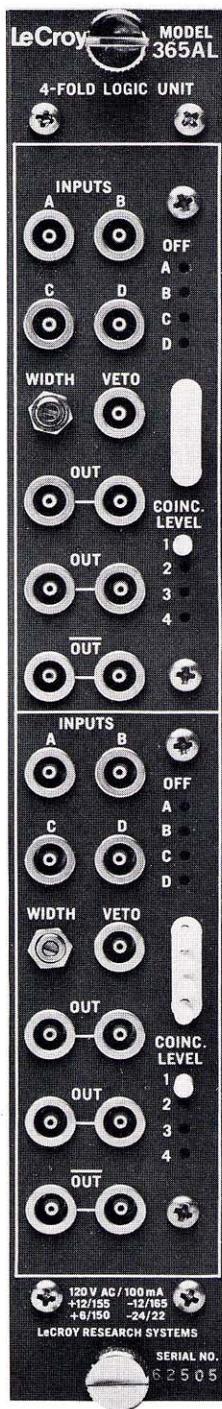
Current Requirements:

$+12$ V at 95 mA	$+24$ V at 45 mA	$+ 6$ V at 235 mA (drawn from $+12$ V if unavailable)
-12 V at 180 mA	-24 V at 80 mA	

*Blanking of the delayed output may be disabled by factory option.

TECHNICAL DATA

LeCroy



NIM Model 365AL

Dual 4-Fold Majority Logic Unit With Veto

The Model 365AL offers an unmatched combination of flexibility, compactness, and performance at a reasonable cost. It provides the functions of fan-in, coincidence, inhibit, and majority logic with high fan-out capability along with 150 MHz operation. Each of the two identical channels accepts standard NIM logic signals at each of the four logic inputs and one veto input.

Front-panel selectors allow programming of one to four simultaneous negative input signals required for an output and provide the ability to disable the separate logic inputs without removing cables. Separate veto inputs are provided for inhibiting the unit regardless of the state of the other inputs. The inhibit need only overlap the leading edge of the coincidence. A single output pulse is produced regardless of input amplitude or duration (no multiple pulsing).

The output pulse duration of the Model 365AL may be continuously set from 3.8 nsec to 50 nsec by a multturn front-panel potentiometer. The duration is independent of input overlap time, amplitude, and rate. Because it is updating, it may be retriggered even before the end of an output pulse that is already present. Two sets of dual (32 mA) negative outputs and one set of dual complementary outputs are provided. Each may be fanned out to two later inputs or be used as a means of cable clipping or reverse terminating.

August 1982

SPECIFICATIONS

NIM Model 365AL

DUAL 4-FOLD MAJORITY LOGIC UNIT WITH VETO

INPUT CHARACTERISTICS

Logic Inputs:	4 Lemo-type connectors; 50 Ω impedance; NIM level input requirements; each input can be separately enabled or disabled.
Veto Input:	Lemo-type connector; 50 Ω impedance; NIM level input requirements. Requires 3 nsec minimum width delayed 3 nsec from leading edge of input.
Bin Gate:	Via rear connector; clamp to ground from +4 volts inhibit; rise and falltimes < 50 nsec.

OUTPUT CHARACTERISTICS

Outputs:	Three; two negative (quiescently 0 mA, -32 mA during output), one positive (quiescently -32 mA, 0 mA during output).
Fan-Out:	6-fold, if each output drives two 50 Ω loads. (Any used output pair should drive 25 Ω for proper amplitude and shape.)
Duration:	Continuously adjustable from less than 4 nsec to greater than 50 nsec by means of front-panel screwdriver-adjustable potentiometer. Updating.
Output Rise and Falltimes	1.2 nsec typical. (Falltime is slightly longer at wide widths.)

GENERAL

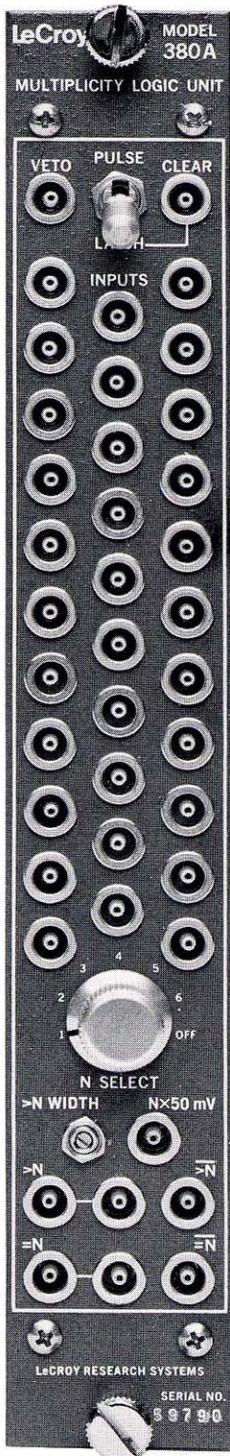
Functions:	AND; OR; Majority Logic; Leading Edge Inhibit; Complement; Pulse standardization without multiple pulsing; coincidence level determined by front-panel selector.
Coincidence Width:	1 nsec up, determined by input pulse durations.
Rate:	150 MHz minimum.
Input-Output Delay:	Approximately 10 nsec.
Double Pulse Resolution:	Typical 5 nsec; (6.5 nsec for triple pulses).
Packaging:	NIM single-width module; Lemo-type connectors used for all inputs and outputs.
Power Requirements:	+ 12 V at 55 mA* - 12 V at 165 mA - 24 V at 22 mA 115 V AC at 70 mA

*Increases to 120 mA if both channels in 4-fold coincidence.

SPECIFICATIONS SUBJECT TO CHANGE.

TECHNICAL DATA

LeCroy



NIM Model 380A Multiplicity Logic Unit

The LRS Model 380A Multiplicity Logic Unit for the first time allows easy generation of higher order multiplicity decisions from a large number of counter or chamber logic signals. The unit produces an output whenever N (or $> N$) out of M input pulses are present, where N is switch-selectable from 1 to 6, and M is any number up to 32. Two sets of outputs are provided, one set for the $= N$ condition and one set for the $> N$ condition. An additional analog summing output is provided giving an amplitude of -50 mV into 50Ω for each coincident input pulse and a duration equal to the overlap time of the coincident input signals. Since the unit can operate in an ungated mode, and does not require a master strobe signal, it is very useful in trigger pulse generation systems. In systems where a master trigger already exists (e.g., with wire chambers), the Model 380A may be operated in a strobed mode with either pulse or latched outputs. Input speed is compatible with normal 100 MHz logic and maximum output rate is determined by output width.

In the pulse mode, the duration of the $= N$ outputs is preset to 20 ns, but is internally adjustable up to 50 ns. The duration of the $> N$ outputs is front-panel adjustable from 25-100 ns and must be set equal to the maximum possible overlap time of the logic inputs. The $> N$ outputs are generated approximately 12 ns after the $> N$ condition is satisfied. The $= N$ outputs appear somewhat later, approximately 8 ns after the end of the $= N$ input condition, because of the logical necessity of waiting to insure no $> N$ condition occurs.

A clear input is provided to reset the unit in the latched mode. For strobed operation, the veto is driven by a complementary logic signal which goes to zero volts during the strobe interval.

May 1982

SPECIFICATIONS

NIM Model 380A

MULTIPLICITY LOGIC UNIT

INPUT CHARACTERISTICS

Logic Inputs:	32; reflections < 7% for inputs of 2 ns risetime; input range – 650 mV to – 900 mV (NIM level); minimum input width 6 ns.
Veto:	Common to all channels; direct-coupled; – 600 mV or greater inhibits; impedance 50 Ω; reflections < 7% for inputs of 2 ns risetime. Veto must overlap logic inputs.
Slow (Bin) Gate:	Via rear connector, with rear-panel On-Off switch; risetimes and falltimes approximately 20 ns; quiescently above + 4 volts, clamping to ground inhibits; direct-coupled.
Clear:	NIM level; minimum duration 10 ns.

OUTPUT CHARACTERISTICS

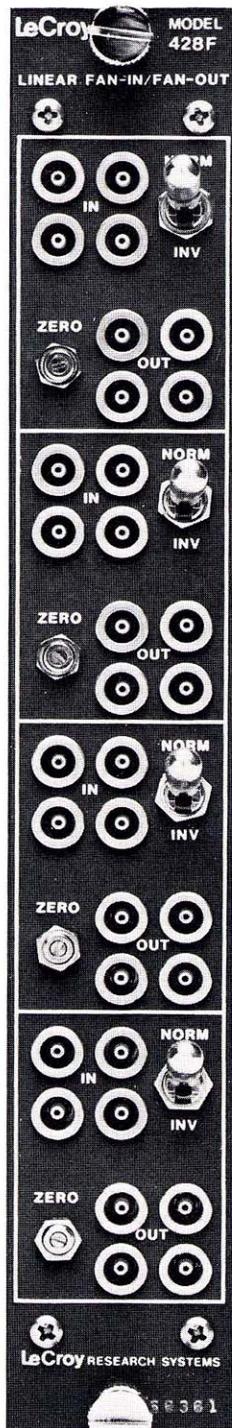
> N Outputs:	2 bridged negative outputs (quiescently 0 mA, – 32 mA during output); one complement (quiescently – 16 mA, 0 mA during output); duration variable from 25-100 ns by means of front panel-multiturn potentiometer in pulsed mode, dc level in latched mode. Must be set ≥ maximum possible overlap time of the logic inputs (since it serves to inhibit the = N outputs when present).
= N Outputs:	2 bridged negative outputs (quiescently 0 mA, –32 mA during output); one complement (quiescently –16 mA, 0 mA during output); duration 20 ns (internally adjustable) in pulse mode, dc level in latched mode.
Risetimes and Falltimes:	3 ns.
Analog Summing Output:	One; amplitude – 50 mV into 50 Ω for each coincident input pulse; duration equal to the overlap time of the coincident input signals; impedance approx. 6 Ω.

GENERAL

Coincidence Level Control:	From 1 to 6 plus "off"; front-panel switch.
Input Double-Pulse Resolution:	< 10 ns.
Output Double-Pulse Resolution:	< 30 ns.
Modes:	Pulse or latched; controls output duration.
Delay:	Input-Output, 12 ns for > N output, 8 ns following end of = N condition for = N output.
Packaging:	In conformance with AEC standard for nuclear modules (AEC Report TID-20893); RF shielded AEC #1 module fitting 12/bin; dimensions 1.375 x 8.75 x 10 inches deep.
Current Requirements:	+ 6 V at 95 mA – 6 V at 400 mA + 24 V at 45 mA

TECHNICAL DATA

LeCroy



NIM Model 428F

Quad Linear Fan-In/Fan-Out

The LeCroy Model 428F Quad Linear Fan-In/Fan-Out combines the functions of two previously separate LeCroy linear circuits in one compact unit. Each of the Model 428F's four channels contains 4 direct-coupled linear bipolar inputs, a polarity inversion switch, and four direct-coupled linear outputs. The bipolar inputs, together with the polarity switch, allow convenient summing of either anode or dynode pulses. An output swing of +100 mV to -2 volts is compatible with all normal analog inputs (e.g., discriminators, ADC's, etc.) and also accommodates standard logic levels. Each of the Model 428F's inputs is provided LeCroy high-risk input protection circuitry which gives immunity to transient signals up to ± 5 A for 0.5 microsecond.

The incorporation of the polarity switch is particularly significant in that it enables convenient, direct use of the fanned-out dynode signals for multiple fast logic decisions, while the anode signal can be directly applied to a current-integrating ADC.

All outputs are reverse-terminated and mutually isolated. The Model 428F utilizes a direct-coupled feedback-stabilized circuit design that provides excellent linearity, long-term stability, and uniformity of gain and pulse shape. The speed of the unit is suitable for all common photomultiplier and logic signals, and there are no duty cycle limitations or rate effects in the Normal Mode.

In the Inverting Mode, the Model 428F operates as a capacitively-coupled unit with a 400 μ sec time constant, recovering to the average non-inverted DC input level. In addition, the Model 428F exhibits duty-factor-related baseline shifts equal to twice that of a normal AC-coupled circuit. Thus, although the Inverting Mode provides great versatility and convenience in application, some care must be exercised when using this mode with wide inputs or at high rates.

The Model 428F is packaged in a standard NIM #1 width module and utilizes ± 12 V, ± 24 V at little enough current to permit the use of 12 modules (48 channels) in a standard NIM power bin.

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SPECIFICATIONS

NIM Model 428F

QUAD LINEAR FAN-IN/FAN-OUT

INPUT CHARACTERISTICS

Number of Channels:	Four.
Inputs:	4 per channel; $50\ \Omega$; direct-coupled in non-inverting mode. In inverting mode operates as a capacitively-coupled unit with a $400\ \mu\text{sec}$ time constant.
Polarity:	Positive or negative.
Reflection Coefficient:	Less than 7% for inputs of 2 nsec risetime.
Input Protection:	Inputs protected against $0.5\ \mu\text{sec}$ transient overloads, up to $\pm 5\ \text{A}$.

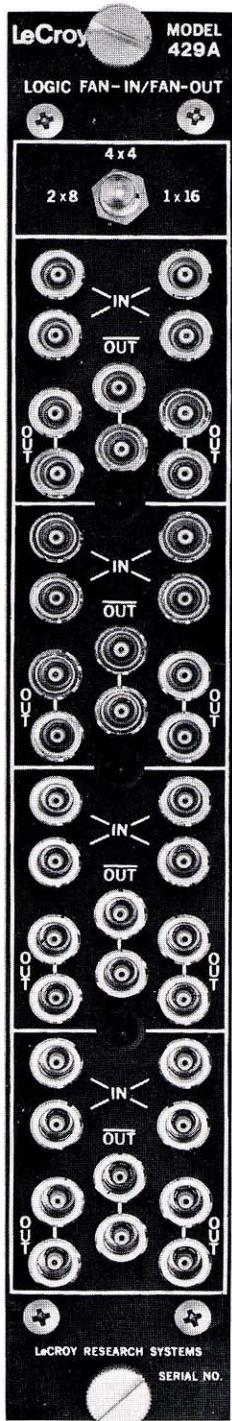
OUTPUT CHARACTERISTICS

Outputs:	4 per channel; reverse-terminated; direct-coupled; for optimum output shape, three outputs must be terminated into $50\ \Omega$. For proper operation, at least 2 outputs must be terminated on each channel used.
Integral Non-Linearity:	$\pm 1\%$ up to $-1\ \text{volt}$.
Linear Range:	Normal Mode: $+100\ \text{mV}$ to $> -2\ \text{volts}$. Inverting Mode: $+100\ \text{mV}$ to $> -1.5\ \text{volts}$.
Maximum Amplitude:	Normal Mode: $> -2.0\ \text{volts}$ into $50\ \Omega$. Inverting Mode: $> -1.5\ \text{volts}$ into $50\ \Omega$.
Risetimes and Falltimes:	$\leq 2.5\ \text{nsec}$, 10% to 90%, with outputs terminated in $50\ \Omega$.
Gain:	Normal Mode: $1.0 \pm 2\%$ up to $-2\ \text{volts}$. Inverting Mode: Approximately 0.98 up to $-1.5\ \text{volts}$.
Duty Cycle Limitations:	None for direct-coupled outputs.
DC Offset:	Adjustable with front-panel potentiometer. Care should be taken to readjust DC level whenever the Normal/Inverting switch is used.
DC Offset Stability:	$< 60\ \mu\text{V}/^\circ\text{C}$ in normal and inverting modes.
Output DC Level Voltage Coefficient:	$< 25\ \mu\text{V}/1\%$ variation of any voltage in normal and inverting modes.
Interchannel Isolation:	40 dB.
Noise:	$< 750\ \mu\text{V}$ rms.
Stage Delay:	$< 6\ \text{nsec}$.
Overload Recovery:	Approximately 2 nsec with four simultaneous NIM level ($-800\ \text{mV}$) inputs.

GENERAL

Polarity Inversion:	A front-panel switch on each channel selects normal or inverting operation.
Packaging:	RF-shielded AEC/NIM #1 module; dimensions $1.375 \times 8.75 \times 10$ inches deep. Lemo-type connectors.
Current Requirements:	$+24\ \text{V}$ at $80\ \text{mA}$, $-24\ \text{V}$ at $80\ \text{mA}$, $+12\ \text{V}$ at $160\ \text{mA}$, $-12\ \text{V}$ at $160\ \text{mA}$.

SPECIFICATIONS SUBJECT TO CHANGE



NIM Model 429A

Quad Mixed Logic Fan-In/Fan-Out

The LeCroy Model 429A is a *multifunctional* fast logic module designed to fulfill a wide variety of signal handling needs. It combines the operations of TTL-to-NIM level translation, logic fan-in, logic fan-out, and polarity inversion in one low-cost module. Each of the four channels of the Model 429A has four inputs which accept both NIM and TTL levels. This is particularly important for present generation experiments involving MWPC systems and elaborate digital triggers.

Each channel of the Model 429A contains four independent logic inputs, four normal logic outputs, and two complementary logic outputs. Channels may be paralleled to provide up to 16 inputs and 24 outputs by means of a front-panel switch. An efficient circuit design holds the power dissipation of the entire module to within the NIM standard.

The Model 429A eliminates the extra cabling and time delay involved when conventional fan-ins and fan-outs must be cascaded. In addition, it eliminates the common use of expensive logic units to perform logical OR-ing with adequate fan-out. The ability to conveniently parallel channels permits the 429A a degree of flexibility and efficiency heretofore unavailable.

Inputs are $50\ \Omega$ impedance for NIM or TTL signals. Unused inputs need not be terminated. Inputs may be driven with single or double amplitude NIM signals or TTL signals without affecting output amplitude. The three pairs of bridged outputs are direct-coupled current sources which deliver -32 mA into two $50\ \Omega$ loads. Output duration is equal to the logical sum of the input durations.

The circuitry of the Model 429A is complete direct-coupled and compatible with either normal or complementary logic signals in any duty ratio. Channel paralleling is accomplished by means of a single front-panel locking switch that is not in the signal path and hence permits switching with minimal effect on signal fidelity. Front-panel lamps located between channels light to indicate channels that are combined, providing a clear, easily-interpreted display of the unit's status.

SPECIFICATIONS

NIM Model 429A

QUAD MIXED LOGIC FAN-IN/FAN-OUT

Number of Sections: Four; may be cascaded by means of front-panel switch to form dual 8-fold fan-in/12-fold fan-out or single 16-fold fan-in/24-fold fan-out, with LED indication.

INPUT CHARACTERISTICS

Number of Inputs: Four per section.
Impedance: $50 \Omega \pm 5\%$.
Reflections: $< 10\%$ for input risetimes ≥ 2 nsec.
Quiescent Level: 0 volts dc.
Signal Level Requirements: Standard NIM logical 1 input levels: -12 mA to -36 mA; standard TTL logical 1 input levels: $+2$ V to $+5$ V.
Signal Width Requirements: 4 nsec minimum, FWHM.
Coupling: Direct.

OUTPUT CHARACTERISTICS

Number of Outputs: 4 normal (2 bridged pairs); 2 complementary (1 bridged pair).
Output Levels: Normal: quiescently 0 mA, > 28 mA into two 50Ω during outputs.
Complementary: quiescently, > 28 mA into two 50Ω loads, 0 mA during output.
Risetimes and Falltimes: 2.3 nsec typical, 2.8 nsec maximum.
Duration: Equal to the logical sum of the input durations.
Time Variation of Output with Input Amplitude: < 1 nsec worst case between inputs of -600 mV and -1.6 volts; typically < 0.5 nsec.
Time Variation Between Outputs: 4 channels, 4 x 6 operation: < 0.2 nsec;
2 channels, 8 x 12 operation: < 0.4 nsec;
1 channel, 16 x 24 operation: < 0.9 nsec.

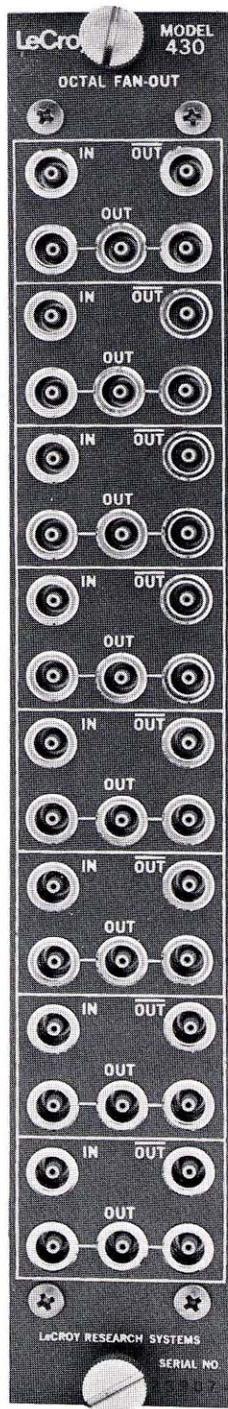
GENERAL

Rate: > 100 MHz.
Stage Delay: < 6.5 nsec.
Duty Cycle Limitations: None.
Packaging: Single-width AEC/NIM module; in conformance with AEC standard for nuclear modules (AEC Report TID-20893); Lemo-type connectors.
Current Requirements: $+12$ V at 35 mA $+6$ V at 295 mA
 -12 V at 50 mA -6 V at 460 mA

SPECIFICATIONS SUBJECT TO CHANGE.

TECHNICAL DATA

LeCroy



NIM Model 430

Octal Logic Fan-Out

- * 8 channels in a single-width module
 - * 4 outputs per channel
 - * Maximum rate >150 MHz
 - * Direct coupled
 - * Stage delay <2.5 nsec
 - * Low power dissipation permits up to 96 fan-out channels
(384 outputs) per standard bin

The LeCroy Model 430 Octal Logic Fan-out provides a unique combination of high fan-out and performance in an exceptionally compact unit. Designed for flexibility in both small and large scale experiments, the 430 offers eight independent channels, each of which supplies three normal and one inverted outputs.

The input to each channel is terminated in 50Ω and may be driven with either single or double amplitude NIM level signals. The output amplitude is independent of input signal overdrive and the high-speed circuitry accurately restandardizes amplitudes of all input signals of width greater than 4 nsec. The normal outputs are generated by a current source which delivers -48 mA into three bridged connectors. The voltage swing is limited to approximately -900 mV, and unused outputs do not require termination to control signal amplitude. The complementary output delivers -16 mA in a 50Ω load.

The circuitry of the Model 430 is completely direct coupled and compatible with normal or complementary logic signals in any duty ratio. The wideband design permits operation at rates in excess of 150 MHz. Stage delays of less than 2.5 nsec assist in minimizing logic system decision time and provide good time resolution (absolute delay and jitter) between all channels.

The 430 is packaged in an RF-shielded single-width NIM Module utilizing LEMO connectors. Power dissipation is within standard limits, permitting 12 modules (96 independent fan-out channels) to be housed in one bin.

October 1977

SPECIFICATIONS

NIM Model 430

OCTAL LOGIC FAN-OUT

Number of Sections: Eight.

INPUT CHARACTERISTICS

Number of Inputs: One per section.

Impedance: $50 \Omega \pm 5\%$.

Reflections: $<10\%$ for input risetimes $\geq 2\text{nsec}$.

Quiescent Level: 0 volts dc.

Signal Level Requirements: Standard NIM logical 1 input levels; -12 mA to -36 mA into 50Ω .

Signal Width Requirements: 4 nsec minimum, FWHM.

Coupling: Direct.

OUTPUT CHARACTERISTICS

Number of Outputs: 3 normal (bridged); 1 complementary.

Output Levels: Normal: quiescently 0 volts, $>-700 \text{ mV}$ into 50Ω during output; complementary; quiescently $>-700 \text{ mV}$ into 50Ω , 0 volts during output.

Risetimes & Falltimes: $<2.5 \text{ nsec}$.

Duration: Equal to the input duration.

Time Variation Between Channels: $<0.5 \text{ nsec}$.

GENERAL

Rate: $>150 \text{ MHz}$.

Stage Delay: $<2.5 \text{ nsec}$.

Duty Cycle Limitations: None.

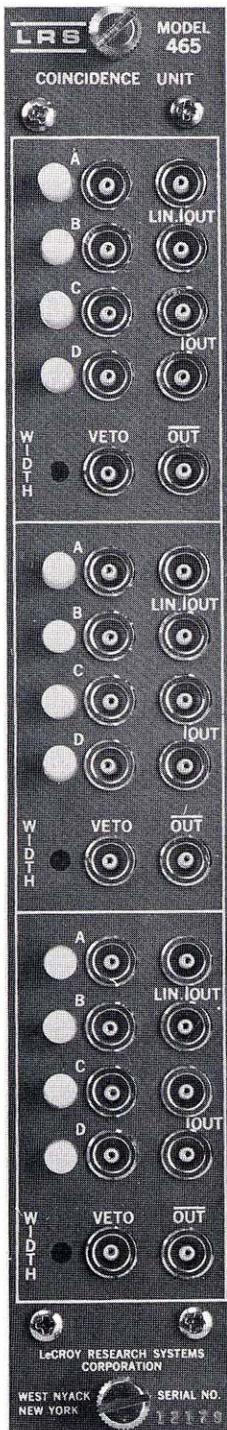
Packaging: Single-width NIM module; in conformance with AEC standard for nuclear modules (AEC Report TID-20893): Lemo-type connectors.

Current Requirements: +6 V at 100 mA
-6 V at 510 mA

SPECIFICATIONS SUBJECT TO CHANGE

TECHNICAL DATA

LeCroy



NIM Model 465 Triple 4-Fold Logic Unit WITH VETO

The LRS Model 465 contains three independent high-speed general-purpose coincidence units in a single-width NIM module. Each channel has four coincidence inputs and a separate veto input which accept standard negative NIM logic levels. The logic inputs may be individually enabled or disabled without altering input cabling or termination by means of front-panel pushbutton switches. With all inputs enabled, four inputs are required. Disabling the logic inputs is equivalent to reducing the number of simultaneous negative inputs required for an output. Thus, each channel may be programmed for 4-fold, 3-fold, or 2-fold logic decisions. With only one input enabled, each channel of the 465 operates as a logic fan-out.

Once triggered by signals satisfying the input coincidence requirements, the 465 generates five NIM fast logic outputs: one pair of -32 mA negative preset outputs, one -16 mA preset complementary output, and one pair of -32 mA overlap outputs. The preset outputs are continuously adjustable from less than 5 ns to greater than 500 ns by means of a front-panel multturn potentiometer and are independent of input overlap time, amplitude, and rate. Because it is updating, it may be retriggered even before the end of an output pulse that is already present. The overlap outputs are equal in duration to the coincidence overlap and produce outputs up to the maximum input rate capability.

The front-panel fast veto input accepts standard negative NIM-level pulses. To veto the linear outputs, the veto signal must completely overlap any input coincidence; to veto the preset outputs, a prompt overlap of the leading edge of the input signal that would otherwise create the coincidence condition is required. A rear-panel bin-gate switch permits a slower (50 ns response time) inhibiting of the 465 by a clamp to ground from +4 volts through the bin gate pin of the rear power connector.

The Model 465 is packaged in a standard AEC/NIM #1 module (AEC Report TID-20893) and uses exclusively Lemo-type front panel connectors.

SPECIFICATIONS

NIM Model 465

TRIPLE 4-FOLD LOGIC UNIT

INPUT CHARACTERISTICS

Logic Inputs:	4; Lemo-type connectors; 50Ω impedance; negative NIM-level input requirements; each input can be separately enabled or disabled by front-panel push-buttons.
Veto Input:	Standard negative NIM-level signal, 3.5 ns minimum width. Requires complete overlap of input coincidence for linear outputs and prompt overlap of the leading edge of the input signal that would otherwise create the coincidence condition for the preset outputs. (Veto should precede this leading edge by approximately 5 ns in this case.)
Bin Gate:	Via rear connector; clamp to ground from +4 volts inhibits; risetimes and fall-times < 50 ns.

OUTPUT CHARACTERISTICS

Preset Outputs:	3; one dual negative (quiescently 0 mA, -32 mA during output), one positive (quiescently -16 mA, 0 mA during output). Updating.
Overlap Outputs:	One dual negative; quiescently 0 volts, -32 mA during output; duration equal to coincidence overlap. Non-updating.
Fan-Out:	5-fold, if each output drives a 50Ω load.
Duration:	Continuously adjustable from less than 5 ns to greater than 500 ns by means of front-panel, screwdriver-adjustable potentiometer. Width stability: better than $\pm 0.2\%/\text{C}$ maximum.
Output Risetimes:*	<u>OUT</u> : ≤ 2.0 ns typical (max. 2.2 ns). <u>OUT</u> : ≤ 2.2 ns typical (max. 2.5 ns; 3.0 ns with negative output unterminated).
Output Falltimes:*	<u>OUT</u> : ≤ 2.0 ns typical (max. 2.5 ns). Slightly longer on wide output durations. <u>OUT</u> : ≤ 2.2 ns typical (max. 2.5 ns). Slightly longer on wide output durations.

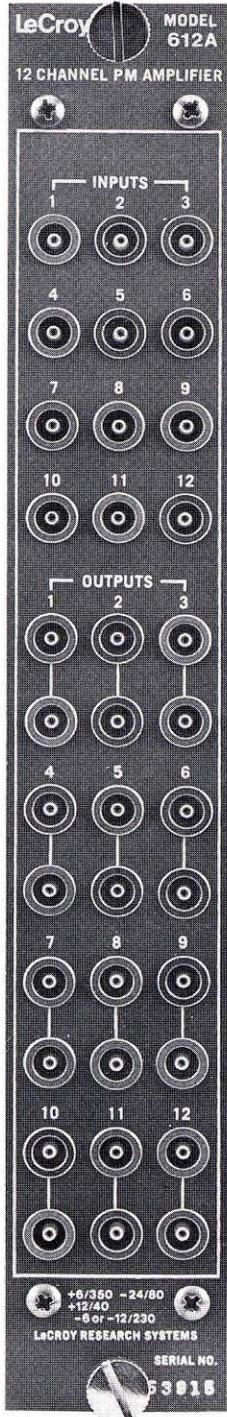
GENERAL

Logic:	2-fold, 3-fold, or 4-fold coincidences plus fan-out determined by selectively disabling logic input.
Coincidence Width:	1 ns up, determined by input pulse durations.
Rate:	120 MHz minimum.
Input-Output Delay:	13 ns preset; 8.5 ns linear.
Multiple-Pulsing:	None; one and only one output pulse of preset duration is produced each time the input conditions are satisfied regardless of the duration of the input pulses or their overlap.
Double-Pulse Resolution:	8 ns.
Packaging:	Single-width AEC/NIM module; in conformance with AEC standard; Lemo-type connectors used for all inputs and outputs.
Current Requirements:	+12 V at 65 mA +6 V at 125 mA -24 V at 5 mA -12 V at 135 mA -6 V at 640 mA

*-100 mV to -700 mV.

TECHNICAL DATA

LeCroy



NIM Model 612A

12-Channel Photomultiplier Amplifier

- * 12 channels/#1 NIM module
- * 2 identical $50\ \Omega$ outputs per channel
- * Gain of 10, direct-coupled
- * Input and Output protected against overload
- * <2 nsec risetime
- * <1 mV dc stability (short and long term) at the output
- * -5 volt linear range (5000:1 usable dynamic range)
- * 0.1% integral linearity
- * Low cost

The LeCroy Model 612A is a new 12-channel, 200 MHz bandwidth, gain of 10 linear amplifier packaged in a #1 NIM module. Representing a major advance in fast amplifier stability, dynamic range, and general utility, the 612A allows the experimenter for the first time to consider the use of economical, lower gain photomultiplier tubes even in demanding direct-coupled ADC applications. The Model 612A offers a built-in fan-out of two, simplifying simultaneous use of the same photomultiplier signal for both analog and logic purposes by eliminating the extra cable run necessary when both anode and dynode signals are used. Packaged 12 channels per module, the 612A offers substantial savings in bin space and is directly compatible with standard LeCroy 12-channel ADC's and multichannel discriminators.

A new high-speed operational amplifier circuit design makes the performance of the amplifier virtually independent of external variables such as supply voltages or temperature. Input and output DC levels remain negligibly small even when the module is moved from bin to bin, or under extremes of operating temperature. There is virtually no warm-up drift on turn-on. These stability characteristics, together with the excellent linearity, speed and noise characteristics of the circuit, come very close to the ideal of a "transparent gain" element that simply magnifies the input without significant distortion or operating constraints.

The Model 612A normally operates from +6, ± 12 , and -24 volts. A rear-panel switch permits operation from -6 instead of -12 volts for those applications in which -6 volts is easily available and where a moderate saving in power consumption is more important than dynamic range. When operated from -6 volts, maximum output amplitude is reduced from -5 to -2 volts. In either case, the large output levels available reduce recovery time problems associated with overload.

June 1980

SPECIFICATIONS

NIM Model 612A

12-CHANNEL PHOTOMULTIPLIER AMPLIFIER

INPUT CHARACTERISTICS

Impedance:	50 Ω.
Input Protection:	±5 A for 0.5 μsec; ±500 mA continuous input voltage; clamps at ±0.6 V.
Reflection Coefficient:	Less than 5% over input dynamic range.
Quiescent Voltage:	±0.5 mV.

OUTPUT CHARACTERISTICS (Both outputs of each used channel must be terminated for optimum waveshape.)

Maximum Positive Amplitude (Linear):	+200 mV.
Maximum Negative Amplitude (Linear):	-2 volts with -6 V supply; -5 volts with -12 V supply.
Overshoot:	Less than ±10% for input risetimes ≥1.5 nsec.
Quiescent Voltage:	0 V ±3 mV.
Output Voltage DC Offset Temperature Coefficient:	100 μV/°C maximum.
Output Voltage Variation with Supply Voltage:	<1 mV for ±1% variation of any supply voltage.

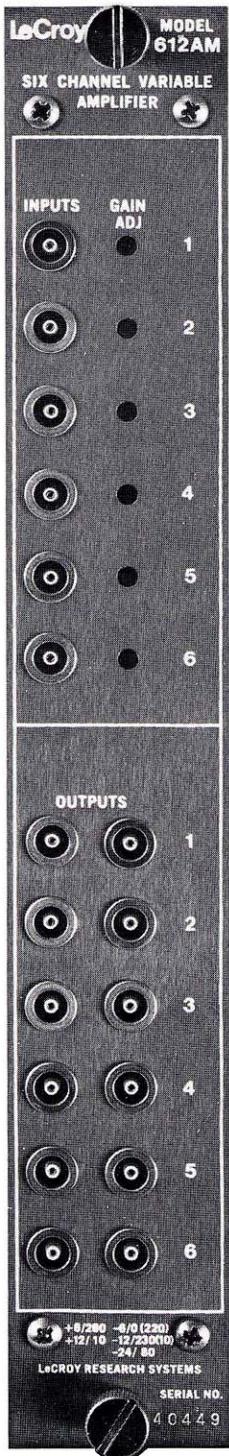
GENERAL

Gain:	Fixed gain of 10, non-inverting. Long-term stability ±1%. Gain tolerance ±5%.
Linearity:	0.1% integral.
Coupling:	Direct.
Risetime:	< 2.0 nsec, 10% to 90%.
Delay:	Approx. 4 nsec.
Noise:	Less than 50 μV rms, referred to input, total.
Interchannel Crosstalk:	Output in one channel affects any other channel by no more than -70 dB.
Overload Recovery:	a) Operation with -12 volt supply: saturated for approximately 15 nsec after 10X overload. b) Operation with -6 volt supply: saturated for approximately 50 nsec after 10X overload. For wide pulses (i.e., > 5 μsec) it is recommended to use -12 V supply for best overload recovery.
Packaging:	RF-shielded AEC/NIM #1 width module conforming to specifications outlined in AEC Report TID-20893; Lemo-type connectors.
Current Requirements:	In rear panel selected 6 V mode: +6 V at 350 mA, -6 V at 275 mA, +12 V at 5 mA, -12 V at 5 mA, -24 V at 80 mA, or in 12 V mode: +6 V at 350 mA +12 V at 5 mA, -12 V at 275 mA, -24 V at 80 mA.

SPECIFICATIONS SUBJECT TO CHANGE

TECHNICAL DATA

LeCroy



NIM Model 612AM

6-Channel Photomultiplier Amplifier

- * 6 channels/ #1 NIM module
- * Identical 50Ω outputs per channel
- * Gain of 2.5 to 40, direct-coupled
- * < 3 nsec risetime
- * -5 volt linear range (5000:1 usable dynamic range)
- * 0.2% integral linearity
- * Low cost

The LeCroy Model 612AM is a six-channel, wide-bandwidth amplifier with continuously adjustable gain packaged in a #1 NIM module. The unit features a bandwidth of DC to 140 MHz with a maximum gain of 40. Representing a major advance in fast amplifier stability, dynamic range, and general utility, the 612AM allows the experimenter for the first time to consider the use of economical lower gain photomultiplier tubes even in demanding direct-coupled ADC applications. The adjustable gain feature affords simpler high voltage distribution systems because the gains may be equalized by the 612AM. This avoids the problems of variation in photomultiplier propagation time with high voltage. The Model 612AM offers a built-in fan-out of two, simplifying simultaneous use of the same photomultiplier signal for both analog and logic purposes by eliminating the extra cable run necessary when both anode and dynode signals are used. Packaged 6 channels per module, the 612AM offers substantial savings in bin space and is directly compatible with standard LeCroy ADC's and multichannel discriminators.

A new high-speed operational amplifier circuit design makes the performance of the amplifier virtually independent of external variables such as supply voltages or temperature. Input and output DC levels remain negligibly small even when the module is moved from bin to bin, or under extremes of operating temperature. There is virtually no warmup drift on turn-on. These stability characteristics, together with the excellent linearity, speed and noise characteristics of the circuit, come very close to the ideal of a "transparent gain" element that simply magnifies the input without significant distortion or operating constraints.

The Model 612AM normally operates from ± 6 , ± 12 , and -24 volts. A rear-panel switch permits operation from -12 instead of -6 volts for those applications in which -6 volts is not available or where dynamic range is more important than a moderate saving in power consumption. When operated from -12 volts, maximum output amplitude is increased from -2 to -5 volts. In either case, the large output levels available reduce recovery time problems associated with overload.

SPECIFICATIONS

NIM Model 612AM

6-CHANNEL PHOTOMULTIPLIER AMPLIFIER

INPUT CHARACTERISTICS

Impedance:	50 Ω .
Input Protection:	± 5 A for 0.5 μ sec; ± 0.5 A continuous; clamps at ± 0.6 V.
Reflection Coefficient:	Less than 5% over input dynamic range.
Quiescent Voltage:	± 0.5 mV.
OUTPUT CHARACTERISTICS	(Both outputs of each used channel must be terminated for optimum wave-shape.)

Maximum Positive Amplitude (Linear):	+200 mV.
Maximum Negative Amplitude (Linear):	-2 volts with -6 V supply; -5 volts with -12 V supply.
Overshoot:	Less than $\pm 10\%$ for input risetimes >1.5 nsec and gains $>4X$. Slightly larger for gains $<4X$.
Quiescent Voltage:	0 V ± 3 mV.
Output Voltage DC Offset Temperature Coefficient:	400 μ V/ $^{\circ}$ C maximum.
Output Voltage Variation with Supply Voltage:	<4 mV for $\pm 1\%$ variation of any supply voltage.

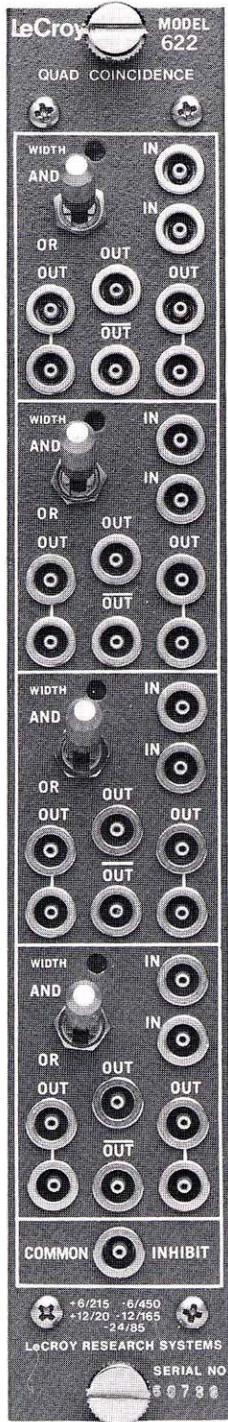
GENERAL

Gain:	2.5 to 40, non-inverting. Long-term stability $\pm 1\%$.
Linearity:	0.2% integral.
Coupling:	Direct.
Risetime:	<3.0 nsec, 10% to 90%.
Delay:	Approx. 5.5 nsec.
Noise:	Less than 50 μ V rms, referred to input, total.
Interchannel Crosstalk:	Output in one channel affects any other channel by no more than -40 dB.
Overload Recovery:	a) Operation with -12 volt supply: saturated for approximately 15 nsec after 10X overload. b) Operation with -6 volt supply: saturated for approximately 50 nsec after 10X overload. For wide pulses (i.e., >5 μ sec) it is recommended to use -12V supply for best overload recovery.
Packaging:	RF-shielded AEC/NIM #1 width module conforming to specifications outlines in AEC Report TID-20893; Lemo-type connectors.
Current Requirements:	+6 V at 280 mA; -12 V or -6 V at 230 mA (selected by rear-panel switch); +12 V at 10 mA; -24 V at 80 mA.

SPECIFICATIONS SUBJECT TO CHANGE

TECHNICAL DATA

LeCroy



NIM Model 622

Quad 2-Fold Logic Unit

The Model 622 Quad 2-Fold Logic Unit has four independent coincidence channels, each with 2 inputs and 6 outputs. Each channel is switch-selectably capable of determining an AND or an OR condition of the two inputs. In addition, a front panel veto input provides the option of inhibiting all channels simultaneously upon application of a fast, NIM-level signal.

Each channel of the 622 provides five NIM-level current source outputs and one complementary output. This high fan-out is achieved by means of an output circuit design that minimizes quiescent power. As a result, up to 12 Model 622's can be powered by a single NIM-standard power bin.*

Output durations are adjustable (via front-panel, screwdriver-control pot) from 5 ns to 1 μ s, and are highly stable and independent of input amplitude, duration and rate. Their long-term stability is excellent, permitting their direct use in subsequent coincidence applications without any need for external clipping cables. Risetimes and falltimes are less than 2.5 ns except on the single negative and complementary outputs, where they are typically less than 1.5 ns.

The LRS Model 622 Quad 2-Fold Logic Unit incorporates much of the basic circuitry found in the widely-used and highly-reliable Model 621AL Quad Discriminator. The single 621AL input was replaced by two summed inputs, and the 621AL threshold control pot was replaced by a two-position switch, which selects one of two threshold levels corresponding to either an AND or an OR requirement of the two inputs. Current limiters, added to provide an internal current standard, also provide inherent input protection against transient signals at least ± 50 V by 5 μ s in size.

The pulse-forming circuit of the Model 622 is deadtimeless (updating), and the unit may be retriggered during the time an output from a previous input signal is being produced.

*(96 watts, with ± 6 V at 10 A shared.)

January 1982

SPECIFICATIONS

NIM Model 622

QUAD 2-FOLD LOGIC UNIT

INPUT CHARACTERISTICS

Number of Channels:	4, all identical.
Logic Inputs:	Two, $50\ \Omega$ direct-coupled; reflections < 7% for standard AEC fast logic signals (-600 mV minimum) of 2 ns risetime.
Slow Bin Gate:	Via rear connector, with rear-panel, ON/OFF switch; quiescently +4 volts, clamping to ground inhibits logic unit; direct-coupled; risetimes and falltimes approximately 50 ns.
Veto:	Front-panel connector permits simultaneous inhibiting of all channels; $50\ \Omega$; requires NIM-level signal ($> -600\text{ mV}$); direct-coupled; must overlap leading edge of input signal that would otherwise cause the coincidence condition; must precede input by approximately 5 ns.

OUTPUT CHARACTERISTICS

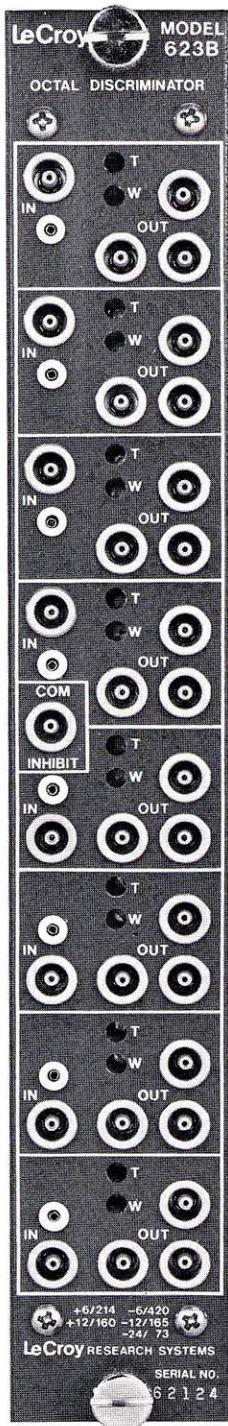
Bridged Negative Outputs:	2 pairs; NIM, quiescently 0 mA, -32 mA during output; duration, 5 ns to $1\ \mu\text{s}$, continuously variable up to 600 ns via front-panel screwdriver control (narrower widths possible at slight expense of amplitude); risetimes and falltimes (all outputs terminated in $50\ \Omega$) typically 2.0 ns (max. 2.5 ns), 10% to 90%. Output falltimes slightly longer on wide output durations. Width stability better than $\pm 0.2\%/\text{C}$ maximum. Updating.
Fast Negative Timing Output:	One, NIM; quiescently 0 mA, -16 mA during output. Other characteristics same as above, except risetimes are typically 1.5 ns (max. 2.0 ns) and minimum width is $\leq 6\text{ ns}$.
Complementary Output:	One; quiescently, -16 mA , 0 mA during output. Other characteristics same as for Fast Negative Timing Output.

GENERAL

Functions:	Fan-in (2-fold); coincidence; inhibit.
Maximum Rate:	110 MHz typical, input and output.
Coincidence Width:	Determined by input pulse durations; total widths from approximately 1.0 ns up without limit.
Double-Pulse Resolution:	Less than 9 ns at minimum output width setting.
Input-Output Delay:	9.5 ns typical.
Multiple-Pulsing:	None; one and only one output pulse of preset duration is produced for each input pulse, regardless of input pulse amplitude or duration.
Packaging:	In RF-shielded, AEC/NIM #1 module (AEC Report #TID-20893); Lemo-type connectors.
Current Requirements:	-6 V at 450 mA; $+6\text{ V}$ at 215 mA; -12 V at 165 mA; $+12\text{ V}$ at 20 mA; -24 V at 85 mA.

TECHNICAL DATA

LeCroy



NIM Model 623B

Octal Updating Discriminator With Inhibit

The Model 623B is a low cost eight channel discriminator featuring high-sensitivity, high-speed, updating performance. A Common Inhibit adds to the versatility of the Model 623B which may be used as an enable for pulsed-mode applications. This discriminator, based upon the proven popular Model 623, offers high density economically.

The minimum threshold of the Model 623B is -30 mV , variable up to -1 V via front-panel screwdriver adjustment. A monitor point is provided to permit measurement of the threshold level with a voltmeter rather than the more difficult and less precise analog measurement via oscilloscope. The stability of the threshold is $<0.2\%/\text{ }^{\circ}\text{C}$, assuring accurate results even in varied operating environments. Because of the extremely low reflections from its input (4%), the 623B is significantly better protected against the multiple-pulsing due to reflections at -30 mV .

The Model 623B operates at maximum rates in excess of 100 MHz. Its updating design permits retrigerring even while an output from a previous input is still present. At minimum output width setting the 623B will respond to a second pulse within 9 nsec of the leading edge of the first pulse. Propagation delay through the 623B is approximately 11 nsec.

The outputs of the 623B are low impedance voltage outputs, providing output levels greater than -800 mV into a $50\text{ }\Omega$ load. The output durations may be independently set via front-panel screwdriver adjustment from $<6\text{ nsec}$ to $>150\text{ nsec}$. Output risetimes are typically 2.1 nsec. Output falltimes increase with output width from approximately 4 nsec at short widths to approximately 7% of the output width at maximum.

March 1980

SPECIFICATIONS

NIM Model 623B

OCTAL UPDATING DISCRIMINATOR WITH INHIBIT

SIGNAL INPUT CHARACTERISTICS

Individual Signal:

Threshold: -30 mV to approximately -1.0 volt ; front-panel screwdriver adjust (screwdriver included).

Impedance: $50 \Omega \pm 1\%$, protected to $\pm 5 \text{ A}$ for $0.5 \mu\text{sec}$ clamping at $+1$ and -7 volts .

Reflections: $<4\%$ for input pulses of 2 nsec risetime.

Stability: $<0.2\%/\text{C}$, 20°C to 60°C operating range.

Offset: $0 \pm 1 \text{ mV}$.

Threshold Monitor: $10:1$ ratio of monitor voltage to actual voltage.

Common Inhibit:

Input: Accepts NIM standard inputs. -600 mV disables all channels.

Impedance: $50 \Omega \pm 5\%$.

Timing: NIM pulse must precede analog input by 6 nsec to inhibit. Minimum width 8 nsec . Effective width 5 nsec less than NIM input width.

OUTPUT CHARACTERISTICS

Amplitude: 3 NIM-level voltage outputs, quiescently 0 volts , -800 mV during output.

Duration: $\leq 6 \text{ nsec}$ to $>150 \text{ nsec}$, continuously variable via front-panel screwdriver control.

Risetime: Typically 2.1 nsec ; maximum 2.5 nsec . At least 2 outputs should be terminated in 50Ω for optimum pulse shape.

Falltime: Approx. 4 nsec at minimum width, increasing with width setting up to 10 nsec max.

Width Stability: Maximum $\pm (50 \text{ psec} + 0.3\%)/\text{C}$ for temperature variation and $\pm 0.1\%/\%$ for variation of any supply voltage.

Amplitude Stability: Better than $\pm 0.1\%/\text{C}$.

GENERAL

Maximum Rate: $>100 \text{ MHz}$, input and output.

Double-Pulse Resolution: Less than 9 nsec .

Time Slewing: 1 nsec for input amplitudes 110% of threshold and above.

Input-Output Delay: 11 nsec .

Multiple-Pulsing: None; one and only one output pulse of preset duration is produced for each input pulse, regardless of input pulse amplitude or duration.

Bin Gate: Slow gate via rear connector and rear-panel ON-OFF switch; risetimes and falltimes approximately 50 nsec ; clamp to ground from $+5 \text{ volts}$ inhibits; direct-coupled.

Packaging: In RF-shielded AEC/NIM #1 module; Lemo-type connectors.

Current Requirements: $+12 \text{ volts}$ at 160 mA

$+ 6 \text{ volts}$ at 240 mA

$- 6 \text{ volts}$ at 490 mA

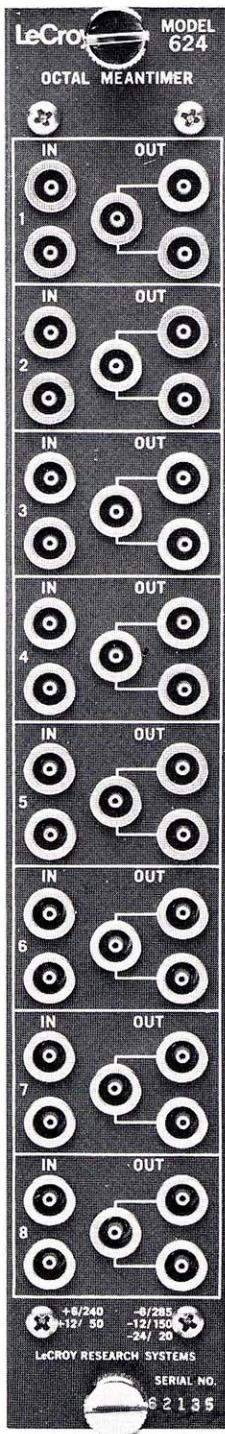
-12 volts at 195 mA

-24 volts at 80 mA

SPECIFICATIONS SUBJECT TO CHANGE

TECHNICAL DATA

LeCroy



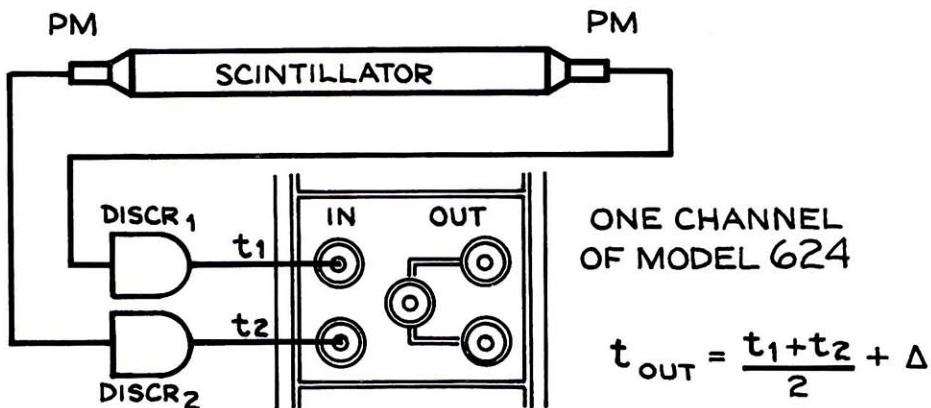
NIM Model 624 Octal Meantimer

A common problem in experiments where the scattering angles are large, necessitating long scintillators, is the difficulty in the extraction of precise timing information. Since a scintillator of several meters length is not uncommon at many facilities, the time of an output pulse emerging from a phototube attached to one end of the scintillator may vary by up to tens of nanoseconds depending upon where the particle struck the detector.

The Model 624 Octal Meantimer was designed to equalize the photon transit time by providing an output pulse at always a fixed time independent of where the impact occurred. Used in conjunction with a phototube and one discriminator at each end of the scintillator, the 624 accepts the two discriminator outputs, feeds them through a delay line element in opposite directions, and gives an output pulse at a time when the pulses overlap. The delay line element, socketed and field-changeable, has 17 pickoff points giving a time resolution of 0.5 nsec.

The three bridged outputs of each 624 channel are driven from a 45 mA differential stage current source, each output giving an amplitude of -750 mV into $50\ \Omega$ if all are terminated. Conveniently, for applications where long cables must be driven, one or more outputs may be left unterminated to give a larger output amplitude to compensate for attenuation through the cable. The duration of the outputs is approximately equal to the total overlap time of the two input signals.

Packaged in a standard NIM #1 width module, the Model 624 may also be provided by special factory option at increased cost with six outputs per channel at the expense of additional current usage (Model 624M).



June 1982

SPECIFICATIONS

NIM Model 624

OCTAL MEANTIMER

INPUT CHARACTERISTICS

Number of Channels: 8, all identical.

Logic Inputs: Two, $50\ \Omega$ direct-coupled; reflections $<7\%$ for standard NIM fast logic signals (-600 mV minimum) of FWHM of $\geq 7\text{ nsec}$ with 2 nsec risetime.

OUTPUT CHARACTERISTICS

Number and Type: Three, bridged, driven from 45 mA current source; quiescently, 0 mA; 45 mA during output (-800 mV nominal with all 3 terminated into $50\ \Omega$). Maximum output amplitude, -2 volts .

Duration: Input pulse duration less approximately 4 nsec.

Risetime-Falltime: 2.5 nsec maximum, with all outputs terminated.

GENERAL

Delay Line Elements: 16 nsec, 17 pickoff points* (15 taps, plus ends).

Time Resolution: 0.5 nsec.*

Input-Output Delay: 5 nsec plus $t_d + (D - t_d)/2$, where t_d = time delay between the two input pulses and D = value of delay line element.

Total Meantime Calculation: With reference to the actual time the particle passes through the scintillator, the time of output is 5 nsec plus one-half the sum of all the delays through the loop, including total scintillator transit time, delay line element value, all cable and discriminator delays.
NOTE: This total time is constant with respect to the scintillator impact time, regardless of impact position.

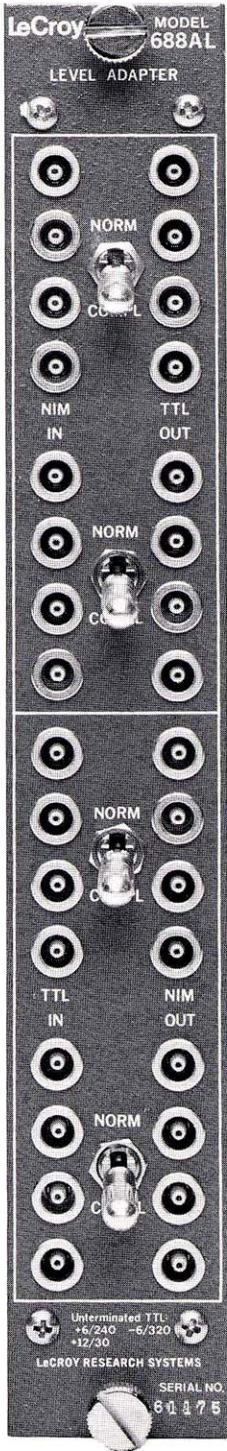
Packaging: In RF-shielded AEC/NIM #1 module, (AEC Report TID-20893); Lemo-type connectors.

Approximate Current Requirements: +6V at 240 mA
-6V at 285 mA
+12V at 50 mA
-12V at 150 mA
-24V at 20 mA

*32 nsec and 40 nsec scales available upon request.

TECHNICAL DATA

LeCroy



NIM Model 688AL Level Adapter

- 8 NIM to TTL and 8 TTL to NIM converters
- Direct - coupled
- Full input protection
- TTL outputs compatible with terminated $50\ \Omega$ cable
- Switchable normal or complementary operation in groups of four
- No duty cycle limitations
- Single-width module

The LRS Model 688AL Level Adapter provides 8 channels of direct-coupled NIM-to-TTL and 8 channels of TTL-to-NIM conversion in a single-width NIM module. Standard negative TTL notation is used to be compatible with unterminated CAMAC and slow NIM logic levels.

The NIM-to-TTL section accepts either normal or complementary NIM logic levels (logical "0" = 0 to -2 mA; logical "1" = -12 to -32 mA) at each of its eight $50\ \Omega$ inputs. The 8 outputs switch between zero volts and +2.5 volts for a time equal to the input signal duration. The polarity of the outputs is controlled by two front-panel switches common to two groups of four channels and provides either normal or complementary operation. Up to 50 mA at +2.5 volts is delivered from each output, making the TTL drive capability compatible with terminated, direct-coupled $50\ \Omega$ cable. The low level clamp capability is 100 mA, or approximately 60 standard TTL loads. Direct-coupled, the 688AL is free from any rate effects and has no limitations on duty cycle.

The TTL-to-NIM section accepts standard negative TTL logic levels (logical "1" = 0 to +.8V; logical "0" = > 2 volts) at each of its eight inputs. The minimum input duration for a full output is 10 ns. The output from each channel is a standard NIM logic level which switches between 0 volts and -16 mA (-800 mV into $50\ \Omega$) during an output. Risetimes and falltimes are < 3 ns and the output width is approximately equal to the duration of the input signal. Two front-panel switches common to two groups of four channels provides either normal operation (TTL logical "1" IN gives NIM logical "1" OUT) or complementary operation.

May 1982

SPECIFICATIONS

NIM Model 688AL

LEVEL ADAPTER

NIM TO TTL SECTION

NUMBER OF CHANNELS

Eight.

INPUT CHARACTERISTICS

Impedance:	$50 \Omega \pm 5\%$; reflections <10% for risetime > 2 ns.
Quiescent DC Level:	0 volts.
Input Signal:	Normal (logical "0" = 0 to -2 mA; logical "1" = -12 to -32 mA) or complementary fast NIM logic levels.
Input Protection:	± 5 volts.
Minimum Input Width:	Less than 10 ns.

OUTPUT CHARACTERISTICS

Signal Levels:	Standard negative TTL logic levels; logical "1" ≤ 0.4 volts; logical "0" $> +2.5$ volts.
High Level Drive Capability:	50 mA at +2.5 volts (compatible with terminated, direct-coupled 50Ω cable.)
Low Level Clamp Capability:	100 mA at 0 ± 500 mV (60 standard TTL loads, or 50Ω to +5 volts).
Risetime and Falltime:	Less than 10 ns.
Output Duration:	Approximately equal to input duration.
Output Impedance:	Less than 5Ω .
Duty Cycle Limitations:	None.

GENERAL

Delay:	Approximately 12 ns.
Logic Polarity:	Two front-panel switches, each common to four channels, provides normal operation (logical "1" IN gives logical "1" OUT) or complementary operation.

TTL TO NIM SECTION

NUMBER OF CHANNELS

Eight.

INPUT CHARACTERISTICS

Input Signal:	Standard negative TTL logic levels (logical "1" = 0 to +0.8 volts, requires -1.6 mA max.; logical "0" = > 2 volts, requires $+100 \mu A$ max.)
Minimum Input Duration:	Less than 10 ns.
Input Protection:	± 5 A for $0.5 \mu s$, clamping at +7 and -1 volts.

OUTPUT CHARACTERISTICS

Signal Levels:	Logical "0", open circuit; logical "1", -16 mA.
Output Duration:	Approximately equal to input duration.
Risetime and Falltime:	Less than 3 ns.
Duty Cycle Limitations:	None.

GENERAL

Delay:	Approximately 6 ns.
Logic Polarity:	Two front-panel switches, each common to four channels, provide normal operation (logical "1" IN gives logical "1" OUT) or complementary operation.

MODULE CHARACTERISTICS

Packaging:	NIM single-width module; Lemo-type connectors.
Current Requirements:	+6 volts at 280 mA; +12 volts at 30 mA; -6 volts at 300 mA.

SPECIFICATIONS SUBJECT TO CHANGE

TECHNICAL DATA

LeCroy



NIM Model 821

Quad 100 MHz Discriminator featuring Common Veto and Rate Lite®

- Burst Guard
- High sensitivity -30 mV
- Output width 5 nsec to 1 μ sec
- Hybrid front-end
- Updating operation
- DPR <9 nsec
- Low time slewing <1 nsec
- High fan-out

The LeCroy Model 821 is a high performance Quad Discriminator incorporating the features requested by experimenters throughout the world. The reliability designed into the 821 is based upon LeCroy's experience with its last three generations of quad discriminators. Its advanced hybrid front ends afford high sensitivity and greater than 100 MHz counting rate capability. Output pulse width stability is excellent even at threshold. Each channel has its own threshold and width controls, five NIM outputs, 1 NIM output and a Rate Lite.® Threshold may be monitored at a front-panel test point.

Updating Operation The output duration of the Model 821 may be adjusted over the range 5 nsec to 1 μ sec. In the updating mode, a threshold crossing extends the output pulse duration by a time equal to the selected pulse width. If the second threshold crossing occurs within the 9 nsec double-pulse resolution, the unit will not respond.

Burst Guard Mode If, in a train of input pulses to a discriminator, the pulses are separated by less than the resolving time, the discriminator output will be extended until the falling edge of the last pulse in the burst. This is a particularly important feature in veto applications.

Rate Lite® is an indicator LED. It produces a flash for each discriminator firing. A stretching circuit allows single firings to be discerned.

Common Veto provides the option of inhibiting all channels simultaneously by application of a NIM fast pulse. This is an effective means of eliminating unwanted background early in the logic system.

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SPECIFICATIONS

NIM Model 821

QUAD DISCRIMINATOR

INPUT CHARACTERISTICS

Signal Input:	Threshold, -30 mV to -1000 mV; front-panel screwdriver adjustment (screwdriver included); 50 Ω protected to ±5 A for 0.5 μsec, clamping at +1 and -7 volts; reflections <1% for input pulses of 3 nsec risetime; stability <0.2%/°C over 20°C to 60°C operating range; offset 0 ±2 mV; threshold monitor has 10:1 ratio of monitor voltage to actual voltage, ±5%.
Bin Gate:	Slow gate via rear connector and rear panel ON-OFF switch; risetimes and falltimes approximately 50 nsec; clamp to ground from +5 inhibits; direct-coupled.
Veto:	Front-panel connector permits simultaneous inhibiting of all channels; 50 Ω; required NIM-level signal (>-600 mV); direct-coupled, must overlap leading edge of input signal; must precede input by approximately 5 nsec. Minimum width 5 nsec.

OUTPUT CHARACTERISTICS

Number of Outputs:	6, differential-type current source; 2 bridged normal pairs (0 mA quiescently, -16 mA during output; complementary: -16 mA quiescently, 0 mA during output).
Risetime:	<2.0 nsec.
Falltime:	<2.5 nsec, (slightly longer on wide output durations).
Width Stability:	<±0.2%/°C maximum.
Duration:	Internal switch permits choice of Update Only or Burst Guard Mode. Front panel LED indicates Burst Guard Mode. <i>Update Only Mode:</i> 5 nsec to 1 μsec, continuously variable up to 600 nsec via front-panel screwdriver control. (Narrower widths possible at slight expense of amplitude). <i>Burst Guard Mode:</i> Output duration is either equal to the time-over-threshold of the input signal or equal to the preset duration, whichever is greater. For input burst rates greater than the DPR of the unit, the output is equal to the duration of the burst.

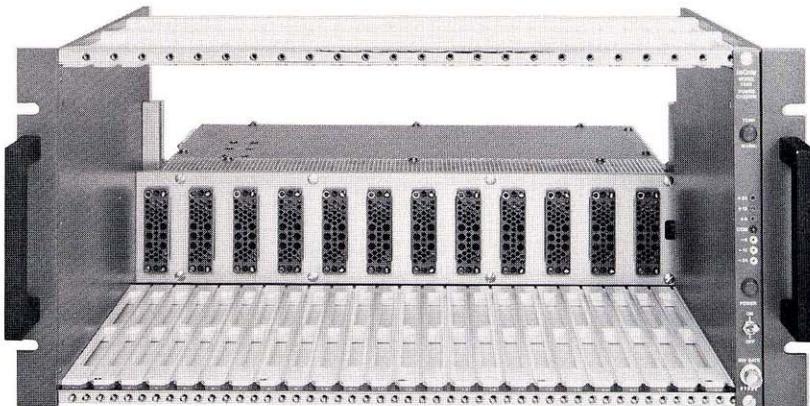
GENERAL

Maximum Rate:	110 MHz typical, input and output.
Double-Pulse Resolution:	Less than 9 nsec.
Time Slewling:	<1 nsec for input amplitudes 110% of threshold and above.
Input-Output Delay:	9.5 nsec. typical.
Multiple-Pulsing:	None; one and only one output pulse of preset duration is produced for each input pulse regardless of input pulse amplitude or duration.
Rate Lite®:	One per channel. Indicates discriminator output. 10 msec stretching employed.
Packaging:	In RF-shielded AEC/NIM #1 module (AEC Report #TID-20893); Lemo-type connectors.
Current Requirements:	-6 V @ 690 mA +6 V @ 230 mA -12 V @ 170 mA +12 V @ 15 mA - 24 V @ 85 mA

SPECIFICATIONS SUBJECT TO CHANGE

Model 1403 High Power NIM Chassis Model 1002A Super NIM Supply

- 200 W maximum power output
- Bus bar power distribution
- 1 mV rms ripple
- Thermal protection
- Short circuit proof
- Overvoltage protection on all supplies
- Heavy duty chassis

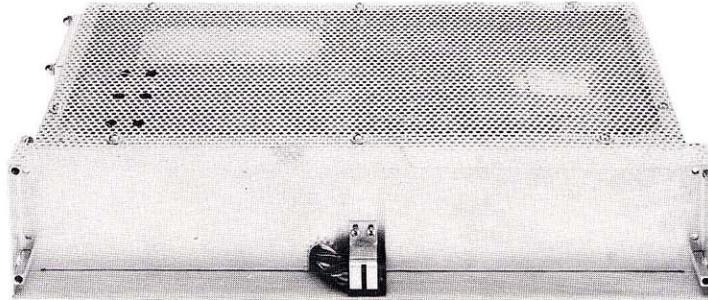


Model 1403 NIM Chassis

Modern experiments place ever increasing demands on the power capabilities of the NIM chassis. The LeCroy Model 1403 is a high power NIM chassis utilizing the LeCroy Model 1002A Super NIM Supply. The package provides high current versions of all voltages specified by the NIM standard: ± 6 V, ± 12 V and ± 24 V. The Model 1002A can supply up to 200 W in contrast to the 96 W specified by the NIM standard. Over voltage protection has been provided for all six supplies at levels which meet or exceed NIM standards.

The heavy duty NIM chassis employs cast metal rails, an improved mounting for the power supply, and printed power buses for distribution of all six supply voltages and ground. This minimizes resistive drops in the chassis which could lead to rate effects in analog circuits. Front panel test points are provided to monitor all six voltages.

Cool reliable operation of the Model 1002A power supply is assured by forced air cooling, integral to the unit. In the event of an over temperature condition, the supply shuts down. A warning of over temperature conditions is indicated by a pilot light on the front panel of the NIM chassis which is illuminated when the operating temperature comes within 30° F of the shut down point.



Model 1002A Supply

SPECIFICATIONS

MODEL 1403 HIGH POWER NIM CHASSIS

MODEL 1002A SUPER NIM SUPPLY

OUTPUTS

Maximum Power: 200 W total of ± 6 V, ± 12 V, ± 24 V and 115 VAC.
Maximum Current:
10 A, + 6 V
10 A, - 6 V
6 A, + 12 V
6 A, - 12 V
2 A, + 24 V
2 A, - 24 V
1 A, 115 VAC

PERFORMANCE

Ripple: 250 μ V rms (10 KHz bandwidth), 3 mV peak-to-peak (50 MHz bandwidth).
Regulation: $\pm (0.01\% + 0.5 \text{ mV})$ line or load (measured at the voltage sense leads).
Temperature Coefficient: <100 ppm/ $^{\circ}$ C.
Long Term Stability: <0.1 %/24 hours at constant load temperature. Measured after 1 hour warm-up.
Response Time: Settles to within 0.1% of final value in less than 50 μ sec for 10% to 50% load change.

GENERAL

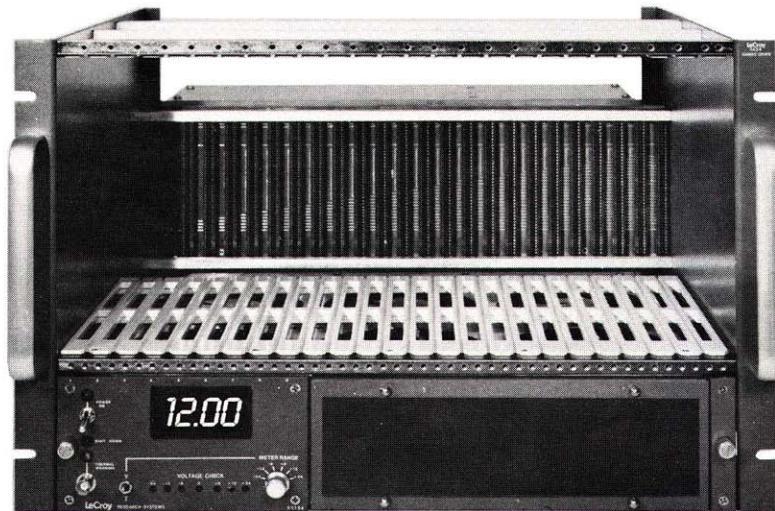
Over Current Protection: Protected against overload by current limit circuit; short circuit proof.
Over Voltage Protection: The 6, 12 and 24 volt supplies will not exceed 7.5, 16 or 33 volts (respectively) for longer than 100 msec.
Thermal Protection: Thermal sensor in Model 1002A shuts down supply in the event of thermal overload. Front panel thermal overload light indicates warning of an over temperature condition. Warning light operates at $210^{\circ} \pm 10^{\circ}$ F. Shutdown occurs at $240 \pm 10^{\circ}$ F.
Operating Range: 5 $^{\circ}$ C to 60 $^{\circ}$ C. Derate output current 2%/ $^{\circ}$ C from 50 $^{\circ}$ C to 60 $^{\circ}$ C.
Input Voltage: 115/230 VAC \pm 12%.
47 to 65 Hz.

SPECIFICATIONS SUBJECT TO CHANGE

Model 1434

Heavy Duty CAMAC Crate

- **High Power:** 450 W output
- **High Cooling Capacity:** 6 high flow fans
- **Digital Meter:** Displays all voltages and currents
- **High Capacity:** 75 A total from ± 6 V
- **Soft Turn On:** 10 msec runup
- **Overload Shut Down:** All supplies switch off
- **Short Circuit Proof**
- **Thermal Warning**
- **All Voltages:** Provides ± 6 V, ± 12 V, ± 24 V



The Model 1434 is a CAMAC Crate designed for applications involving a full crate complement of modules, especially if the modules have a high power dissipation. Because of its high power rating and high cooling capacity, the 1434 is recommended for those applications where system reliability is a major consideration.

The Crate employs the Model 1034P Super Power CAMAC Supply which provides up to 450 W and contains a fan to assure cool reliable operation. It supplies the standard ± 6 V and ± 24 V as well as the optional ± 12 V (derived from ± 24 V). Either of the 6 V outputs can provide up to 50 A, limited to 55 A, up to a total of 75 A shared. The 1034P also contains high capacity ± 12 V and ± 24 V supplies.

The power supply contains convenience features which add to the utility and versatility of the crate. At turn on, the supplies ramp up in the correct ratio. Runup takes about 10 msec. This can be a significant factor in preventing premature module failures. The supply contains overload detectors and cannot be damaged by a short circuit. In the event of an overload, all outputs are shut down together. This eliminates the risk of damage to modules caused by the voltage foldback of a single supply as with individual current limit circuits. A temperature sensor within the supply detects an over temperature condition. This sensor turns on a warning light and generates a TTL low level, which can be wire OR'ed, at a front panel BNC connector.

The high power output of the supply is matched by high capacity forced ventilation to provide cooling for the modules. Six fans, each rated at 127 CFM, provide an air flow far in excess of that recommended by the CAMAC standard.

The mechanics of the Model 1434 have been designed for convenience and serviceability. Both the fan assembly and the power supply can be removed without removing the crate from the rack.

The CAMAC crate and Dataway meet all the requirements of the CAMAC standard. Cast aluminum guides and low insertion force connectors are employed to assure proper mechanical alignment, thus increasing the ease of module installation. A multilayer Dataway is employed.

SPECIFICATIONS

Model 1434

HIGH POWER CAMAC CRATE

OUTPUTS

Total Power:	450 W maximum ± 6 V, ± 12 V, ± 24 V combined.
± 6 V:	Up to 50 A from either supply. 75 A maximum total.
± 24 V:	6 A maximum each. Subtract current drawn by ± 12 V load.
± 12 V:	3 A maximum each. Derived from ± 24 V supply.

PERFORMANCE

Ripple:	<5 mV peak-to-peak (50 MHz bandwidth).
Regulation:	$\pm (0.01\% + 1 \text{ mV})$ line or load (measured at the sense leads).
Temperature Coefficient:	<100 ppm/ $^{\circ}\text{C}$.
Long Term Stability:	<0.1%/24 hours of constant load and temperature. Measured after 1 hour warmup.
Response Time:	Settles to within 0.1% of final value in less than 100 μsec for 10% to 100% load change.
Tracking:	During switch on all six output voltages rise together. Risetime 10 msec.

GENERAL

Overload Protection:	Protected against overload by current limit circuit; short circuit proof. All outputs switch off within 20 msec of overload.
Oversupply Protection:	All outputs are protected against transient oversupplies by high current transient suppressors. Any sustained oversupply will turn off all outputs within 20 msec.
Thermal Protection:	A thermal sensor shuts down the supply in the event of a thermal overload. A front panel thermal overload light indicates an over-temperature condition. Remote indication of an overload is provided.
Operating Range:	Full 450 W output from 0 $^{\circ}\text{C}$ to 50 $^{\circ}\text{C}$ ambient temperature.
Meter:	3½ digit meter provides monitoring of all output currents and voltages. Accuracy $\pm 1\%$ of full scale voltage; $\pm 2\%$ of full scale current. Resolution better than 0.5%.
Input Voltage:	100/115/230 VAC $\pm 12\%$ 47 to 65 Hz.
Dimensions:	19" rack mount, 12½" height, 20⅞" depth.

ORDERING INFORMATION

Model No.	Description
1434	Complete Crate Assembly. Includes supply and fan tray
1034P	Power Supply Only
1034F	Fan Tray Assembly

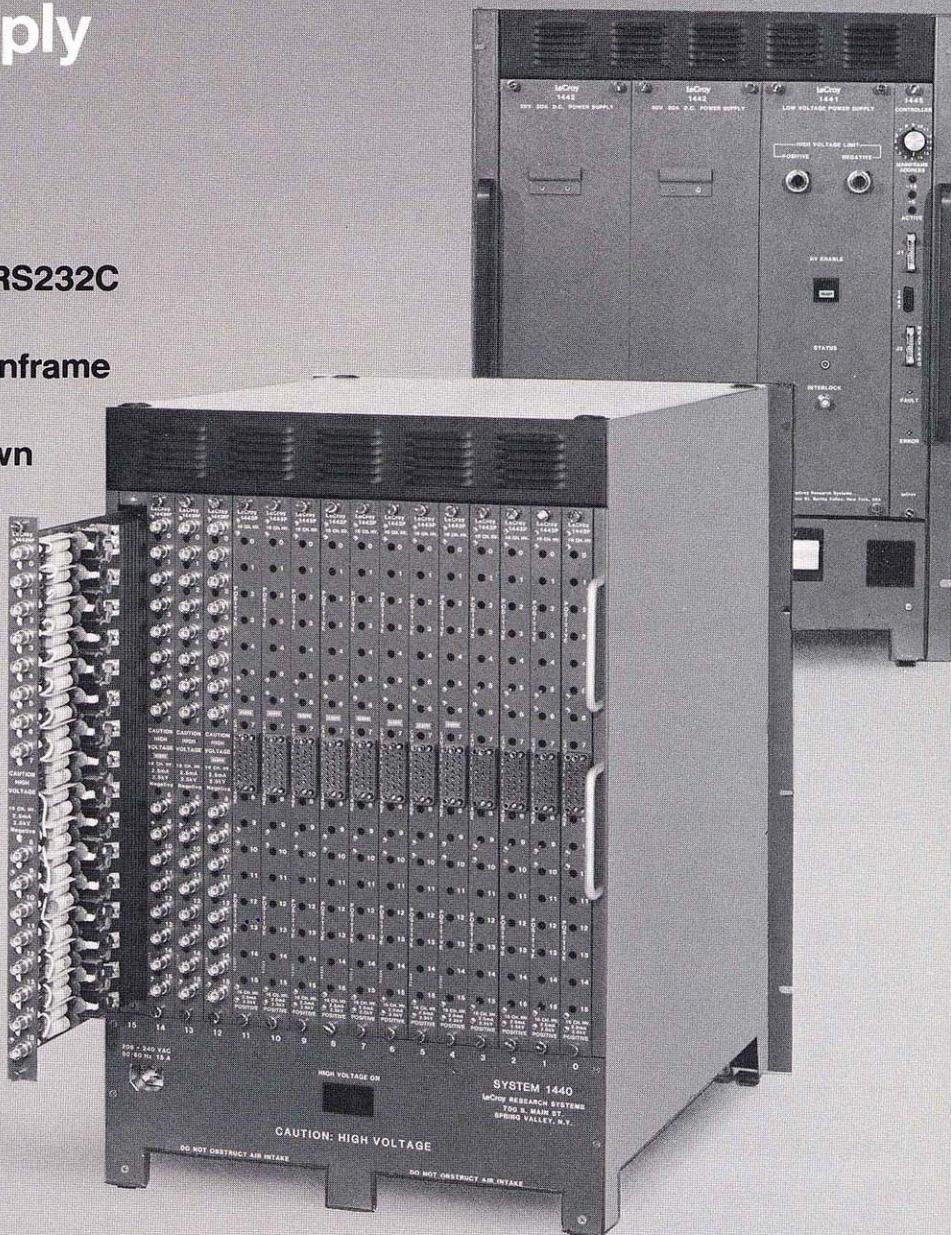
SPECIFICATIONS SUBJECT TO CHANGE

System 1440

June 1984

Programmable Multichannel High Voltage Supply

- 256 Channels per mainframe
- Remote control via CAMAC or RS232C
- Lowest cost per channel
- POS/NEG modules in same mainframe
- ± 2500 V, 2.5 mA per channel
- Slow HV ramp-up and ramp-down
- Output voltage set:
0.375, 0.5, 0.625, or 1 V steps
- Short-circuit and arc protected
- Panic OFF button
- TTL system interlock
- HV status output
- 12-bit voltage programmability



LeCroy

System 1440

GENERAL DESCRIPTION

System 1440 is a multichannel programmable high voltage system designed for large scale applications where high reliability and performance are most important. The system provides up to 256 channels of high voltage in each 1440 chassis, or 4096 channels, may be controlled and monitored via a single daisy chain. Control may also be done from CAMAC via the LeCroy Model 2132 CAMAC/HV interface.

System 1440 employs high efficiency switching supplies. As a fourth generation design, the HV supplies offer cool and reliable operation. The system reliability is further enhanced by the design of the mainframe which provides excellent cooling and a minimum of interconnects.

Convenience, versatility and servicability have been achieved through the use of modular construction. The microprocessor circuit, the power unit, two 31 V DC supplies and up to sixteen 16-channel HV supplies plug into the 1449 mainframe. As a result, the system can provide negative outputs, positive outputs or both. Systems of less than 256 channels may be easily established. A more economical low power chassis, model 1449E, is also possible for those applications which require less than the full power output of the unit. For details, see the ordering information listed below.

System 1440 provides many features to protect its costly loads against HV damage. The HV run-up and run-down rates may be selected by a jumper option on the control unit. Rates of 0.5 - 3.0 KV/sec are available. Rapid shutdown (panic off) of all channels is provided locally by a push-button and

also from a remote sensor via TTL System Interlock input. The 1449 chassis provides a clamp-to-ground output to indicate that the HV is on. The 1443/12 HV module provides an interlock to disable all 16 channels when the Card Interlock contacts are opened (available on block connector-type modules only).

The 1449 mainframe has two vernier potentiometers to provide separate hardware limits to set the maximum voltage output of the positive and negative channels. Two eight-bit registers are available to provide separate software limits to set the output current limit threshold of the positive and negative channels. The 1443/12 Series modules are available for both polarities. To avoid problems caused by the use of modules of the wrong polarity, the 1443/12 treats a demand voltage of the wrong polarity as a 0 V demand. As a second safeguard, output polarity indication is provided in the voltage monitor readback.

System 1440 contains a 13-bit ADC (12 bits plus sign) to allow the output voltage of all channels to be measured. The accuracy of the monitor is $\pm(0.1\% + 1.5\text{ V})$. The voltage programmability of the HV modules is 12 bits (plus sign).

The maximum output voltage available from the 1443/12 Series card is 2500 V. The full scale of the system programming may be jumper selected to be 2500 V, 2047 V, 1500 V and 4095 V (2500 V maximum allowable demand value). This allows the range and resolution of System 1440 to be matched to the experimental requirement.

FEATURES

Continuous Memory

Battery backup protects the integrity of internal memory for 24 hours. This makes the memory immune to occasional power failures. The batteries are continuously recharged whenever AC power is available.

Voltage Limit



Two front panel adjustments set hardware limits separately for positive and negative channels.

Panic Off



A front-panel pushbutton shuts down all supplies promptly. Protects against the unexpected.

Sophisticated Interactive TTY Operation

A simple, easy to understand mnemonic language allows all of the features of System 1440 to be exercised. This includes setting, measuring and adjusting any channel or all channels. The language offers iterative command execution similar to a Fortran DO Loop, allowing commands to operate on groups of channels. The system can offer a status report and print out an array of measurements of all outputs within the mainframe.



Each mainframe must be assigned a unique address. This allows commands to be referred to each chassis. Special shorthand allows the addressing to be skipped after the first reference. An RS232C type interface is employed.

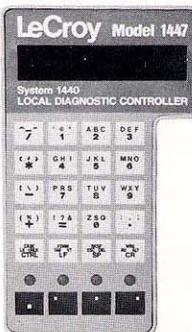
Thermal Protection

A temperature monitor on each of the low voltage power supplies shuts off the high voltage in the event of overheating. This can be the result of excessive loading, clogged fan filters, or high ambient temperatures.

Complete CAMAC Programmability

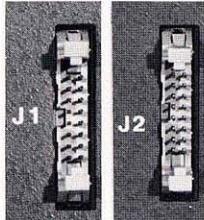
All the operations which may be performed from the TTY are available through the Model 2132 CAMAC interface. A simple binary control word scheme makes programming easy.

Hand Held Controller



Optional Model 1447 hand held controller allows local control of a 1449 chassis. By plugging the Model 1447 into the Auxiliary Control connector of the 1449 chassis, commands can be issued to the chassis without interruption of the other chassis in the control daisy chain.

Intelligent Daisy Chain



Up to 16 mainframes may be operated remotely. Serial Transmit and Receive lines are used. Also, an identifier line allows the system to differentiate between CAMAC and TTY modes. This allows for ASCII coding for TTY operation and binary coding for CAMAC operation. Binary coding greatly simplifies programming. The 1440 system automatically knows which remote device is active.

Digital Voltage Sensing

A system ADC reads the actual output voltage with 12-bit precision, NOT the demand setting. The output polarity is also reported.

PROGRAMMED COMMANDS

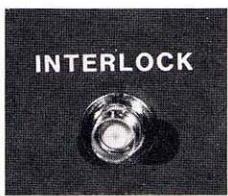
Demand Buffer Registers

The 1440 contains two 256 word voltage demand registers used for setting the output voltage. These words are 13-bits wide, comprised of 12-bits plus a sign bit. Although the standard HV modules employ 10-bit programming, the extra two bits are maintained to allow for optional higher precision 12-bit HV modules.

The two buffer registers are called the ACTIVE and BACKUP registers. Inclusion of two such registers gives System 1440 the ability to perform many useful operations. The system offers COPY (set Backup equal to Active) SWAP (reverse Backup and Active) and AUTOTRIM commands. Through these commands the following operations are possible:

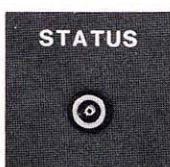
AUTOTRIM: Set Active register so ADC reading is equal to Backup value. Channels for which the resultant demand and measured output differ by $\geq 3\%$ are not trimmed and are loaded into an error list.

Interlock



A front-panel BNC input accepts a TTL input, triggering a panic-off. Internal programming jumper allows user assignment of logic levels, allowing the input to be used as a failsafe interlock or a remote panic off.

HV Status Output



A front-panel Lemo output used to indicate HV present at rear connectors. May be used for personnel safety interlocks or as an independent indicator.

Fault Indicator



A front panel connector signals a fault by a clamp-to-ground. A fault condition is generated by a failure of any of the DC power supplies. The most common causes are over-temperature or over-current conditions.

Error Indicator



A front panel Lemo connector used to indicate that all HV channels are operating within 3% of their demand settings. An error condition produces a TTL clamp-to-ground. Empty stations within the mainframe are ignored for this diagnostic. If the error is corrected, the Error Indicator output returns to its quiescent open circuit condition.

IDLE-DOWN:

Load slightly lower voltages into the Backup buffer and swap at Idle-Down time. Swap again to return to previous operating conditions.

SCRATCH PAD:

Copy the Active buffer into the Backup buffer. Perform any series of changes. A SWAP command returns the system to its original status.

Current Control Registers

The 1440 contains two current limit programming registers. One acts on all negative channels in the chassis. The other acts on all positive channels.

The current limit may be set to values appropriate for the detectors. Also, by lowering the current limit, and observing the output voltage, a crude measure of the current drawn from each channel can be obtained.

SPECIFICATIONS/Model 1449/1449E

HV CONTROL MAINFRAME

GENERAL

HV Modules/Mainframe:

Up to 16.

Channels/Mainframe:

Up to 256.

Max. HV Output Power:

1.6 KW for Model 1449.
800 W for Model 1449E. For each
1443/12 in excess of eight, deduct 15
W from the 800 W available.

DISPLAY

HV ON Indicators:

Yellow lamp indicates HV is enabled
for turn on, i.e., HV DISABLE is not
actuated and INTERLOCK is not
asserted. Integral with front panel HV
ON indicator (red lamp) and HV
DISABLE button.
Rear panel indicator lamp.

LVPS Status:

Two LED's indicate presence of -15 V and +5 V. Ready lit by +15 V.

System Active:

Front panel LED indicates 1443/12
Cards enabled for generating HV.
Normally on except when interlock
conditions occur.

CONTROLS

Power ON/OFF:

Rocker switch controls AC power.
Also acts as a circuit breaker.

Mainframe Address:

Front panel 16-position rotary switch
used to assign a mainframe address
for communication.

HV Limit Set:

Two front panel verniers set hardware
high voltage limits for negative and
positive output channels. Channel-to-
channel accuracy \pm 3%.

Current Limit:

Separate 8-bit registers for positive and negative HV modules. Allows limit setting of all channels in approximately 10 μ A steps up to 3 mA \pm 15%.

Programming Memory:

Two 13-bit voltage programming registers for each channel (12 bits plus sign).

Continuous Memory:

Programmed values are maintained in memory by rechargeable batteries: capacity 24 hours at 25°C.

Remote Mode Connectors:

2 dual 16-pin lock-and-eject type headers.

Hand Held TTY Input:

"D" type connector. When a controller is plugged into the hand held TTY input, the 1449 mainframe is controlled only from the TTY, however normal communications with the remainder of 1449 units via the normal controller is still available. Intended for use with Model 1447 hand held controller.

SAFETY

HV Enable:

Front panel pushbutton disables HV. Remote commands to turn HV ON are ignored until HV is re-enabled. Condition reported via status request.

Interlock:

TTL compatible input. Negative edge triggers HV disable. While the INTERLOCK is low, the READY indicator is off and remote HV turn on commands are ignored. Active state of INTERLOCK may be inverted by user via jumper. Condition reported via status request.

Status:

Clamp-to-ground when HV is present at outputs; high impedance when AC is off.

Fault:

Clamp-to-ground when fault is detected; high impedance when AC is off. Capable of sinking 25 mA from a 5 V source. Fault conditions include overtemperature, overcurrent or loss of regulation of internal supplies.

Error:

Clamp-to-ground when any installed channel is detected as being different from its programmed value by more than 128 counts.

MECHANICAL

Packaging:

19" rack-mount chassis, 17" wide \times 22" deep \times 26 $\frac{1}{4}$ " high. (Add 3" to depth to include handle protrusion.)

Input Power:

180-260 VAC/60 Hz
190-260 VAC/50 Hz

Ambient Humidity:

0 to 85% relative humidity.

Operating Temperature:

10 to 40°C ambient.

Shipping Weight:

210 lbs. (95 kg).

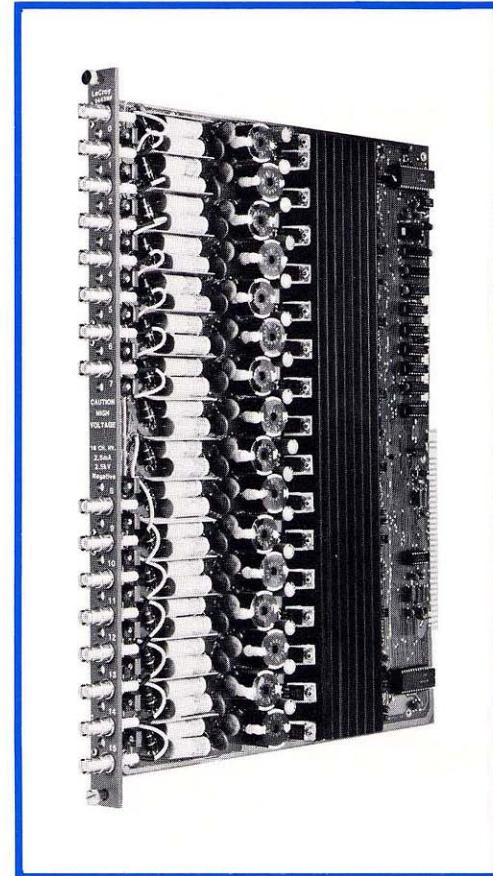
SPECIFICATIONS SUBJECT TO CHANGE



SPECIFICATIONS/Model 1443/12

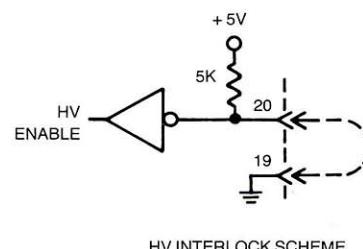
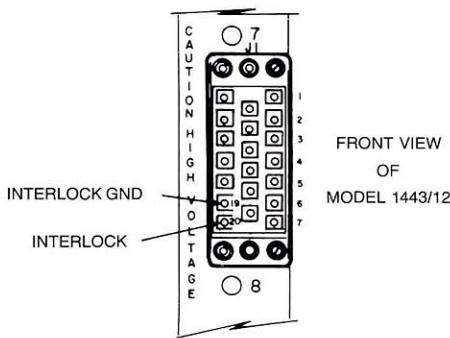
16-CHANNEL HV MODULE

Channels/Module:	16.
Output Voltage:	0 to 2500 V; \geq 500 V for rated performance. Polarity indicated by N or P suffix.
Voltage Regulation:	0.05% of full scale, line and load.
Full Scale:	2500 V, 2047 V, 1500 V; 4095 V also available (limited to 2500 V max.) mainframe jumper option.
Programming Step:	0.025% of full scale.
Programming Accuracy:	< \pm (0.5% + 2 V) for demand voltages $>$ 500 V.
Programming Reproducibility:	< 1 V at a constant load and temperature after 10 minutes warm up.
Voltage Monitor Accuracy:	\pm (0.1% + 1.5 V) channel-to-channel.
Monitor Long-Term Stability:	< 1.5 V/wk at constant load and temperature.
Output Long-Term Stability:	< 2 V/wk at constant load and temperature.
Monitor Temperature Coefficient:	Typically 0.005%/°C. Max., 0.01%/°C from 500 V to 2500 V (10°C to 40°C ambient).
Output Ripple:	Typically < 50 mV peak-to-peak; < 250 mV peak-to-peak maximum.
Current Output:	Up to 2.5 mA per channel.
Output Protection:	Fully protected against arcs at load, short circuit and overload.
Output Connector Type:	Multiconductor block-type connectors. SHV connectors specified by F suffix.



CONNECTOR DATA

PIN-OUT DATA



PIN ASSIGNMENTS

Pin	Function	
1	HV Output Channel	0
2	HV Output Channel	1
3	HV Output Channel	2
4	HV Output Channel	3
5	HV Output Channel	4
6	HV Output Channel	5
7	HV Output Channel	6
8	HV Output Channel	7
9	HV Output Channel	8
10	HV Output Channel	9
11	HV Output Channel	10
12	HV Output Channel	11
13	HV Output Channel	12
14	HV Output Channel	13
15	HV Output Channel	14
16	HV Output Channel	15
17	Ground Return	—
18	Ground Return	—
19	Interlock (short to 20 for enable)	—
20	Interlock (short to 19 for enable)	—

CONNECTORS

LeCroy Model HVCK20FB Female bulkhead type (used on 1443/12 front panel).
LeCroy Model HVCK20MB Male bulkhead type.
LeCroy Model HVCK20FC Female cable type.
LeCroy Model HVCK20MC Male cable type (mates with 1443/12 front panel).

ORDERING INFORMATION

Mainframe 1449/1449E

To order a System 1440, it is first necessary to determine the total HV power required for the application. For those systems requiring less than 256 channels or those requiring less than full voltage and current, the low power mainframe, 1449E, may suffice. If not, order the Model 1449 mainframe. Both versions include all logic and control units required for use with up to 256 HV channels. The 1449 provides a total of 1.6 KW to the 1443/12 HV cards. The Model 1449E provides 0.8 KW. For each 1443/12 card in excess of eight, 15 W must be deducted from the available 1449E power.

Example: A system consisting of 176 channels, operating at 2 KV, each with a load of 2 mA must provide $176 \times 2 \text{ KV} \times 2 \text{ mA} = 704 \text{ W}$. Since 11 cards are required, 755 W are available from the 1449E so the lower priced 1449E may be selected.

If the 1449E must be upgraded for 1600 W operation, a Model 1442 DC Supply must be ordered. The time required to install and test the addition is less than 1 hour. No special tools are required.

Sixteen Channel HV Modules 1443-Series

HV modules provide 16 outputs of up to 2.5 mA at 2500 V. Modules of positive and negative output are available and are denoted by P and N suffixes, respectively.

The HV modules employ front panel block connectors for the sixteen HV outputs. Also available is the SHV connector by specifying an F suffix.

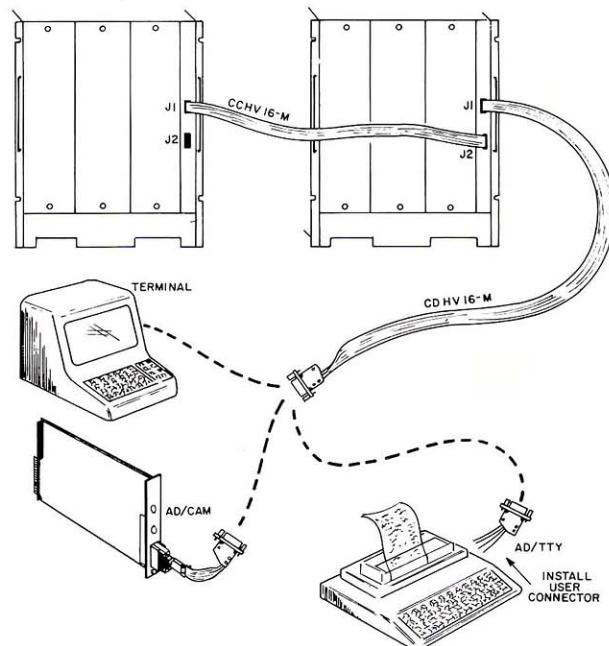
The standard versions of the 1443/12 employ 10-bit programming of the voltages.

Modules which accept 12-bit programming are available by special request. For details, consult the factory.

Model 1443/12	Negative, block connector
Model 1443/12	Positive, block connector
Model 1443/12	Negative, SHV connectors
Model 1443/12	Positive, SHV connectors
Model 1440X	Extender for 1443/12 Series HV module and 1445 microprocessor unit. Intended as a service tool.
Model 1441	Power module. Spare part. Included in 1449-Series.
Model 1442	DC supply. Included in 1449-Series.
Model 1445	Microprocessor unit spare part. Included in 1449-Series.
Model 1447	Hand held TTY.
Model 2132	Interface to CAMAC.

Accessories

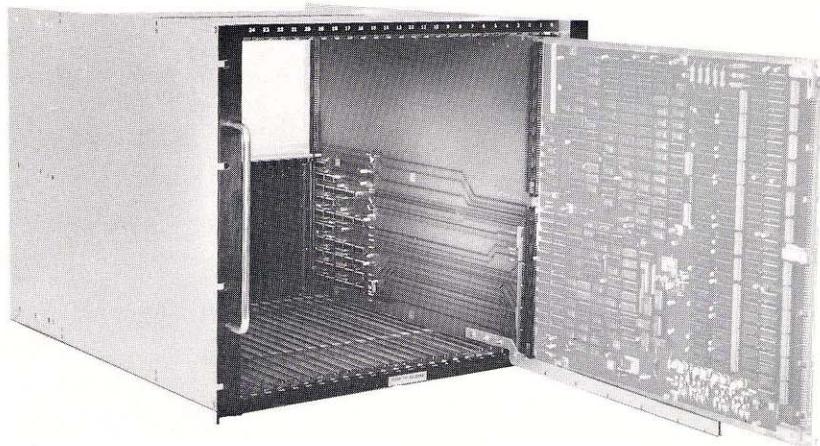
CCHV16-M	A data cable used to connect the 1440 chassis to each other. M is the length of the cable in meters.
CDHV16-M	A data cable used to connect the 1440 chain to a controller. A standard RS232C twenty-five pin "D" connector is employed at the controller end. M is the length of the cable in meters. See below for "D" to adapter options.
AD/TYY	Mates with CDHV16 cable. Provides pigtailed suitable for direct connection to a Teletype.
AD/CAM	Mates with HVDC16 cable. Provides the correct connector for connection to the Model 2132 Interface to CAMAC.



Model 1801 FASTBUS Active Extender

- **FASTBUS standard**
- **Buffered logic**
- **Master or slave**
- **Fused power lines**

The Model 1801 is a FASTBUS Active Extender designed as a service tool for use in FASTBUS crates. It provides an electrical and mechanical extension of a FASTBUS module, allowing it to be operated externally to the crate. This aids test and service of any FASTBUS module.



The Model 1801 provides extension for all of the 130 FASTBUS lines as well as 2 × 65 pins of Auxiliary Connector. All supply voltages and Reserved lines are fused (10 A). All of the high speed logic lines are buffered so that no impedance mismatch and no excessive bus loading result from use of the extender. The Model 1801 may be installed in the crate without a FASTBUS module in it with no loss of crate performance.

SPECIFICATIONS

Model 1801

ACTIVE EXTENDER

Hardwired Extension:	Daisy chain (6), FP0-FP3, UR0, UR1, TX, RX, AL0-AL5, GA0-GA4, Grounds, Reserved lines.																				
Fused:	All voltages and Reserved lines have 10 A fuses.																				
Buffered Input:	AG, AI, BH to card																				
Buffered Outputs:	AR, GK, to segment																				
Bidirectional Buffers:	TR0-TR7, WT, SR, RB																				
Directed Bidirectional Buffer (Type 1):	AD0-AD31, MS0-MS2, AS, DS, RD, EG, TP, PE, PA (see below).																				
Directed Bidirectional Buffer (Type 2):	DK, AK, SS0-SS2. Opposite sense of Type 1 (see below).																				
Directed Buffer Sense:	<table><thead><tr><th>GK</th><th>RD</th><th>Type 1</th><th>Type 2</th></tr></thead><tbody><tr><td>0</td><td>0</td><td>IN</td><td>OUT</td></tr><tr><td>0</td><td>1</td><td>OUT</td><td>IN</td></tr><tr><td>1</td><td>0</td><td>OUT</td><td>IN</td></tr><tr><td>1</td><td>1</td><td>IN</td><td>OUT</td></tr></tbody></table>	GK	RD	Type 1	Type 2	0	0	IN	OUT	0	1	OUT	IN	1	0	OUT	IN	1	1	IN	OUT
GK	RD	Type 1	Type 2																		
0	0	IN	OUT																		
0	1	OUT	IN																		
1	0	OUT	IN																		
1	1	IN	OUT																		
Propagation Delay:	<10 nsec																				
Power:	<2 A at -5.2 V <1 A at -2 V																				

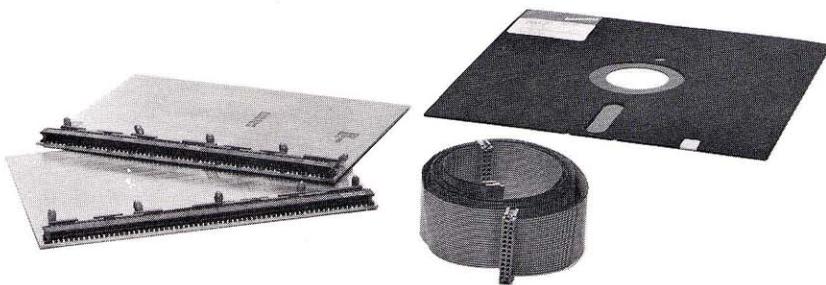
SPECIFICATIONS SUBJECT TO CHANGE

TECHNICAL DATA

LeCroy

Model 1805 FASTBUS Starter Kit

- FASTBUS versatility
- Interface to CAMAC
- Allows all data transfer and control operations
- Sample software



The Model 1805 is a FASTBUS Starter Kit, providing all the equipment required for a CAMAC link to FASTBUS. Although the 1805 does not provide the speed of FASTBUS, it does offer the versatility of the standard. It is intended to allow FASTBUS modules to be read out, written to and controlled via CAMAC, thus providing experience with FASTBUS and allowing for the first use of the standard. The Model 1805 includes the following items:

Model 1822 is a FASTBUS register providing read and write functions for both the FASTBUS protocol and data (A/D) lines. These operations are provided via a front panel control input from the Model 2891.

Model 2891 is a CAMAC register intended as a link to the Model 1822 (and to the Model 1821). In conjunction with the Model 1822, it allows any FASTBUS protocol sequence to be generated under software control. Also, the pair allows data to be written to or read from FASTBUS.

Model DC4-34/3 is a 3 m long cable used to connect the 1822 to the 2891.

Model 1802 is a FASTBUS terminator. Two are supplied for rear installation at each end of the FASTBUS crate backplane. It provides the levels for the Geographical Addressing lines but does not provide for crate arbitration.

Model 3910-40 is an RT11-formatted floppy disk containing sample FORTRAN programs to be used as an aid in constructing FASTBUS primitive and macro routines.

In addition to serving as a first introduction to FASTBUS, the 1822/2891 combination is a useful diagnostic tool in the long term. Also, the 2891 may later be used with the Model 1821 Segment Manager/Interface.

Preliminary
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FASTBUS Model 1810

Calibration And Trigger Module

- **Fan Out:** gate, clear, common stop
- **Programmable Time Resolution:** TDC, ICA oscillators
- **Calibration Facility:** ADC, TDC, ICA
- **FASTBUS Standard**

The Model 1810 is a FASTBUS module designed to accommodate the calibration and trigger functions of the System 1800 Data Acquisition Crate. The Calibration And Trigger module, CAT, may be placed in any slot of a standard FASTBUS crate. It receives and distributes the strobes required to operate the Data Acquisition Modules. The required clock signals and calibration pulses are also distributed from the CAT. The FASTBUS backplane is used for all of these operations.

The CAT may be downloaded with control words used to set the operating conditions for the DAM's, i.e., clock frequencies for the TDC and ICA modules. The CAT also accepts control words to set up the calibration pulses and levels for the DAM's. The charge to be applied to the ADC channels is 12-bit programmable. The times and pulse widths may be separately programmed for TDC channels. A second pulse may be enabled to test the compacting circuitry of the TDC. The ADC amplitude word and TDC timing pulse also program the calibration test pulser in the ICA.

The control words are loaded into Control Space Register and DATA space within the CAT. The write operations follow standard FASTBUS protocol with the Model 1810 acting as a SLAVE. During the write (and readback) operations, a yellow LED is illuminated on the front panel of the CAT.

To enable the CAT to process trigger strobes requires that the Acquisition Mode (AM) be established. The Crate Master, usually a Model 1821, gains mastership of the Segment from the Arbitration Timing Controller (ATC) and generates an AM broadcast. The CAT recognizes this operation, and 1800 DAM's within the crate are initialized for data acquisition. The CAT then uses the segment to transmit its signals to the DAM's. The TR lines are used in order not to compromise use of the crate during the AM.

The event time is defined as the earliest of the three system strobes (ADC Gate, TDC Common Stop and ICA Common Stop). The Measure Pause Interval begins at the event time and lasts for 0-63 μ sec. It is FASTBUS programmable. A Master may then begin read out of the DAM's. A Fast Clear pulse received at the CAT during the MPI restarts TDC and ICA clocks and applies a Fast Clear pulse to the ADC modules.

At the end of the MPI, the CAT provides the trailing edge of the Common Stop pulse. This action is used by the DAM's to initiate data conversion.

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SPECIFICATIONS

Model 1810

CAT MODULE

INPUTS

A Gate In:*	Defines the integrating time for the ADC's. Distributed to 1882, 1885 modules via the FASTBUS segment. Duration 50-2000 nsec. Begins the MPI.
T Common Stop:*	Minimum width 50 nsec. Stops the oscillator signals used to clock the pipeline TDC's. Begins the MPI.
I Common Stop:*	Minimum width 50 nsec. Stops the oscillator signals used to clock the ICA's. Begins the MPI.
ATI Fast Clear:*	Minimum width 50 nsec. Distributes fast clear signal to ADC modules, restarts the TDC and ICA oscillators and terminates the MPI.
TI Personality Card Strobe:*	Minimum width 50 nsec. Supplies a pulse to the personality cards to define the event time. Not used by the DAM's.
TI Test In:*	Minimum width 50 nsec. Applies timing pulses to the TDC and ICA DAM's. Used in conjunction with the Common Stop inputs.

OUTPUTS

AI Level:	Output via a Lemo connector. Supplies 0 to + 10 V DC level used to program the ADC and ICA pulsers. Output impedance 1 KΩ.
MPI In:	Bidirectional port used to synchronize the MPI's in all crates. Provided via two identical Lemo connectors. Bidirectional current sink: output – 28 mA at – 1.4 V; input 50 Ω, – 1.4 V to enable. When daisy chained, the duration of the MPI at all CAT's in the daisy chain is equal to the duration of the longest MPI in the chain.
MPI Out:	
Busy Mode:	A NIM false level indicates that the crate is in the AM. NIM True indicates a trigger has been received.

DATA ACQUISITION CONTROL

I/T Osc Frequency:	A 7-bit programmable divide down factor covering a factor of 2 (Data Space).
--------------------	--

CALIBRATION CONTROL

ICA:	TBA.
TDC:	Programs the time of the trailing edge of a time pulse, and the time of the stop pulse (Data space). Also enables and disables a second pulse approximately midway between pulse 1 and the Common Stop (CSR Space).
ADC:	A 12-bit amplitude word. Sets the amount of charge injected into each ADC when the test feature is enabled (Data Space).

GENERAL

Power Requirements:	50 mA at + 15 V 1.0 A at + 5 V 4.0 A at – 2 V 6.5 A at – 5.2 V 1.00 mA at – 15 V
Packaging:	Single width FASTBUS module in conformance with FASTBUS specification dated December, 1983.

FASTBUS CONTROL

Implemented Addressing Modes:	Geographical, Secondary, Broadcast	
Implemented Broadcast Functions:	Code $(0D)_h^{**}$	Significance All device scan
	$(8D)_h$	Comments The 1810 asserts its "T pin" on following rea cycles.
Slave Status Response to Data Cycles:	SS 0 6	AM Valid action Error, data rejected
		Begins acquisition mode.

CONTROL FUNCTIONS IMPLEMENTED

Module Identification Code:	(Read only) $(1038)_h$
Test Pulse:	Disable, enable one pulse, enable double pulse
Cal Trigger:	NIM pulse signifying that the crate has entered the acquisition mode—typically 85 nsec.

*Two inputs, one bridged high impedance Lemo pair accepting NIM inputs, and one 110 Ω impedance two-pin header accepting differential ECL inputs.
**An h subscript denotes a hexadecimal number, i.e., base 16.



FASTBUS Model 1821 Programmable Segment Manager/Interface

- 1800 Data Acquisition Scanner
- Interface via Personality Cards:
CAMAC, ECLbus, UNIBUS®, etc.
- FASTBUS Module Tester
- Event Builder
- Sparse Data Scan
- All FASTBUS Operations
- Full FASTBUS Speed
- Programmable

The Model 1821 is a programmable FASTBUS module designed to provide operations on the Segment at the full speed of the standard. The device can be programmed to act as a Slave, a Master or as a Snoop. The 1821 provides two sections, the Sequencer and the Interface.

The Sequencer within 1821 operates under the control of its micro-program, executing one instruction every 33 nsec. The instructions have multiple fields, typically allowing five operations to be performed at once. The unit offers complete exercise of the FASTBUS protocol lines allowing any FASTBUS operation or series of operations to be programmed. The program word includes a branch operation based upon a wide variety of possible conditions including SS, MS and the data on the AD lines. This branching feature allows the Model 1821 to execute programs with Loops.

The Sequencer offers complete FASTBUS arbitration logic. It also provides hardware for a sparse data scan based upon the T-pins.

Data may be written to the FASTBUS AD lines either from the program word or from the Interface. Data may also be read from the AD lines and either used by the Sequencer or transmitted to the interface section. The Sequencer does not provide arithmetic operations on the data.

The Interface of the Model 1821 provides hardwired pedestal subtraction and threshold comparison. Both features can be enabled by the Host computer. The Interface offers a 8K x 10 pedestal memory and a 4K x 32 data memory. Data from the Sequencer may be pipeline processed at a 10 megawords/sec rate. The information is applied at the FASTBUS Auxiliary Connector as it is loaded into the data memory. In this way, the Host can address the data memory, or datawords may be pipeline transferred out of the 1821 to another device such as the 1891 FASTBUS Multiple Event Buffer.

The Interface is connected to an intelligent Host via an interface personality card. The FASTBUS Auxiliary Connector is employed for this purpose. Personality cards allowing connection to the Model 1891 Multiple Event Buffer and to a PDP11 UNIBUS Interface (DR11W) are available. A front-panel connector on the Model 1821 provides for connection to a CAMAC Interface, Model 2891. For details on interconnection, see LeCroy Application Note AN28.

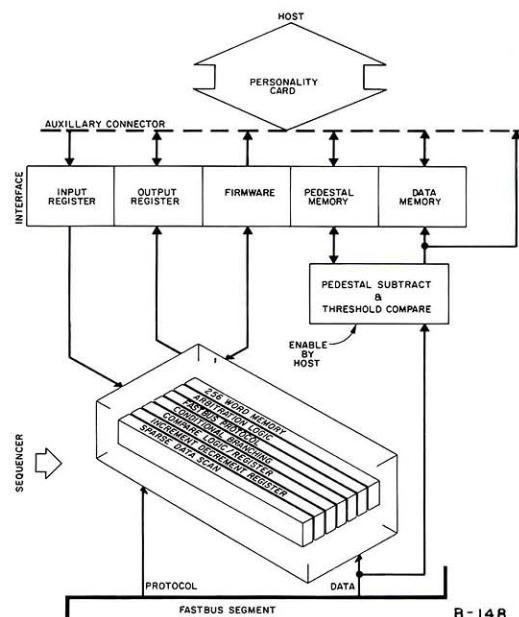
The 1821 may be user programmed; however, firmware within the unit allows the most common FASTBUS primitives and macros to be executed by simple calls from the Host. Many operations can be executed by a single call; however, the 1821 provides for executable lists also.

Extensive firmware is provided for use with LeCroy's 1800 Series of FASTBUS data acquisition modules. In addition, to set up operating parameters and automated test of the crates, the 1821 provides ordered readout of 1800 Series ADC's, TDC's and ICA's.

The Model 1821 has four Menu PROM's, each containing a series of functionally grouped FASTBUS operations. One PROM provides crate checkout and startup operations, another contains CSR setup routines, another data acquisition, another calibration. Any one of the PROM's may be loaded into the Sequencer's memory under control of the Host computer in < 1 msec. Thereafter, any of the routines in the PROM may be called and executed.

Control words transferred from the Host to the 1821 are used for setup. This allows data compaction and pedestal subtraction to be enabled, it allows Sequencer programs or firmware to be uploaded or downloaded to or from the Host or from the Menu PROM's.

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SPECIFICATIONS

FASTBUS Model 1821

PROGRAMMABLE SEGMENT MANAGER/INTERFACE

CONNECTORS

Personality Connector:

Uses FASTBUS Auxiliary Connector. Intended for interface to the Host. TTL logic. Provides 16-bit data field, 3-bit address and two strobes; read and write. Access time <300 nsec. Also 32-bit data in/out field presented at rates up to 10 MHz. See the I/O Circuit Diagram below.

Sequencer Monitor:

Front panel 34-pin ECL connector. Provides monitor of the operation of the Sequencer. Interface Monitor:

IN1, IN2, IN3:

Differential ECL inputs via 2-pin ECLline connectors. Used as real time conditions for the 1821 Sequencer. Operations depend upon software. Minimum duration 30 nsec.

OUT1, OUT2, OUT3:

Differential ECL outputs via 2-pin ECLline connectors. Driven under software control.

GENERAL

Packaging:

Standard double width FASTBUS module in conformance with FASTBUS Working Group Document dated June 9, 1982.

Power Requirements:

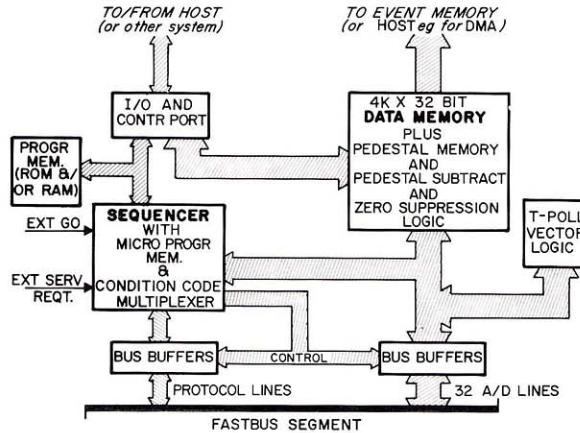
5 A at +5 V
13 A at -5.3 V
7 A at -2 V

Accessories:

Model 2891: CAMAC Interface

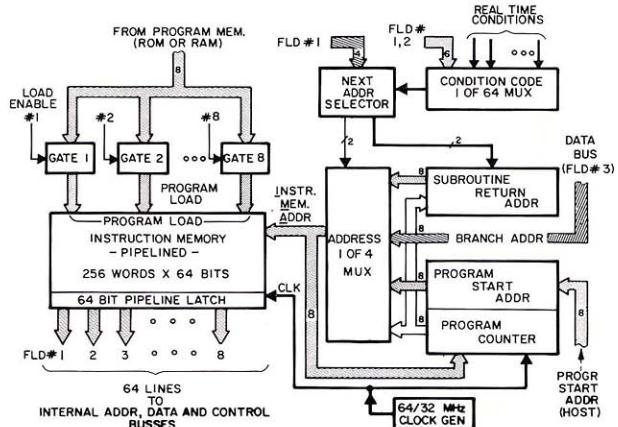
Model DC4/34-m: Connecting cable for 2891; Here m is length in meters.

Model 1821/DEC: Personality card for the DR11W UNIBUS Interface.



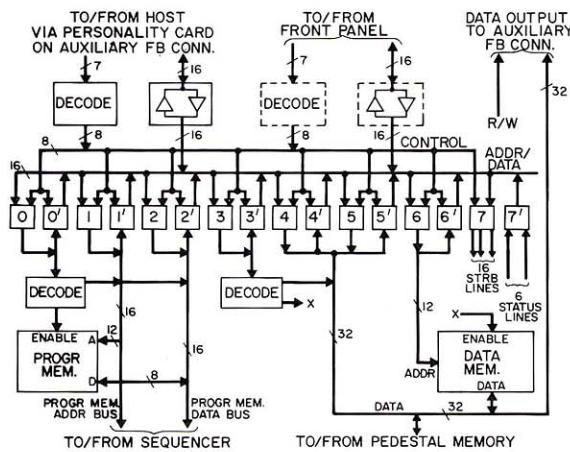
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Simplified Block Diagram



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Block Diagram Sequencer



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I/O Circuit

SPECIFICATION SUBJECT TO CHANGE



FASTBUS Models 1878 and 1879 96 Channel Pipeline TDC

- Multihit Capability
- FASTBUS Readout: 10 x CAMAC
- Programmable Gain
- Pulse Width Encoding
- Test Feature: FASTBUS controlled
- Trigger Processor Connection: via Auxiliary Connector

Designed to provide multihit time-to-digital conversion, the FASTBUS Models 1878 and 1879 are 96 channel Pipeline TDC's. The Model 1879 provides a 10-bit time readout format (nine bits plus stop phase), allowing for resolution to below 1 nsec. The Model 1878 provides a 9-bit format (eight bits plus stop phase). The units operate in a Common Stop mode, eliminating the need for delay cables normally required for each input when used with fixed target machines.

The TDC's are designed for use in a standard FASTBUS crate. The optional Model 1810 CAT module may be used to provide the Calibration And Trigger signals employed by the TDC, however, operation without a CAT is also possible using the software-selectable front panel Common Stop and Fast Clear inputs. In this case, calibration must then be user supplied. The readout is in accordance with the FASTBUS standard. Readout can be via standard FASTBUS hardware (i.e., a Segment Interconnect or a LeCroy Model 1821 FASTBUS Segment Manager).

A low frequency crystal oscillator within the TDC or one within the CAT provides an accurate and stable frequency reference for the on-board oscillator. Programmable divide down ($x1$, $x1/2$, $x1/4$ and $x1/8$) within the TDC module allows the gain to be user selected. The on-board crystal may be used to provide stand alone operation. Alternatively, the programmable oscillator in the CAT may be user selected as the TDC reference frequency via CSR programming, providing frequency reduction range from $x1$ to $x1/2$ with 128 steps. This allows the full scale to closely match the drift time. The combination of the programmable divide down and the range of the CAT oscillator provides a full scale that is programmable from 1 to 16 μ sec.

The oscillator may be free run, eliminating the need for synchronization to the experiment. This mode is particularly useful for beam on target applications where no timing reference exists in advance of an event. A stop timing reference called the Phase Latch records the phase of the clock to a resolution of 1/2 of the time bin. For pulsed collider applications, a front panel ECL Sync Input may be used to synchronize the Acquisition Oscillator to the experiment. Either the Phase Latch or the Sync provide improved resolution to the time measurement.

Both TDC's employ a high speed, low power Silicon-On-Sapphire (SOS) shift register as the central element. This device, the MLL400, was pioneered at Brookhaven for the TDC application. The shift register divides the time interval to be recorded into a series of time bins. The 1878 employs a 250 MHz, 256 element shift register, and the 1879, 500 MHz, and 512 elements. When the MLL400s are shifted, chamber discriminator signals are loaded as 1s and 0s, thus recording the history of the drift gap. A Common Stop signal terminates the clock signals and begins the Measure Pause Interval. This is a CAT programmable duration of 1 to 63 μ sec, during which the TDC readout circuit holds off encoding. A Fast Clear causes the shift clock to restart, thus providing zero fast clear time. After the MPI, time encoding begins on the TDC card. A Fast Clear pulse received after the MPI requires clearing of the TDC modules and the readout. This operation requires 1.6 μ sec.

The hit detector in the TDC reports only the time of the edges of input pulses. Also, the pattern recognition circuits eliminate phantoms caused by chamber afterpulsing. A hit is suppressed unless it is preceded by an interval of null

input. The interval, called Z, may be programmed over the range 0-15 time bins (Z = 0 corresponds to the "All True Data" Mode). This readout circuit also filters out data from wires which are "stuck on".

To speed the encoding, the Models 1878 and 1879 are organized in six groups (hexants). Each is interrogated by its hit detector circuit. All six are controlled by a common sequencer so that six channels are encoded at once. Hits are encoded and stored in a leading edge 1024 word memory utilizing one word to record up to six simultaneous hits.

The TDC also contains a similar circuit operating on the trailing edge of the input pulse. Recording these times in conjunction with the leading edge times provides pulse width information. This allows software discrimination against narrow (noise) signals and also provides an estimate of the chamber pulse amplitude.

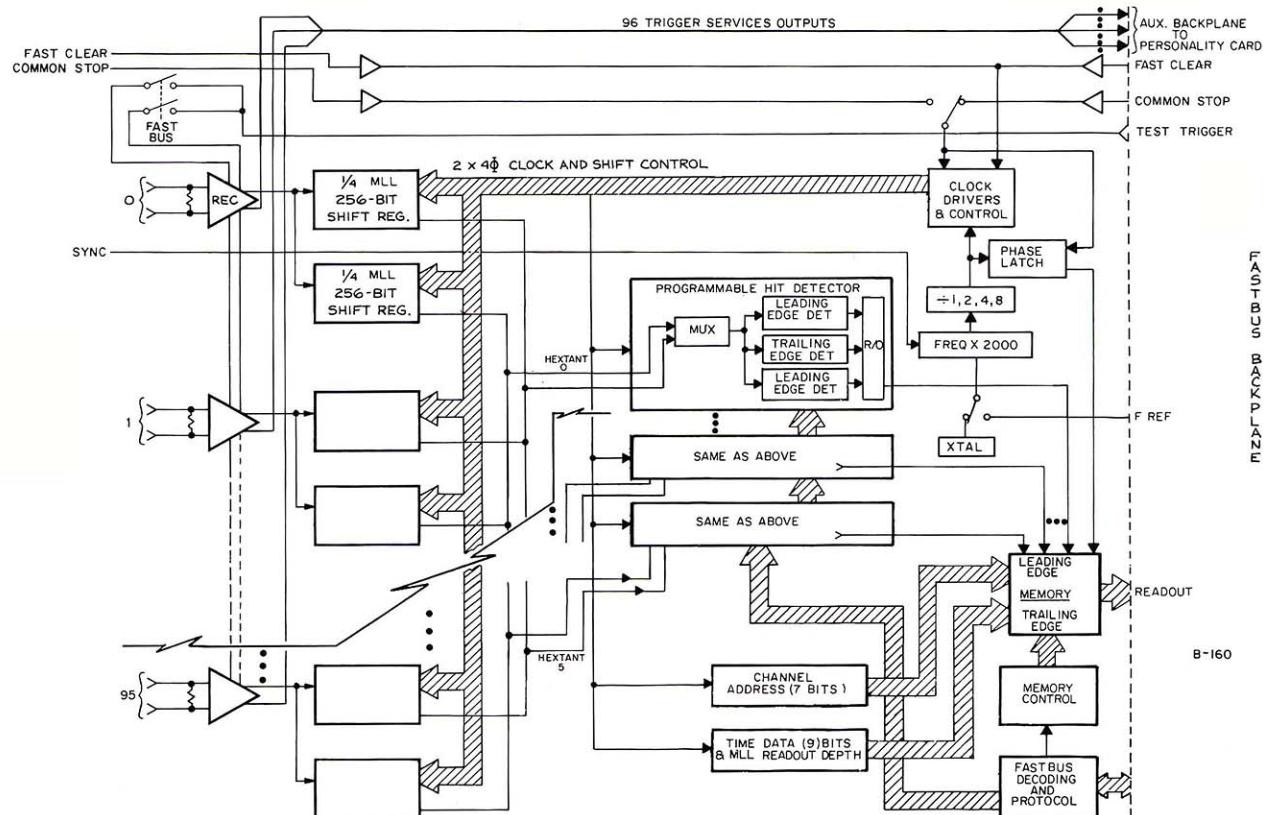
Encoding of the data requires 412 μ sec plus approximately 50 nsec per hit at full readout depth. This involves loading all hits into the 1024 word leading and trailing edge memories. Readout can then proceed at full FASTBUS speed. Datawords consist of a 7-bit address and 5-bit geographical address along with the time of the hit (9 bits for the 1879 and 8 bits for the 1878). One dataword is read out for each hit received. The memory organization is non-volatile, allowing an event to be read more than once if required.

In most cases, the data from a single event can be contained in a small fraction of the memory. Data is readout to FASTBUS in a first-in, first-out sequence. Successive datawords have been read, a SS = 2 "end of block" response is returned. This facilitates block transfer readout.

The TDC's provide self-test in conjunction with the CAT module. A programmable pulser within the CAT is provided, allowing the times of the leading and trailing edges of a test pulse to be user programmed via FASTBUS. A second pulse may also be enabled to test the double pulse response of the TDC's. The pulser signals are distributed to the TDC's via the FASTBUS segment. Two control bits within the CSR space of the TDC modules allow even and odd channels to be enabled separately on a card-by-card basis. The test circuitry allows the TDC channels to be checked for cross talk, to be calibrated, and their data compactors to be tested.

In order to allow the input signals to participate in the trigger, the FASTBUS Auxiliary Connector space is used for installation of an Auxiliary Functions Card (AFC). The 96 inputs are restandardized and applied to the FASTBUS Auxiliary Connector, allowing arbitrary user configured triggers to be established. By using the FASTBUS Auxiliary Connector and its card cage, integral to the crate, ease and convenience of cabling are achieved. When the trigger processor is connected to the rear of the personality cards, connections between the trigger processor and the data acquisition module are completed by inserting the module into the crate. Up to fourteen 14-bit locations may be user implemented on the AFC for trigger programming.

The 1878 and 1879 provide the high performance, high density, versatility, and automated test features required for large scale experiments. Use of the new FASTBUS standard has helped make the 1800 family of data acquisition modules one of the most sophisticated data acquisition systems.



SPECIFICATIONS

Models 1878/1879

96 CHANNEL PIPELINE TDC

Inputs:

Phase Latch Accuracy:

Least Count

(Phase Latch):

Model 1878

Model 1879

(Time Bin Size):

Model 1878

Model 1879

TDC Range:

Model 1878

Model 1879

Long Term Stability:

Full Scale:

Double Pulse Resolution:

Common Stop Trigger:

Sync Input:

96 ECL differential line receivers. Input impedance $110 \Omega \pm 10\%$. Minimum pulse width 10 nsec fwhm (must be >1 time bin width). Input swing ≥ 400 mV, differential.
 ± 200 psec or $\pm 10\%$ of time bin size, whichever is greater

2, 4, 8 or 16 nsec, CSR selected in stand alone mode. 2 to 31.5 nsec with Model 1810 (half time bin size).

1, 2, 4 or 8 nsec, CSR selected in stand alone mode. 1 to 15.5 nsec with Model 1810 (half time bin size).

4, 8, 16 or 32 nsec, CSR selected in stand alone mode. 4 to 63 nsec with Model 1810.
 2, 4, 8 or 16 nsec, CSR selected in stand alone mode. 2 to 31 nsec with Model 1810.

9 bits, 8 + Phase Latch

10 bits, 9 + Phase Latch

$\pm 0.02\%$

1, 2, 4 or 8 μ sec, $\pm 0.01\%$, CSR selected in stand alone mode. 1 to 16 μ sec with 1810.

3-15 bins programmable, Compacting Mode. 3 bins, "All True Data" Mode.

From the Model 1810 CAT Module via TR line or from front panel differential ECL input.
 CSR selected.

Differential ECL two pin input. Terminated in 100Ω . Minimum width 10 nsec. Quenches the Acquisition Oscillator for the duration of the input width. Acquisition Oscillator is active and stable after a time equal to 4 times the Sync pulse width. Synchronism is achieved with respect to the trailing edge of the Sync pulse. Sync accuracy: 0.1 time bins at start up. See Long Term Stability spec above. Recommended width: $(8 \pm 1/2)/f$. Here f is the Acquisition Oscillator frequency, i.e., input to the divide down circuit.

Channel-to-Channel Matching:

Gain:

Pedestal:

Differential Non-Linearity:

Integral Non-Linearity:

Pedestal Stability:

Fast Clear Response Time:

AS-AK Handshake Time:

DS-DK Handshake Time:

Digital Clear:

Conversion Time:

$<\pm 0.01\%$ card-to-card

$<\pm 4$ nsec channel-to-channel

<1 nsec, typical

$<\pm 0.5$ nsec or ± 0.25 LSB, whichever is greater

<100 psec/ $^{\circ}$ C, 1 nsec long term

<10 nsec. Must be performed during MPI. 50 nsec minimum width

30 nsec, typical

80 nsec, typical

1.6 μ sec

412 μ sec + approximately 50 nsec per hit

GENERAL

Power Requirements:

5 mA at 15 V

7.2 A at +5 V (Model 1879, 8.5 A)

4.2 A at -5.2 V

2.0 A at -2 V (Model 1879, 3.3 A)

50 mA at -15 V

Packaging:

Single width FASTBUS module in conformance with FASTBUS Specification dated December, 1983.

FASTBUS CONTROL

Implemented Addressing Modes:

Geographical, Secondary, Broadcast

Implemented Broadcast Functions:

Code **Significance**

(01)_h* General Broadcast Select

Comments

The TDC modules are selected and respond to subsequent data cycles.

(09)_h Sparse Data Scan (SDS)

TDC modules containing time data assert their "T pin" on the following read data cycle.

(09)_h Pattern Select

TDC's seeing their T pin asserted on the following write data cycle become selected to respond to subsequent data cycles.

(0D)_h All Device Scan

All TDC modules assert their T pin on the following read data cycle.

(AD)_h TDC SDS

Unique sparse data scan for only 1878 and 1879 modules. Follows standard SDS (see above).

(BD)_h AFC SDS

All TDC modules with AFC's requiring service assert their T pins.

Slave Status Responses
to Data Cycles:

SS **Significance**

0 Valid action.

1 Busy. The module is in the encoding mode and will not respond to data space read or write transactions.

3 Valid data space read with second event pending encoding.

2 End of data

6 Error. Non-implemented secondary address or invalid mode.

7 Error. Invalid secondary address loaded into internal address register.

*An h subscript denotes a hexadecimal number, i.e., base 16.

CONTROL FUNCTIONS IMPLEMENTED (CSR Space)

Module Identification Code:

Compacting Parameters (Z):

Read Only (1032)_h for 1878, (1033)_h for 1879.

A 4-bit programmable number of leading zeros which must precede a 0 to 1 transition to be recognized as a hit. To account for edge effects, all history before the first time bin is assumed equal (0 or 1) to the first bin. To allow a diagnosis of "stuck" channels, first bin reporting may be enabled via "Enable Bin 1" of CSR0. All True Data mode (Z = 0) reports every true bin.

Readout Depth, active time interval (ATI):

A 5-bit programmable time range for valid data. For 1878, the number of valid time bins is 8(ATI + 1). For 1879, 16(ATI + 1). The valid bins are those corresponding to the earliest times.

Calibration Enable (T_e and T_o):

Two bits enable the TDC to receive the test input via a TR line and apply it to the even and odd TDC channels, respectively.

Common Stop Source:

Selects the source of the Common Stop, either front panel or a TR line.

FREF Source:

Selects either the internal crystal frequency reference or a rear panel low frequency reference, via a TR line (normally supplied from the CAT).

Gain Control:

A 2-bit parameter used to divide down the on board shift register oscillator. The divide down factor is 1, 2, 4 or 8.

Reread:

Resets the memory pointers for event reread.

Stop Inhibit:

Used for disabling the TDC.

Encoding Inhibit:

Used to allow for two event buffering (one in SOS shift registers, one in data memory. If a second event is buffered, SS = 3 responses replace SS = 0 on valid data space reads.

AFC:

Fourteen locations allocated to Auxiliary Functions Card.

AUXILIARY CONNECTOR

(Auxiliary Functions Card Socket)

T0	B1	A1	T1
T2	B2	A2	T2
T4	B3	A3	T3
T6	B4	A4	T4
T8	B5	A5	T5
T10	B6	A6	T6
T12	B7	A7	T7
T14	B8	A8	T8
T16	B9	A9	T9
T18	B10	A10	T10
T20	B11	A11	T21
T22	B12	A12	T22
T24	B13	A13	T25
T26	B14	A14	T27
T28	B15	A15	T29
T30	B16	A16	T31
T32	B17	A17	T33
T34	B18	A18	T35
T36	B19	A19	T37
T38	B20	A20	T39
T40	B21	A21	T41
T42	B22	A22	T43
T44	B23	A23	T45
T46	B24	A24	T47
T48	B25	A25	T49
T50	B26	A26	T51
T52	B27	A27	T53
T54	B28	A28	T55
T56	B29	A29	T57
T58	B30	A30	T59
T60	B31	A31	T61
T62	B32	A32	T63
T64	B33	A33	T65
T66	B34	A34	T67
T68	B35	A35	T69
T70	B36	A36	T71
T72	B37	A37	T73
T74	B38	A38	T75
T76	B39	A39	T77
T78	B40	A40	T79
T80	B41	A41	T81
T82	B42	A42	T83
B84	B43	A43	T85
B86	B44	A44	T87
T88	B45	A45	T89
T90	B46	A46	T91
T92	B47	A47	T93
T94	B48	A48	T95
BRD	B49	A49	UCSRSTRB
A2	B50	A50	A3
A0	B51	A51	AI
TRIG STRB	B52	A52	VALID ADDRESS
FC	B53	A53	PCT
DB10	B54	A54	DB11
DB8	B55	A55	DB9
DB6	B56	A56	DB7
DB4	B57	A57	DB5
DB2	B58	A58	DB3
DB0	B59	A59	DB1
-2V	B60	A60	A.G.
-5.2V	B61	A61	-5.2V
+5V	B62	A62	+5V
-15V	B63	A63	+15V
D.G.	B64	A64	D.G.
D.G.	B65	A65	D.G.

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VIEWED FROM FRONT OF CRATE
(REVERSE FOR REAR VIEW)

Hit Pulses: 96 signals called T0 to TR95. Pulse equal in duration to the front panel input pulse duration. TTL, active low signals.

Trigger Strobe: A signal received by the TDC via the FASTBUS segment from the 1810 CAT module. Normally used by the AFC to define the fiducial time interval.

DB0-DB13: A 14-bit bidirectional bus. TTL, active low.

BRD: Defines direction of data bus DB0-DB13. When high AFC is in read mode (i.e., being read from the Segment).

Address Lines: A0-A3; UCSRSTRB: Addresses A0-A3 in conjunction with the decode AFC address strobe (UCSRSTRB) allows user implementation of FASTBUS CSR locations C0000002_n to C000000F_h. Fourteen locations are available for use on the AFC. A0-A3 are latched on TDC card.

Valid Address: TTL Active low signal to be driven by AFC circuits if an implemented address being accessed on the AFC. Used to generate the proper SS=0 response to FASTBUS; otherwise, SS=6 is generated if Valid Address is not driven low.

Power Supply: All FASTBUS voltages.

PCT: TTL active low signal asserts module t pin (Service Request) in response to a (BD)_h broadcast.

FC: TTL active low signal equal in duration to the Fast Clear input applied via the front panel or 1810 CAT module.



FASTBUS Series 1880 96 Channel Gated Integrating ADC

- **High Density:** 96 channels/#1 FASTBUS
- **Short Gates:** 50 nsec to 2 μ sec
- **Fast Clear:** <600 nsec
- **Calibration:** to \pm 1.5%
- **Fast Readout:** to 8 megawords/sec
- **Trigger Outputs:** 24 current sums
- **Short Conversion Time:** <750 μ sec
- **High Sensitivity:** to 50 fC/count
- **Readout During Conversion**
- **Positive and Negative Versions**
- **Wide Dynamic Range:** to 15 bits

The FASTBUS Series 1880 consists of 96 Channel ADC's providing current integrating quasi-differential negative or positive inputs. The two versions offered, Models 1882 and 1885, differ in that the 1882 offers 12-bit operation and the 1885 offers the equivalent dynamic range of a 15-bit linear ADC. An N or P suffix indicates negative or positive operation.

Gated integrating ADC's provide high flexibility. The use of gated integrators allows the shaping time of the system to be determined at run time. The same ADC can be used to encode photomultiplier and chamber signals or to sample slowly varying signals. DC-coupled, gated integrators are best suited to high rate applications, especially when a wide dynamic range is required.

The 96 inputs are received via two 100-pin pc edge connectors. The input has been designed to accept signals via two pc paddle cards, simplifying the routing of cables. The input reference for each group of 48 channels is separately isolated from ground for low frequencies. This provides common mode noise rejection and hence minimizes the effect of ground loops.

The 1880 Series may be used with the optional Model 1810 CAT module to provide the Calibration And Trigger signals required by the ADC. Operation without a CAT is also possible using the software-selectable front-panel Gate and Fast Clear Inputs. Strobe Fan-Outs and the calibration voltage must however then be supplied by the user. The readout of the 1880 Series is in accordance with the FASTBUS Standard, so modules may be read out via Standard FASTBUS hardware such as a Segment Interconnect (SI), a Model 1821 FASTBUS Segment Manager/Interface (SM/I) or via a Model 1805 FASTBUS Starter Kit.

The conversion time of the 1880 Series ADC is less than 750 μ sec and readout can proceed during the conversion time. Thus, ADC readout can be complete just after the encoding process is finished. This simultaneous readout feature is implemented in the Model 1821 SM/I.

INPUT CIRCUIT

The input circuit employs 24 of the 4 channel Charge Multiplexers (QMUX) Model MIQ401 monolithic circuits. The QMUX is designed to supply the integrate-and-store function as well as the output multiplexing to the common integrator and ADC.

Each input signal is split into three parts called "low range" (80% of the input signal), "high range" (10% of the input signal) and "current sum" (10% of the input signal). Note that the current sum is an ungated signal whereas the rest of the signals are gated, integrated and held inside the MIQ401 prior to digitizing. For details, see the MIQ401 data sheet.

CONVERSION TECHNIQUE

In order to cover a wide dynamic range with a single 12-bit ADC the dual range technique is used within the 1885 Series ADC's. This technique allows less than 1% quantization error from 5 pC to 1600 pC and corresponds to 15 bits of dynamic range.

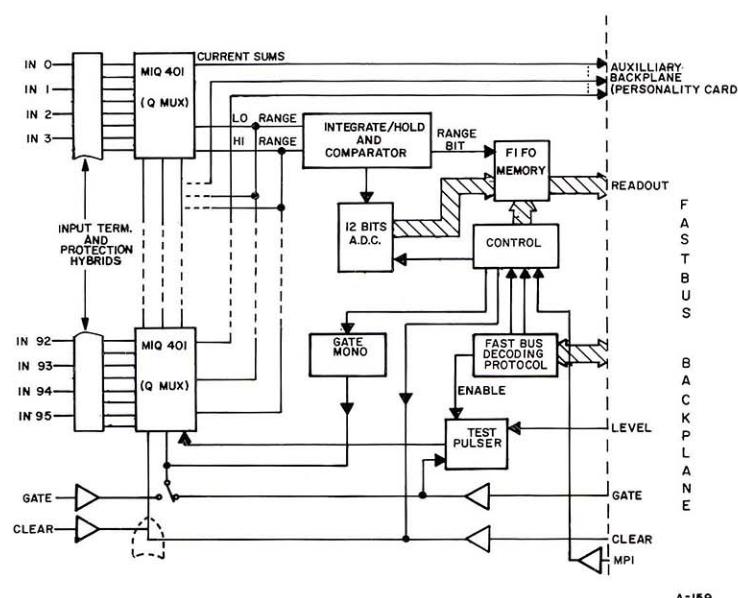
For input signal less than ≈ 180 pC the 1885 Series ADC's digitize the signal with a resolution of 50 fC per count. For signals between ≈ 180 and 1600 pC the resolution is 400 fC/count. The digitized output from each channel consists of a 12-bit amplitude word and a range bit (13th bit). The user can choose by program between "low range", "high range" or "auto range".

ANALOG OUTPUT

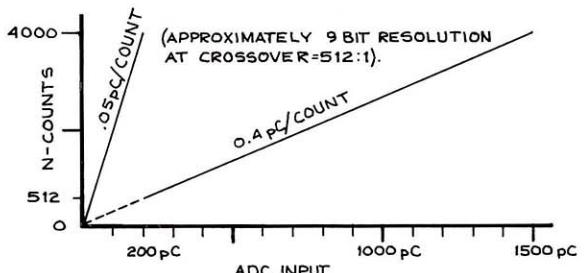
Twenty-four sum output signals to be used for triggering are routed to the FASTBUS Auxiliary Connector. Each of these 24 signals is 10% of the ungated sum of a group of 4 adjacent channels. The output stages are open collectors, allowing further summing to be performed easily, if needed. The 1880 Series modules also provide power and control at the Auxiliary Connector.

CALIBRATION

The Series 1880 employs a calibration circuit allowing the gain of all ADC channels to be measured to better than 1.5%. The calibration circuits are voltage-programmed pulse generators. A DC level (Test Ref) is bussed from the 1810 CAT module to all 1880 Series modules within the FASTBUS crate using the FASTBUS UR lines. When calibration is enabled via CSR 0, the leading edge of the gate causes a well defined amount of charge (proportional to the Test Ref Level) to be deposited in each of the ADC inputs.



Block Diagram 1880 Series ADC



Dual Range Technique for Increased Dynamic Range

SPECIFICATIONS

Models 1882/1885

96 CHANNEL FASTBUS ADC

Type:	Gated Current-Integrating
Channels:	96
Input:	Quasi-differential. Impedance $50 \Omega \pm 5\%$. Protected to $\pm 100 V$ for $1 \mu\text{sec}$.
Input connector:	Two 100-pin pc edge connectors AMP 583 900-3 or equivalent. For input paddle cards, consult the factory.
CMRR:	
Negative mode:	>50 dB for $\pm 200 \text{ mV DC}$ to 1 kHz
Positive mode:	>40 dB for $\pm 200 \text{ mV DC}$ to 1 kHz.
Full-Scale Charge:	
1882:	200 pC $\pm 10\%$ (larger full range by special factory option)
1885 Low Range:	180 pC nominal
1885 High Range:	1600 pC $\pm 10\%$
Sensitivity:	
1882:	50 fC/count $\pm 10\%$
1885 (Bi-linear):	Low range: 50 fC/count $\pm 10\%$ High range: 400 fC/count $\pm 10\%$ $< \pm (0.25\% \text{ of reading} + 2 \text{ counts})$
Integral Non-Linearity:	
Operating Region:	
Negative version:	+ 10 mV to - 1.5 V for specified linearity, (+ 0.2 to - 30 mA into 50Ω).
Positive version:	- 10 mV to + 0.5 V for specified linearity, (- 0.2 to + 10 mA into 50Ω).
Gate Input:	Differential ECL input via a 2-pin front panel connector or via TR1 (B47) and TR2 (B48) lines on the FASTBUS backplane. May be driven by the Model 1810 CAT Module. TR1 is the positive input. Width: 50 nsec to 2μ . Uses removable termination resistor for busing of more than one module.
Fast Clear:	Differential ECL input via a 2-pin front-panel connector or a single-ended ECL signal via TR0 (B46) line on FASTBUS backplane which may be driven by the Model 1810 CAT module. May be executed at any time. Settles to within ($0.1\% \text{ of reading} + 1 \text{ count}$) within 600 nsec. Minimum width: 50 nsec. Uses removable termination resistor for busing of more than one module.
Interchannel Isolation:	>60 dB
Calibration Feature:	Allows the gain of any channel to be measured to within $\pm 1.5\%$. Needs an external DC voltage and a gate signal. The charge pulse applied to all channels is proportional to the DC voltage across the differential Test Level Inputs (UR1 is the positive input) on the FASTBUS backplane. Voltage range: 0 to 10 V. The calibration coefficient is 160 pC/V. $< \pm (0.1\% \text{ of reading} + 1 \text{ count})/\text{°C}$ $\pm (0.25\% \text{ of reading} + 10 \text{ counts})/\text{week}$
Temperature Coefficient:	
Long Term Stability:	
Power Dissipation:	<0.40 W/channel
Fast Analog Output:	24 un gated current sum signals on Auxiliary FASTBUS connector. Signal shape: same as analog input; signal amplitude = 0.1 times input signal amplitude. Output impedance: $\geq 100 \text{ k}\Omega$. Output compliance: 4 to 7 V.
ADC:	12 bits
Conversion Time:	<750 μsec for all 96 channels
External (MPI) Input:	Measure Pause Interval. Single-ended ECL signal via TR5 (B51) line on FASTBUS backplane. May be driven by the Model 1810 CAT Modules. Defines when conversion starts, if enabled by program.
Packaging:	Single-width FASTBUS module in conformance with FASTBUS Specification dated December 1983.
Power Requirements:	300 mA at + 15 V 3.4 A at + 5 V 1 A at - 2 V 2.8 A at - 5.2 V 100 mA at - 15 V

FASTBUS CONTROL

Implemented Addressing Modes:
Implemented Broadcast Functions:

Geographical, Secondary, Broadcast

Code	Significance	Comments
01 _h *	General Broadcast Select	The ADC modules are selected and respond to subsequent data cycles.
09 _h	Sparse Data Scan (SDS)	ADC modules containing data assert their "T pin" on the following read data cycle.
09 _h	Pattern Select	ADC's seeing their T pin asserted on the following write data cycle become selected to respond to subsequent data cycles.
0D _h	All Device Scan	All ADC modules assert their T pin on the following read data cycle.
9D _h	ADC SDS	Unique Sparse Data Scan for 1880 Series modules only. Follows standard SDS (see above).

*An h subscript indicates hexadecimal (base 16).

Slave Status Responses to
Data Cycles:

SS	Significance
0	Valid action
1	Busy
2	End of data
6	Error. Invalid mode
7	Error. Invalid Secondary Address loaded into internal address register

CONTROL FUNCTIONS IMPLEMENTED

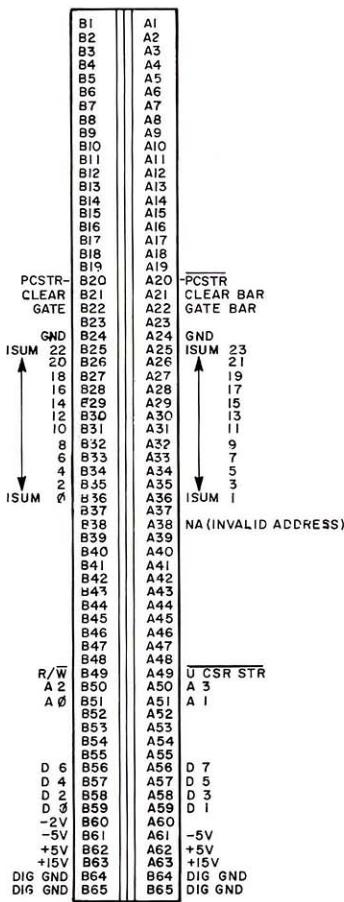
(CSR Space)

Module Identification Code:
Trigger Personality
Programming:
Auto Range Select:
Hi-Lo Range Select:
Gate Source:
MPI Source:
Test Enable:
Memory Test:

Read Only. (1040)_h for 1882N, (1041)_h for 1885N, (1042)_h for 1882P, (1043)_h for 1885P.
Addressing supplied for sixteen 8-bit user-supplied registers.
Sets the readout conversion mode to Auto Range.
Fixes the readout conversion mode to high or low range.
Selects either front panel or backplane.
Selects internal monostable or backplane.
Enables test mode
Enables FASTBUS write to internal data buffer.

AUXILIARY CONNECTOR

(Auxiliary Functions Card Socket)



Pin Out Description:

- ISUM_j: 1/10 of the sum of the ungated input currents of 4 adjacent channels ($0 + 1 + 2 + 3$, $(4 + 5 + 6 + 7)$, ..., $(92 + 93 + 94 + 95)$). $0 \leq j \leq 23$.
- CLEAR, CLEAR: Differential ECL Fast Clear pulse. Valid from 20 nsec after the time of application of the Fast Clear pulse at the CAT until 20 nsec after the next Gate pulse.
- GATE, GATE: Differential ECL Conversion Gate Pulse. Occurs 20 nsec after the Gate is applied to the CAT. Duration equal to the input pulse.
- R/W: Defines which operation, read or write, is strobed by UCSRSTR.
- UCSRSTR: User CSR strobe. Applied when the user accesses (reads or writes) the CSR user space C000000_h-C000015_h.
- A_j: Four-bit CSR user space address. Eg. CSR address C00001_h corresponds to A = 1.
- D_j: Eight-bit data word.
- Invalid Addr: TTL high level applied to pin A38 from the Auxiliary Card indicates that the CSR register accessed is not implemented. The 1880 Series modules responds with SS = 7.

AUXILIARY CONNECTOR PIN ALLOCATIONS FOR THE

1880 SERIES ADC PERSONALITY CARD

A209

SPECIFICATIONS SUBJECT TO CHANGE



FASTBUS Model 1891

Multiple Record Buffer Memory

- **High Capacity:** 1 megabyte
- **High Density:** #1 FASTBUS
- **Event Blocking**
- **Dual Port Memory:** FASTBUS and ECLport
- **Parity Checking**
- **High Data Rate:** 20 megabyte/sec
- **1821 Compatible**
- **Obsolescence Protected:** Upgradeable to 4 megabytes
- **FASTBUS Standard**

This single-width FASTBUS 1 megabyte memory module is intended to be used as a fast first-in first-out (FIFO) memory for 16 or 32-bit data from event based experiments. It may be used as a straight line FIFO, Linear Mode (see Figure 1) or as a rotary FIFO, Circular Mode (see Figure 2). The Model 1891 can also be used as a fast random access FASTBUS memory.

The 1891 accepts data via its front-panel ECLport using the ECLbus standard protocol. It is compatible with a variety of 16 and 32-bit data sources, including the Model 1821 FASTBUS Segment Manager/Interface, the PCOS III MWPC system and the 4300 FERA ADC system. Data may also be written from the FASTBUS Segment. The module has facilities to accept or overwrite (Fast Clear), the record being received via the ECLport.

The Model 1891 can output data to FASTBUS in the same order in which it was received at a combined read/write rate of ≤ 20 megabyte/sec. Each record is stored in a block of contiguous memory locations. A Header Word is automatically written at the start of the record upon completion of data transmission (End of Record Signal). The Header contains a Record Valid flag bit, an ID number assigned to the event, user-set bits and a pointer to the address of the start of the next record. The circuitry within the Model 1891 allows records to be read out or skipped one by one under FASTBUS control.

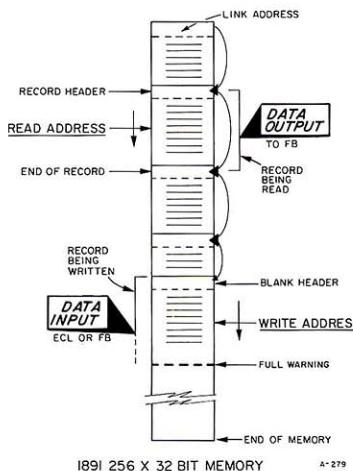


Figure 1
Linear Mode

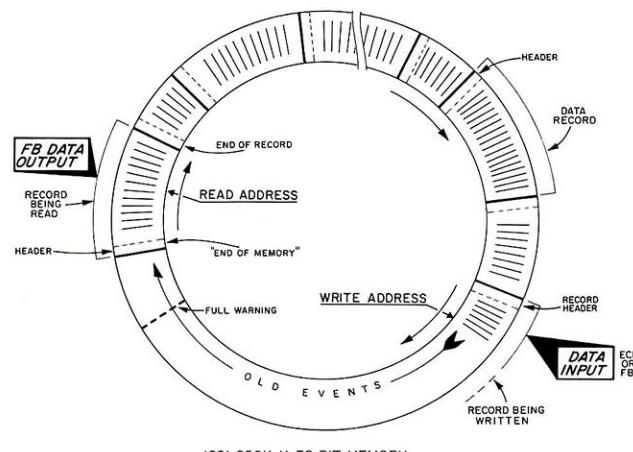


Figure 2
Circular Mode

MODULE FEATURES

MEMORY SIZE

The memory has a capacity of 512K 16-bit words or 256K 32-bit words plus parity. The capacity to upgrade to 1024K words is provided in its operating system. A larger capacity can be provided by linking two or more modules in either the Circular or Linear modes. In either mode, the transfer of the active data input ECLport from module to module is transparent to the user.

DATA INPUT

A front-panel ECLport is employed to accept high-speed 16 or 32-bit datawords using the ECLine standard. A CSR #0 bit can be set and cleared to enable and disable the ECLport input.

DATA STORAGE

The Write Pointer register contains the destination of the next data word received. After each write, the Write Pointer is incremented. The end of a data record is signaled either by an End of Record strobe from the data source or by a FASTBUS command. A Record Header is then written into the first word of the record.

The Record Header contains four Flag Bits, an 8-bit event ID number and the 20-bit address of the header of the next record. The next header address is used to identify the end of the record during a block read. The event ID is used to distinguish records. When several memories are recording data from the same event the ID allows synchronization checks. The two user Flag Bits can be set from the front panel or from FASTBUS for a variety of purposes. The other two Flag Bits are used internally but may be read via FASTBUS. One indicates that the writing of the record has been completed and that it may be read. The other indicates that the record extends into the next module. When a record spans a module boundary, the "next header" address is zero. The first word in the next contains the Record Header.

FAST CLEAR

A Write Abort command from either the front-panel input or FASTBUS disables data input until receipt of an End of Record input. The Write Abort also resets the Write Pointer to the start of the current record, thus releasing that part of memory for overwriting.

INPUT OVERFLOW WARNING

On reaching an address equal to "end of memory less offset", a front-panel differential ECL Full Warning output signal is generated. The offset may be user programmed. This signal can be used to terminate the flow of input data in an orderly manner. A CSR #0 bit is set by the Full Warning and another upon reaching End of Memory. In Circular Mode, the end of memory is defined by the value in the End of Memory register. In Linear Mode, it is the physical end of the memory.

DATA OUTPUT

Any word in the memory can be read directly by a FASTBUS Single read from data space. The normal output mode, however,

is the FASTBUS block transfer. Recognition of the block boundaries can be enabled by transferring the Header into an End of Block register via FASTBUS. The Block Transfer will continue until the header of the next record is read when SS = 2 will be generated. A record can be reread by writing its header address to the Read Pointer. When the physical end of memory is reached, SS = 6 is generated. If a parity error is detected during data output, SS = 7 is sent and a CSR #0 bit is set.

MODULE LINKING

If several modules are linked and fed in parallel with the same data, they can be used as a single large memory. As each one fills, it disables its own ECLport input and enables that of the next module. A CSR #0 bit is used to select which of the linked modules will be stored. To facilitate the paralleling, the inputs are terminated in $110\ \Omega$ with socketed DIP resistors which may be removed to provide a high-impedance input.

All records, including those which straddle a module boundary, may be read via FASTBUS. When the end of the first memory is reached, it is necessary to release one module and lock on to the second. An SS = 3 response is used to indicate that the end of the memory has been reached before the end of the record. The first word of the second memory is the Record Header of the boundary-spanning record. To allow the Master to keep track of which module is being read, a CSR #0 bit can be used by the Host as a flag.

LINEAR MODE

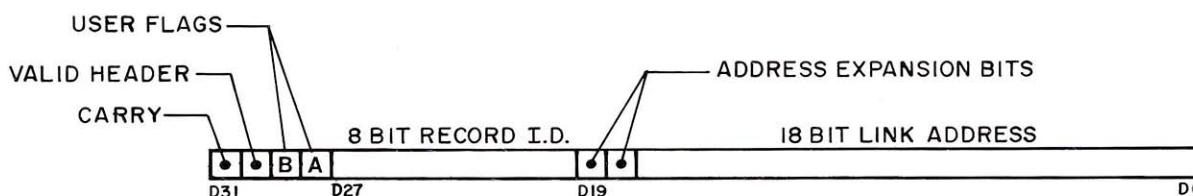
In linear FIFO Mode, each memory location is used once as a write location and once as a read location. The Read Pointer is always nearer the beginning of the memory than the Write Pointer. The pointers are only reset after all the data has been read. This mode is most useful for data which comes in bursts and sufficient memory is required to store nearly all the input data from a burst.

CIRCULAR MODE

If the data input source is continuous, it is possible to link one or more modules as a circular FIFO. The header valid/invalid bit prevents the Read Pointer overtaking the Write Pointer. The End of Memory register provides protection against the Write Pointer overtaking the Read Pointer. Note that in Circular Mode, the "End of Memory" is an user-set variable and does not indicate the physical end. EOM should be located at the end of the last completely read record.

INTERFACE CONTROL

A bidirectional Control Port is provided to facilitate setup of a Model 1821 Segment Manager/Interface, which may be the ECL data source when used as a Master in a FASTBUS crate. The port is written to and read as a CSR register. It provides 24 single-ended TTL level signals at a front-panel mounted 34-pin connector. Eight bits are used to send control signals to the 1821, the other 16 can send and receive data. One of the control bits sets the direction of data flow.



Record Header Format

SPECIFICATIONS

Model 1891

256K WORD MULTIPLE RECORD BUFFER MEMORY

Unless specified all inputs are differential ECL level (≥ 400 mV input swing), $110 \Omega \pm 10\%$ impedance. High impedance by a simple user option.

FRONT-PANEL I/O

Data Inputs:	32 inputs grouped as two 16-bit words.
Minimum pulse length:	60 nsec.
Maximum data rate:	5.1 megawords/sec, 32-bit input. 10.2 megawords/sec, 16-bit input.
Data Strobe:	Latches input data at the Auxiliary Port.
Minimum pulse length:	20 nsec.
Minimum data set-up time:	0 nsec.
Minimum data hold time:	60 nsec.
End of Record Strobe:	Indicates data input over. Writes the Header. Disables Data Inputs for 3 μ sec and retains all words received before the strobe.
Minimum pulse length:	20 nsec.
Write Abort Strobe:	Aborts the block being written.
Minimum Width:	20 nsec.
User Flag Inputs:	See Record Header Format, above.
Minimum Width:	20 nsec.
Flag A:	Differential ECL. A true level sets the Header A bit to 1.
Flag B:	Differential ECL. A true level sets the Header B bit to 1.
Flag A and B:	Differential ECL. A leading edge sets the A and B Header bits to 0.
User Flag Strobe Clear:	Latches the User Flags.
Minimum Width:	20 nsec.
Full Warning:	3-state differential ECL* output via a front-panel 2-pin connector. Active as long as the Write Pointer lies between the values End of Memory and (End of Memory—Offset).
Full:	3-state differential ECL* output via a front-panel 2-pin connector. Active as long as the Write Pointer equals the End of Memory.
Ready:	3-state differential ECL* output via a front-panel 2-pin connector. Indicates that the module is able to accept input data; i.e., it is enabled, it is in Run mode, and it is not carrying out an internal operation (End of Record, Write Abort, etc.)
Link Left/Link Right:	TTL-level single-ended control signals supplied via two 4-pin front-panel connectors. Used to link adjacent modules for operation as a single memory.
Control (SM/I) Port:	TTL-level front-panel port comprising a 16-bit bidirectional data bus and seven control lines. Used to control an 1821 SM/I from the Segment containing the 1891. This port has no effect on the operation of the 1891.

FRONT-PANEL INDICATORS

S	Slave activity indicator. Monostable-stretched to 100 msec minimum.
LM	Last Module. Indicates the rightmost module, i.e., that no further module is linked in a Linear mode chain. Also indicates a single Circular mode module.
CM	Circular Mode. Indicates that one or more modules are circularly linked.
FW	Full Warning. Indicates that the Full Warning output is active.
FL	Full. Indicates that the memory cannot accept more data.
RY	Ready. Indicates that the module is enabled to store input data.
ST	Strobe. Indicates the arrival of a Data Strobe input. Monostable-stretched to 100 msec minimum.

GENERAL

Memory Size:	512K 16-bit words or 256K 32-bit words plus one parity bit.
Data Blocking:	A Record Header is written to memory at the start of a data record on receipt of a front-panel or FASTBUS End of Record command.
Header Format:	Four flag bits (two user specified). Eight Record Identity bits. Twenty Link Address bits pointing to the start of the next record.
AS-AK Handshake Time:	65 nsec typical. 90 nsec maximum.
DS-DK Handshake Time	440 nsec typical.
Single transfers:	620 nsec maximum.
Block Transfers:	TBA typical. TBA maximum.
Mean Block Transfer Rate:	5.1 megawords/sec.

NOTE: These times assume that the Auxiliary Port is idle during FASTBUS operations.

*Disabled when the module is inactive. This output may be bused between linked modules.

Power Requirements:
 11 A at + 5 V.
 2 A at - 5.2 V.
 Packaging:
 Single-width FASTBUS module in conformance with FASTBUS specification dated December, 1983.

FASTBUS CONTROL

Addressing Modes:
 Geographical, Logical, Broadcast.
 Logical Addressing uses a 16-bit Module Address and no Internal Address. All memory access is via Secondary Addressing.
 Broadcast Functions:
 A 16-bit Broadcast Class register is provided. Modules which recognize their Class will execute subsequent CSR Write Cycles. This permits selected groups of modules to perform simultaneous control operations.

Slave Status Responses to Data Cycles:

SS	Significance
0	Valid action
1	Busy.
2	Indicates the end of a record.
3	End of Memory was reached before the end of the record.
6	Error—Non-implemented command or action with invalid address.
7	Error—Invalid address written or memory parity error.

BIT ALLOCATIONS

CSR #0

Bit	Function	Type
0	Memory Parity Error	Status
1	Logical Address Enable	Mode Select
2	Run/Stop	Command
6	Last Module	Mode Select
7	Circular Mode	Mode Select
8	Full Warning	Status
9	Full	Status
10	End of Record	Command
11	Write Abort	Command
12	Active Flag	Command
13	User Flag	Status
16-31	Module ID (1046) _h *	
30	Master Reset (i.e., CSR #0, 7 and 10 _h -15 _h) Clear Data (i.e., CSR #11 _h , 13 _h , 15 _h)	Command

CSR REGISTER FUNCTIONS

CSR #

	Function
(3) _h *	Logical Address
(7) _h	Broadcast Class
(10) _h	Control (SM/I) Port Read/Write
(11) _h	Write Pointer. Used as the Write Address for Auxiliary Port input. Increments automatically after each input word.
(12) _h	Record Number. 8-bit register for record identification. Incremented automatically each time a header is written.
(13) _h	End of Memory. Pointer to the first unavailable memory location.
(14) _h	Offset. User-selected offset above End of Memory used to generate Full Warning.
(15) _h	End of Block. Pointer to the first address not to be read in a Block Transfer.

FASTBUS OPERATIONS

Data Space Write:

Data can be written from FASTBUS using either single transfers or Block Transfers. The user must generate appropriate header words to read the stored data in record format. Both Single and Block Transfers are supported. Appropriate SS codes are generated to indicate End of Block, parity error and End of Memory. See above.

Data Space Read:

Single Transfer and Broadcast modes are supported.

CSR Space Write:

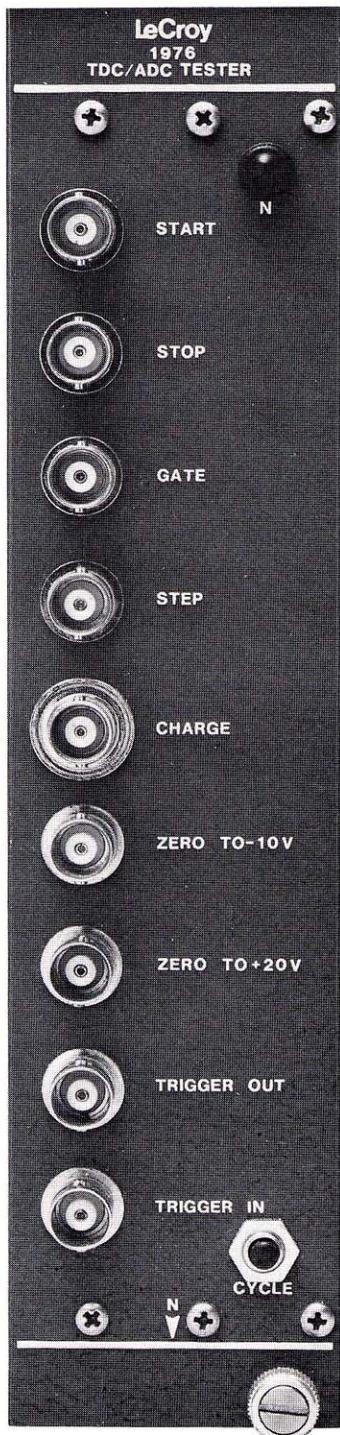
Single Transfer mode is supported.

CSR Space Read:

This module can be addressed Geographically and Logically and also responds to Broadcast addressing. Secondary addressing is used for all access to Data Space which comprises the 256K data words.

*An h subscript denotes a hexadecimal number, i.e., base 16.

SPECIFICATIONS SUBJECT TO CHANGE



CAMAC Model 1976 ADC/TDC Tester

The LeCroy Model 1976 is a programmable pulse generator packaged in a #3 CAMAC module. It has been designed as a test instrument useful for servicing ADC's and TDC's of the type manufactured by LeCroy. With it, linearity and resolution measurements can be made on TDC's and current-integrating ADC's. In conjunction with the Model 1516 Shaper-Amplifier it can also be used to test peak-sensing ADC's.

The Model 1976 has front-panel BNC outputs to accommodate each of the test modes. For ADC calibration, separate outputs are provided which supply a CHARGE pulse, a voltage STEP, a positive DC level, and a negative DC level. Peak signals are derived from the voltage step output using the LeCroy Model 1516 Peak-Shaping Amplifier. A NIM standard GATE output allows the ADC under test to be strobed or gated. NIM standard START and STOP outputs are also supplied for TDC calibration.

The pulse generator circuits of the Model 1976 are driven by a pair of digital-to-analog converters (DAC's). The output pulse amplitude or time interval programming precision is 16-bits, whereas an 8-bit DAC is used to determine the gate width.

The operating mode of the Model 1976 is defined by a 13-bit control word. This allows the charge, peak (when used with Model 1516), or time-interval mode to be selected. It also specifies the full-scale for each mode. CHARGE pulse shape and the width of the START and STOP pulses are also defined in this way.

The Model 1976 contains three registers called GATE TIME, AMPLITUDE, and CONTROL. The information written into them uniquely defines a test cycle which is executed 5 msec after the AMPLITUDE word is written into the Model 1976. A cycle may also be initiated by application of a TTL pulse at the front-panel trigger input. A front-panel cycle button can be used to initiate repetitive cycling at 100 Hz rate. Each cycle is preceded by a trigger output to facilitate interrogation of the signal outputs.

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SPECIFICATIONS

CAMAC Model 1976

ADC/TDC TESTER

OUTPUT CHARACTERISTICS

CHARGE

Front-panel BNC connector shield is AC-coupled to chassis ground. Output impedance is 50 ohms. Supplies a signal similar to a photomultiplier pulse with falltime selectable under CAMAC control. See options below. Charge output should be disabled when not in use in order to avoid crosstalk with other outputs. The risetime is <6 nsec, but smaller outputs are significantly faster.

Programming Options:

	Fall Time (90% to 10%)	
<u>Full Scale</u>	<u>Fast Tail</u>	<u>Slow Tail</u>
300 pC	15 nsec	350 nsec
600 pC	35 nsec	600 nsec
1200 pC	65 nsec	1200 nsec

See Control Word Breakdown Table under CAMAC OPERATIONS for Mode Selection.

Full-Scale Accuracy:

±2%.

Linearity:

<0.05% of full scale.

Amplitude Temp. Coef.:

<0.003%/°C (25°C to 50°C).

Noise:

<0.1 pC (rms).

Load Impedance:

50 Ω ± 1%.

STEP

Front-panel BNC connector, DC-coupled, supplies a negative-going transition of maximum amplitude of 1.0 V with a 10-90% risetime of 10 nsec from a quiescent level of +0.7 V. Load impedance should be 50 Ω. Step output should be disabled when not in use to avoid crosstalk with other outputs.

GATE

Front-panel BNC connector. NIM current source outputs parallel-terminated with 50 Ω. Drives a 50 Ω load to -800 mV with risetimes and falltimes of <2 nsec. (10% to 90%). Leading edge precedes the CHARGE pulse by 15 nsec and the STEP output by 35 nsec.

Programming Options:

Pulse width equal to the START-STOP interval +10 nsec. See below. Normally programmed via the 8-bit DAC. See Control Word Breakdown Table under CAMAC OPERATION for Mode Selection.

START/STOP

Front-panel BNC connector NIM current-source outputs parallel-terminated with 50 Ω. Risetimes and falltimes <2 nsec. Delivers -800 mV into a 50 Ω load.

Programming Options: (See CAMAC OPERATIONS section for Mode Selection.)

<u>Pulse Width</u>	<u>Full Scale Time</u>	<u>DAC Selection</u>
20 nsec	150 nsec	8-bit ¹
100 nsec	300 nsec	16-bit ²
	600 nsec	
	1200 nsec	
	2400 nsec	
	4800 nsec	
	9600 nsec	

¹8-bit normally for ADC gate width studies.

²16-bit normally for TDC studies.

Full-Scale Accuracy:	$\pm 2\%$.
Linearity:	<0.05% of full scale.
Temperature Coefficient:	<0.005%/°C (25°C to 50°C)
Time Jitter:	<20 psec (rms) for 150 nsec scale. Proportionally greater for longer time ranges.
 NEGATIVE DC LEVEL	
Full-Scale Accuracy:	Front-panel BNC connector. DC level set by the 16-bit DAC. Amplitude 0 to -10 V. Intended to drive $\geq 500 \Omega$.
Linearity:	$\pm 0.5\%$.
Temperature Coefficient:	<0.005% of full scale.
Temperature Coefficient:	<0.001%/°C (25°C to 50°C).
 POSITIVE DC LEVEL	
Full-Scale Accuracy:	Front-panel BNC connector. DC level set by the 16-bit DAC. Amplitude 0 to $+20$ V. Intended to drive $\geq 500 \Omega$.
Linearity:	$\pm 0.5\%$.
Temperature Coefficient:	<0.005% of full scale.
Temperature Coefficient:	<0.001%/°C (25°C to 50°C).
 TRIGGER OUT	
	Front-panel BNC connector supplies a 35 nsec wide 300 mV pulse into 50Ω . AC-coupled TTL negative-going edge (510 ohm in series with 0.01 μF .) Precedes the leading edge of the gate by approximately 50 nsec. (Proportional to the full-scale time range selected.)

CONTROLS

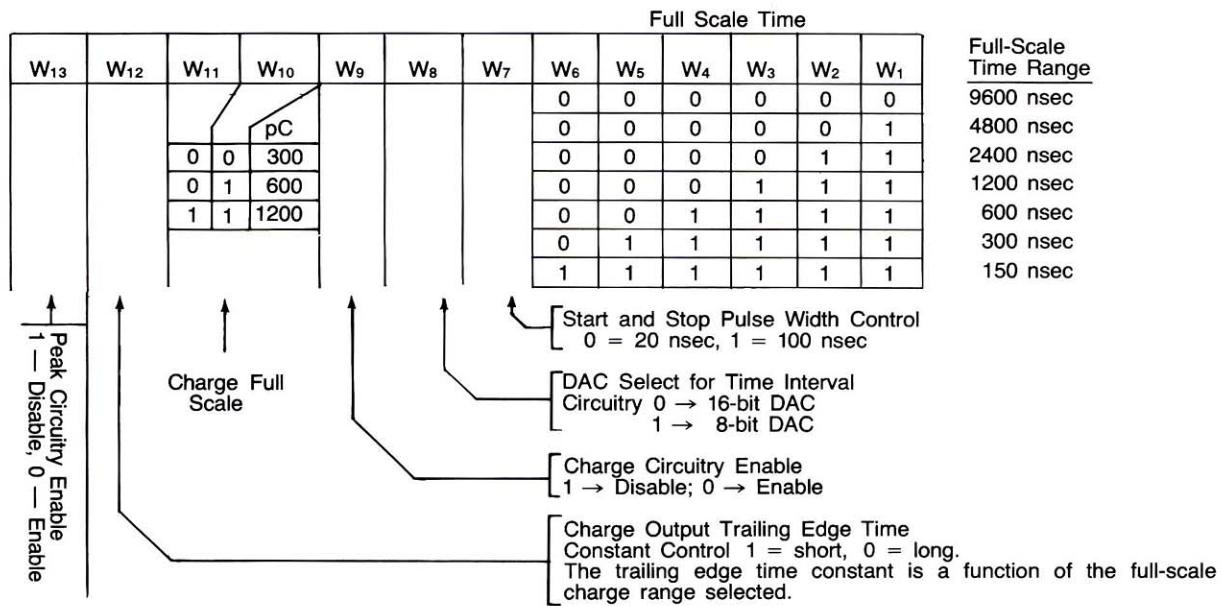
CYCLE BUTTON:	A front-panel pushbutton initiates cyclic operation. The operation is defined by CONTROL, GATE, and AMPLITUDE words. Repetition rate 100 Hz. Cycling is terminated when the module is addressed via the data-way.
TRIGGER INPUT:	Front-panel BNC connector. TTL level (2.5 mA sink). A positive-going edge initiates one cycle as defined by the CONTROL, GATE, and AMPLITUDE words. A TTL low level will inhibit execution of a pulser cycle normally initiated by CAMAC F(16)•A(0) command. Maximum rate 200 Hz.
DAC 8 (Gate Register):	An 8-bit DAC programmable via CAMAC command. May be selected to drive the TIME circuitry using CONTROL word bit W8. Normally used in this way to select gate width.
DAC 16 (Amplitude Register):	A 16-bit DAC programmable via CAMAC command. Drives the AMPLITUDE circuitry. May be selected to drive the TIME circuitry (W8=0). Both POSITIVE LEVEL and NEGATIVE LEVEL outputs track this DAC.

CAMAC OPERATION

Normal operation of the 1976 involves selecting an operating mode by writing into the CONTROL register. This allows the appropriate mode, scale, and pulse options to be selected. If required, an 8-bit word is next written into the gate register. A cycle is initiated when a 16-bit word is written into the AMPLITUDE register. The cycle occurs 5 msec after the CAMAC cycle.

CONTROL WORD BREAKDOWN:

LOADED WITH A N • F(16) • A(1) @ S₁ Time



NOTE: 1 — CAMAC "C" sets the Control Word to all zeros

2 — In Peak or Charge Mode the 8-bit DAC must be used for the time interval. The maximum gate width is then defined by the 'Full Scale Time Range' and the actual gate is:

$$\text{Gate Width} = 10 \text{ nsec} + \text{Full Scale} \times \left[1 - \frac{\text{Gate DAC Word}}{255} \right]$$

CAMAC COMMANDS:

- F(16) • A(0) Write AMPLITUDE and cycle. Loads W1-W16 into the 16-bit AMPLITUDE register. At S₁ time + 5 msec one pulser cycle is executed.
- F(16) • A(1) Write CONTROL. Loads W1-W13 into the 13-bit CONTROL register.
- F(16) • A(2) Write GATE word. Loads W1-W8 into the 8-bit GATE register.
- C • S₂ Zeros CONTROL word.

Power Requirements:

- 510 mA at + 6 V
- 85 mA at + 24 V
- 540 mA at - 6 V
- 170 mA at - 24 V

SPECIFICATIONS SUBJECT TO CHANGE



CAMAC Model 2228A Octal Time-to-Digital Converter

- 8 channels in single-width module
- 11-bit resolution
- Switch-selectable 100, 200, and 500 nsec full-scale time ranges
- Time resolutions of 50, 100, or 250 psec/count
- Rejects stops before starts
- Fast clear input
- Internal test capability
- Common stop input for precision on-line testing
- Full LAM functions
- Fast digitizing time
- Q and LAM suppression

The LeCroy Model 2228A is an Octal Time-To-Digital Converter, packaged in a No. 1 CAMAC module. It incorporates all the advanced operating characteristics which experience has indicated necessary for accurate and reliable measurement of nanosecond time intervals.

The Model 2228A has 8 independent channels, each of which measures the time from the leading edge of a common start pulse to the leading edge of its individual stop pulse. Each 2228A channel disregards any stop pulses received before a start signal and will accept only one stop for every start.

Conversion begins upon receipt of the start signal and proceeds until one of the following: a stop signal is received; the cycle is terminated by the application of a front-panel clear signal; or the TDC reaches full scale.

The 2228A converts the measured time intervals into a 11-bit digital number at the rate of 20 MHz, for a full scale digitizing time of 100 microseconds. Rear-panel control of full-scale and conversion slope permits digitization to fewer bits and a shorter conversion time if desired. The conversion clock is started in phase with the TDC start signal to assure synchronization and eliminate the inaccuracy introduced by the free-running oscillators in conventional designs. LAM, if enabled, is generated at the end of the conversion interval.

The 2228A has three switch-selectable full-scale time ranges, 100, 200 and 500 nsec, which are digitized to 95% of 11 bits (2048 channels) and provide 50, 100, and 250 psec resolutions respectively. Longer time ranges (up to 10 microseconds) may be provided on request at slight expense of stability and accuracy.

On line testing is facilitated by either a front-panel common stop input of F(25). A signal at the common stop input generates simultaneous stops for each channel, permitting accurate testing of both front end and scaler section of the module and uniform system testing and time calibration. F(25) is provided for a quick test of the front end and scaler sections with a time measurement of 80% of full scale.

In higher rate or colliding beam experiments, excessive system deadtime due to false starts may be eliminated through use of the 2228A's fast clear input. Accepting NIM level signals, this input allows the TDC to be cleared at any point in its conversion cycle without the necessity for any Dataway operations.

All standard LAM functions are available in the 2228A to facilitate data readout. To minimize readout time, both Q and LAM may be suppressed if the module does not contain data.

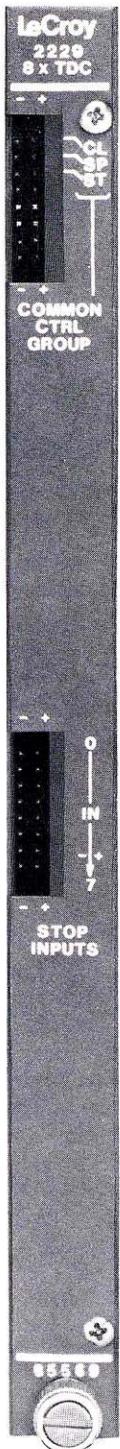
SPECIFICATIONS

CAMAC Model 2228A

OCTAL TIME-TO-DIGITAL CONVERTER

Stop Inputs:	8, one per channel, $50\ \Omega$ impedance; Lemo-type connectors; direct-coupled; input amplitude $> -450\text{ mV}$; ineffective unless preceded by a "Start" input.
Common Start Input:	One, common to all channels, $50\ \Omega$ impedance; Lemo-type connector; input amplitude $> -450\text{ mV}$.
Common Stop Input:	One, common to all channels, $50\ \Omega$ impedance; Lemo-type connector; $> -450\text{ mV}$; functions identical to individual "Stop Inputs" above; used for on-line testing.
Fast Clear	One input, common to all channels; Lemo-type connector; $50\ \Omega$ impedance; -450 mV or greater clears; minimum duration 50 nsec. Requires $1.4\ \mu\text{sec}$ after start of clear signal to settle to 1 ± 1 counts. (However, if the unit is always cleared at a fixed time before each start, it will settle to a constant offset with a small uncertainty, effectively permitting fast reset times on the order of 500 nsec.)
Full-Scale Time Range:	11-bit binary output corresponds to 100, 200, and 500 nsec nominal, switch-selectable (with longest range field-adjustable up to $1\ \mu\text{sec}$). Larger full-scales possible by factory option up to $10\ \mu\text{sec}$. Both the full-scale value and conversion slope are rear-panel adjustable, permitting faster conversion at the expense of range.
Integral Non-linearity:	± 2 counts (20 nsec to full scale).
Differential Non-linearity:	Channel widths vary by $\pm 10\%$ (10 nsec to full scale).
Time Resolution:	50 psec on 100 nsec range; 100 psec on 200 nsec range; 250 psec on 500 nsec range.
Temperature Coefficient:	Typically ($\pm 0.02\%$ of full scale $\pm 0.01\%$ of reading) per degree C.
Digitizing Time:	CAMAC modes conversion is initiated by receipt of "Start" input. Approximately $100\ \mu\text{sec}$ for 11 bits; rear-panel adjustable for fewer bits, shorter conversion time.
Readout Time:	Readout may proceed at the fastest rate permitted by the CAMAC standard after digitizing is complete.
Test Functions:	An internal start/stop is generated by F(25) with approximately 80% of full scale spacing. On-line testing and calibrations can be done with common start and common stop above.
Data:	The proper CAMAC function and address command gates the binary data of the selected channel onto the R(1) to R(11) (2^0 to 2^{10}) Dataway bus lines. The full-scale number of bits, and thus the conversion time, can be selected by a rear-panel pot and test point. (Conversion curve provided with unit.) The overflow flag is always presented on R(12).
CAMAC Commands:	Z or C: All registers are simultaneously cleared by the CAMAC "Clear" or "Initialize" command. Requires "S2". I: "Start" input is inhibited during CAMAC "inhibit" command. Q: A Q=1 response is generated in recognition of an F0 or F2 Read function, or an F8 function if LAM is set for a valid "N" and "A", but there will be no response (Q=0) under any other condition. The Q response for empty modules is suppressed (see Q and LAM suppression). X: An X=1 (Command Accepted) response is generated when a valid F, N, and A command is generated. L: Look-At-Me signal is generated from end of digitizing until a module Clear or Clear LAM. LAM is disabled for duration of N, can be permanently enabled or disabled by the Enable or Disable function command, and can be tested by Test LAM. Switch-selectable option causes LAM to be suppressed by empty modules.
CAMAC Function Codes:	F(0): Read registers; requires N and A. A(0) through A(7) are used for channel address. F(2): Read registers and clear module; requires N, A, and S2. Clears on A(7) only. F(8): Test Look-At-Me; requires LAM, N and any A from A(0) to A(7). Q is Generated if LAM is present and enabled. F(9): Clear module (and LAM); requires N and any A from A(0) to A(7), and S2. F(10): Clear Look-At-Me; requires N, S2 and any A from A(0) to A(7). F(24): Disable Look-At-Me; requires N, S2 and any A from A(0) to A(7). F(25): Test module; requires N, S2 and any A from A(0) to A(7). F(26): Enable Look-At-Me; requires N, S2 and any A from A(0) to A(7). Remains enabled until Z or F(24) applied. Caution: The state of the LAM mask will be arbitrary after power turn-on.
Q and LAM Suppression:	A module receiving no stop inputs will produce no Q response or LAM and appears during readout as an empty CAMAC slot, thus reducing readout time. A Command Accepted response is still generated. The Q and LAM suppress features can be disabled with side-panel switches.
Packaging:	In conformance with CAMAC standard for nuclear modules. (ESONE Report EUR4100 or IEEE Report #583.) RF-shielded CAMAC #1 module.
Power Requirements:	+24V at 25 mA; -24V at 140 mA; +6V at 600 mA; -6V at 550 mA.

SPECIFICATIONS SUBJECT TO CHANGE.



CAMAC ECLine Model 2229 Octal Time-to-Digital Converter

- 8 channels in single-width module
- Complementary ECL inputs and strobes
- 11-bit resolution
- Full-scale time ranges — 100, 200, and 500 nsec
- Time resolutions — 50, 100, or 250 psec/count
- Rejects stops before starts
- Fast Clear input
- Internal test capability
- Common stop input for precision testing
- Q and LAM suppression

The LeCroy Model 2229 is an Octal Time-to-Digital Converter, packaged in a single width CAMAC module. It incorporates all the advanced operating characteristics which experience has indicated necessary for accurate and reliable measurement of nanosecond time intervals. It employs the new ECLline logic standard resulting in cabling convenience and economy.

The Model 2229 has 8 independent channels, each of which measures the time from the leading edge of a Common Start pulse to the leading edge of its individual Stop pulse. Any stop pulses received before Start signal are ignored and only one Stop is accepted for every Start.

Conversion begins upon receipt of the start signal and proceeds until one of the following: a stop signal is received; the cycle is terminated by the application of a front-panel Fast Clear signal; or the TDC reaches full scale.

The 2229 converts the measured time intervals into a 11-bit digital number at the rate of 20 MHz, for a full scale digitizing time of 100 microseconds. Rear-panel control of full-scale and conversion slope permits digitization to fewer bits and a shorter conversion time if desired. The conversion clock is started in phase with the TDC start signal to assure synchronization and eliminate the inaccuracy introduced by the free-running oscillators in conventional designs. LAM, if enabled, is generated at the end of the conversion interval.

The 2229 has three switch-selectable full-scale time ranges, 100, 200, and 500 nsec, which are digitized to 95% of 11 bits (2048 channels) and provide 50, 100, and 250 psec resolutions respectively. Longer time ranges (up to 10 microseconds) may be provided on request at slight expense of stability and accuracy.

On line testing is facilitated by either a front-panel Common Stop input or F(25). A signal at the Common Stop input generates simultaneous stops for each channel, permitting accurate testing of both front end and scaler section of the module and uniform system testing and time calibration. F(25) is provided for a quick test of the front end and scaler sections with a time measurement of 80% of full scale.

In high rate or colliding beam experiments, excessive system deadtime due to false starts may be eliminated through use of the 2229's fast clear input. Accepting ECL level signals, this input allows the TDC to be cleared at any point in its conversion cycle without the necessity for any Dataway operations.

All standard LAM functions are available in the 2229 to facilitate data readout. To minimize readout time, both Q and LAM may be suppressed if the module does not contain data.

November 1982

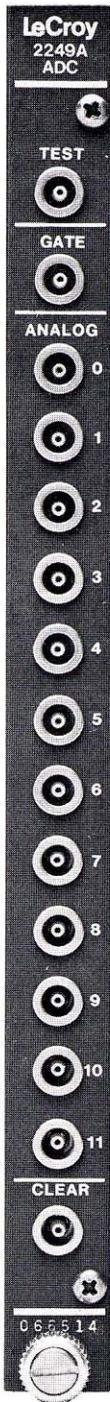
SPECIFICATIONS

CAMAC Model 2229

OCTAL TIME-TO-DIGITAL CONVERTER

Stop Inputs:	Eight, using a 2 × 8 pin connector (mates with LeCroy 403211016 or 3M 3452-6016 or equivalent); accepts differential ECL input levels; 110 Ω input impedance pin-to-pin; direct coupled; 5 nsec minimum width; inputs ignored unless preceded by a "Start" input.
Common Start Input:	One, common to all channels, using a pin pair on the control group (2 × 8-pin) connector (mates with LeCroy 403211016 or 3M 3452-6016 or equivalent); accepts differential ECL input levels; 112 Ω input impedance pin to pin; direct coupled; 5 nsec minimum width.
Common Stop Input:	One, common to all channels, input characteristics identical to Common Stop. Functions identical to the individual Stop inputs above, used for on-line testing.
Fast Clear:	One, common to all channels, input characteristics identical to Common Stop except 50 nsec minimum width. Requires 1.4 μsec after start of clear signal to settle to 1 ± 1 counts. (However, if the unit is always cleared at a fixed time before each start, it will settle to a constant offset with a small uncertainty, effectively permitting fast reset times on the order of 500 nsec).
Full-Scale Time Range:	11-bit binary output corresponds to 100, 200, and 500 nsec nominal, switch-selectable (with longest range field-adjustable up to 1 μsec). Larger full-scale possible by factory option up to 10 μsec. Both the full-scale value and conversion slope are rear-panel adjustable, permitting faster conversion at the expense of range. $< \pm 2$ counts (20 nsec to full scale).
Integral Non-linearity:	Channel widths vary by $< \pm 10\%$ (10 nsec to full scale). $< \pm 30\%$ for long-range option.
Differential Non-linearity:	50 psec on 100 nsec range; 100 psec on 200 nsec range; 250 psec on 500 nsec range.
Time Resolution:	Typically ($\pm 0.02\%$ of full scale $\pm 0.01\%$ of reading) per degree C.
Temperature Coefficient:	Approximately 100 μsec for 11 bits; rear-panel adjustable for fewer bits, shorter conversion time.
Digitizing Time:	Readout may proceed at the fastest rate permitted by the CAMAC standard after digitizing is complete.
Readout Time:	An internal start/stop is generated with approximately 80% of full scale time in response to an F(25) command. On-line testing and calibrations can be done with common start and common stop above.
Test Functions:	The proper CAMAC function and address command gates the binary data of the selected channel onto the R(1) to R(11) (2^0 to 2^{10}) Dataway bus lines. The full-scale number of bits, and thus the conversion time, can be selected by a rear-panel pot and test point. The overflow flag is always presented on R(12).
Data:	Z or C: All registers are simultaneously cleared by the CAMAC "Clear" or "Initialize" command. Requires "S2".
CAMAC Commands:	I: "Start" input is inhibited during CAMAC "inhibit" command. Q: A Q=1 response is generated in recognition of an F(0) or F(2) Read function, or an F(8) function if LAM is set for a valid "N" and "A", but there will be no response (Q=0) under any other condition. The Q response for empty modules is suppressed (see Q and LAM suppression). X: An X=1 (Command Accepted) response is generated when a valid F, N, and A command is generated. L: Look-At-Me signal is generated from end of digitizing until a module Clear or Clear LAM. LAM is disabled for duration of N, can be permanently enabled or disabled by the Enable or Disable function command, and can be tested by Test LAM. Switch-selectable option causes LAM to be suppressed by empty modules. F(0): Read registers; requires N and A. A(0) through A(7) are used for channel address. F(2): Read registers and clear module; requires N, A, and S2. Clears on A(7) only. F(8): Test Look-At-Me; requires LAM, N and any A from A(0) to A(7). Q is Generated if LAM is present and enabled. F(9): Clear module (and LAM); requires N and any A from A(0) to A(7), and S2. F(10): Clear Look-At-Me; requires N, S2 and any A from A(0) to A(7). F(24): Disable Look-At-Me; requires N, S2 and any A from A(0) to A(7). F(25): Test module; requires N, S2 and any A from A(0) to A(7). F(26): Enable Look-At-Me; requires N, S2 and any A from A(0) to A(7). Remains enabled until Z or F(24) applied.
CAMAC Function Codes:	Caution: The state of the LAM mask will be arbitrary after power turn-on. A module receiving no stop inputs will produce no Q response or LAM and appears during readout as an empty CAMAC slot, thus reducing readout time. A Command Accepted response is still generated. The Q and LAM suppress features can be disabled with side-panel switches.
Q and LAM Suppression:	In conformance with CAMAC standard for nuclear modules. (ESONE Report EUR4100 or IEEE Report #583). RF-shielded CAMAC #1 module.
Packaging:	+ 24 V at 25 mA - 24 V at 140 mA + 6 V at 600 mA - 6 V at 600 mA.
Power Requirements:	

SPECIFICATIONS SUBJECT TO CHANGE



CAMAC Model 2249A 12 Channel A-to-D Converter

FEATURES:

- **COMPACT PACKAGING**
12 channels per single-width module means fewer crates, smaller systems, less gate fan-out.
- **WELL-CONTROLLED PEDESTAL**
Advanced hybrid circuit front end eliminates peak shifts and/or constant calibration.
- **EXCELLENT INPUT IMPEDANCE MATCH**
Minimizes possibility of digitizing input reflections.
- **10-BIT RESOLUTION**
One part in 1024.
- **WIDEST DYNAMIC RANGE**
4 times the range of 8-bit ADC's allows broader spectra, better accuracy, simplified setup, prevents small gain shifts from exceeding range of ADC.
- **HIGH SENSITIVITY**
0.25 picocoulomb per count.
- **NO FEEDTHROUGH**
Up to 1,000-fold overloads are rejected by fast gate, eliminating spurious data due to out-of-time chamber firings, noise, etc.
- **UNIFORM SENSITIVITY THROUGHOUT GATE INTERVAL**
No modulation of measurement with position of signal within gate.
- **NO INTERCHANNEL CROSSTALK**
regardless of input amplitude.
- **WELL-VENTILATED MODULE**
Low component count, less than one-fifth of competing designs, permits free circulation of air for cooler, more reliable, and longer-lasting operation.
- **FAST CLEAR INPUT**
enables fast rejection of unwanted data.
- **FULL TEST CAPABILITY**
F(25) simultaneously injects charge into all ADC's proportional to DC level on front panel (or patch pins on Dataway).
- **FULL LAM FUNCTIONS.**
- **HIGH DIGITIZING SPEED**
without sacrifice in differential linearity.
- **LAM AND Q SUPPRESSION**
eliminates readout of empty modules.

The LRS Model 2249A 12-Channel Analog-to-Digital Converter embodies all the operational characteristics which have proved important for general-purpose use in high energy particle physics, including expanded resolution (0.1%), higher sensitivity, excellent stability, faster digitizing rate, LAM and Q suppression, provision for fast clear, calibrating test mode, and flexible LAM options.

These ADCs are specifically intended for use in demanding applications such as particle identification using dE/dx counters, recording x-ray, neutron, or recoil proton energies using lead glass or other total energy absorption counters, improving time resolution by correcting for slewing due to variances in counter output amplitudes, monitoring gas threshold Cerenkov counters, and debugging or monitoring proportional or drift chambers.

The Model 2249A contains twelve complete ADC's in a single-width CAMAC module. Each ADC offers a resolution of ten bits to provide 0.1% resolution over a wide 1024-channel dynamic range. The factor of 4 wider range allows operations with broad signal spectra such as are encountered in experiments anticipating fractionally charged particles or covering extensive energy ranges. It also greatly reduces the necessity for careful adjustment of signal strengths to match the limited range of an 8-bit, 256-channel instrument. The input sensitivity of the Model 2249A is 0.25 pC/count for a full-scale range of 256 pc. This is compatible with most available signal sources and no additional buffering or reshaping of any kind is required to digitize nanosecond pulses.

The excellent long-term stability, temperature characteristics, and isolation between ADC channels assure accurate and reliable performance under the demanding conditions encountered in actual experiments. Confirmation of operation and calibration is provided by the unique test feature which allows all twelve ADC's or an entire system to simultaneously digitize a charge proportional to a dc level provided to a front-panel Lemo connector or patched into P₁, P₂ or P₅ of the Dataway connector.

The Model 2249A offers excellent event rate capability through the incorporation of a fast clear and a fast digitizing rate. The fast clear input enables the ADC to begin digitizing on the command of a prompt gate and be reset, if necessary, before the end of conversion on the basis of delayed logic or chamber information. This feature eliminates the long input delay cables now required in these situations.

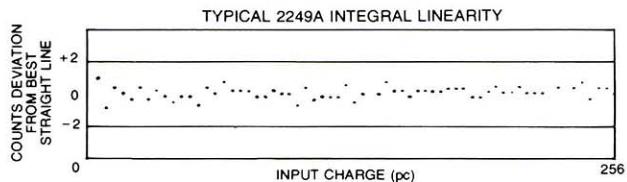
End of conversion of modules which contain data is flagged by generation of a CAMAC LAM. Readout of modules which do not contain information can be eliminated either by use of the LAM signals or through Q suppression.

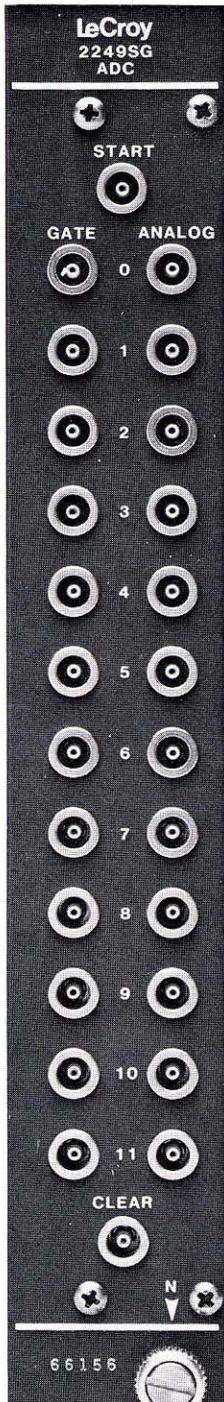
SPECIFICATIONS

Model 2249A

12 CHANNEL ADC

Analog Inputs:	Twelve; Lemo-type connectors; charge-sensitive (current-integrating); direct-coupled, quiescently at approximately +4 mV; 50 Ω impedance; linear range normally -2 mV to -1 V; protected to \pm 50 volts against 1 μ sec transients.
Full-Scale Range:	256 pC \pm 5%.
Full-Scale Uniformity:	\pm 5%.
Integral Non-linearity:	\pm .25% of reading \pm 0.5 pC (12 pC to 256 pC) for $>$ 500 Ω source.
ADC Resolution:	10 bits actual, (0.1%).
Long-Term Stability:	Better than 0.25% of reading \pm 0.5 pC/week (at constant temperature).
Temperature Coefficient:	Typical, 0; max., \pm [.03% of reading (in pC) + .002t] pC/ $^{\circ}$ C (where t = gate duration in nanoseconds, with 50 Ω reverse termination).
ADC Isolation:	A 5-volt, 20 ns overload pulse in any one ADC disturbs data in any other ADC by no more than 0.25 pC.
Gate Input:	One gate common to all ADC's; LEMO-type connectors; 50 Ω impedance; -600 mV or greater enables; minimum duration, 10 ns; maximum recommended duration, 200 ns (actual limit approximately 2 microseconds with reduced accuracy; partial analog input must occur within 0.5 μ sec after opening gate to preserve accuracy), effective opening and closing times: 2 ns; internal delay, 2 ns.
Fast Clear:	One front-panel input common to all ADC's; LEMO-type connector; 50 Ω impedance; -600 mV or greater clears, minimum duration, 50 ns. (Caution: narrower pulses cause partial clearing.) Requires additional 2.0 μ s settling time after clear.
Residual Pedestal:	Typically 1 + 0.03t picocoulombs (where t = gate duration in nanoseconds) with 50 Ω reverse termination.
Test Function:	With CAMAC I present, the positive DC level applied to front panel "Test" input (internal high impedance connection to +12 volts) or optional rear connector P1, P2, or P5 patch points will inject charge with a proportionality constant of -12.5 pC/volt into all inputs at F(25) \bullet S2 time. (With CAMAC I not present, F(25) \bullet S2 will generate the \approx 80 ns gate only, providing a measure of residual pedestal only.)
Digitizing Time:	60 μ s. By factory option, 8-bit operation at 12.5 μ s digitizing time may be provided.
Readout Time:	Readout may proceed at the fastest rate permitted by the CAMAC standard after digitization is complete.
Readout Control:	Ready for readout when LAM signal appears. Refer to ESONE Committee Report EUR4100e and EUR4600e for additional timing details, voltages, logic levels, impedances, and other standards.
Data:	The proper CAMAC function and address command normally gates the 10 binary bits plus overflow bit of the selected channel onto the R1 to R11 (2 ⁰ to 2 ¹⁰) Dataway bus lines.
CAMAC Commands:	Z or C: ADC's and LAM are cleared by the CAMAC "Clear" or "Initialize" command; requires S2. Z also disables LAM. I: Gate input is inhibited during CAMAC "Inhibit" command. (Test Function is enabled.) Q: A Q=1 response is generated in recognition of an F(0) or F(2) Read function or an F(8) function if LAM is set for a valid "N" and "A", but there will be no response (Q=0) under any other condition. The Q response for empty modules can be suppressed. (See Q and LAM suppression.) X: An X=1 (Command Accepted) response is generated when a valid F, N, and A command is generated. L: A Look-At-Me signal is generated from end of conversion until a module Clear or Clear LAM. LAM is disabled for the duration of N, can be permanently enabled or disabled by the Enable and Disable function command, and can be tested by Test LAM. Standard option causes LAM to be suppressed for empty modules.
CAMAC Function Codes:	F(0): Read registers; requires N and A, A(0) through A(11) are used for channel addresses. F(2): Read registers and Clear module and LAM; requires N and A; (Clears on A(11) only.) F(8): Test Look-At-Me; requires N and any A from A(0) to A(11) independent of Disable Look-At-Me. Q response is generated if LAM is set. F(9): Clear module and LAM; requires N, S2, and any A from A(0) to A(11). F(10): Clear Look-At-Me; requires N, S2, and any A from A(0) to A(11). F(24): Disable Look-At-Me; requires N, S2, and any A from A(0) to A(11). F(25): Test module; requires N, S2, and any A from A(0) to A(11). F(26): Enable Look-At-Me; requires N, S2, and any A from A(0) to A(11). Remains enabled until Z or F(24) applied. Caution: The state of the LAM mask will be arbitrary after power turn-on.
Q and LAM Suppression:	Adjustable potentiometer (accessed from side of module) sets count level required (from 0 to 100) before data is considered useful. A module in which all channels contain less than set amount will produce no Q-response or LAM and appears during readout as an empty CAMAC slot, thus reducing readout time. A Command Accepted response is still generated. The LAM suppress portion can be disabled with a solder jumper option.
Packaging:	In conformance with CAMAC standard for nuclear modules (ESONE Committee Report EUR4100e). RF shielded CAMAC #1 module.
Current Requirements:	+24 V at 35 mA; -24 V at 15 mA; +6 V at 850 mA; -6 V at 200 mA.





CAMAC Model 2249SG 12-Channel A-to-D Converter With Separate Gates

The LeCroy Model 2249SG 12-Channel Analog-to-Digital Converter is a separately gated version of the world's most widely used integrating ADC, the Lecroy Model 2249A. It embodies all the operational characteristics which have proved important for general-purpose use in high energy particle physics, including high resolution, high sensitivity, excellent stability, fast digitizing rate, LAM and Q suppression, provision for fast clear, calibrating test mode, and flexible LAM options.

The Model 2249SG contains twelve complete ADC's in a double-width CAMAC module. Each ADC offers a 10-bit conversion to provide a wide 1024-channel dynamic range. The input sensitivity of the Model 2249SG is 0.25 pC/count for a full-scale range of 256 pC. This is compatible with most available signal sources and no additional buffering or reshaping of any kind is required to digitize nanosecond pulses.

The excellent long-term stability, temperature characteristics, and isolation between ADC channels assure accurate and reliable performance under the demanding conditions encountered in actual experiments. Confirmation of operation and calibration is provided by a unique optional test feature which allows all twelve ADC's or an entire system to simultaneously digitize a charge proportional to a dc level provided to a front-panel Lemo connector or patched into P₁, P₂, or P₅ of the Dataway connector.

The Model 2249SG offers excellent event rate capability through the incorporation of a fast clear and a fast digitizing rate. The fast clear input enables each ADC to begin digitizing on the command of a prompt gate and be reset, if necessary, before the end of conversion on the basis of delayed logic or chamber information. This feature eliminates the long input delay cables now required in these situations.

End of conversion of modules which contain data is flagged by generation of a CAMAC LAM. Readout of modules which do not contain information can be eliminated either by use of the LAM signals or through Q suppression.

SPECIFICATIONS

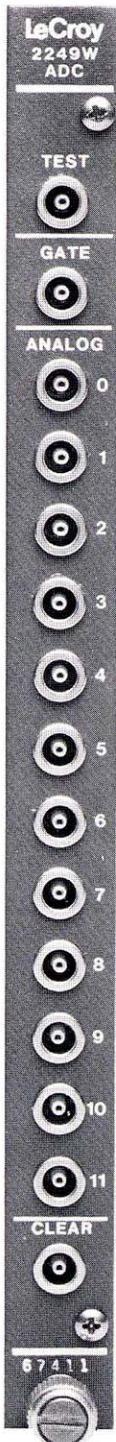
MODEL 2249SG

12-CHANNEL ADC WITH SEPARATE GATES

Analog Inputs:	Twelve, Lemo-type connectors; charge-sensitive (current-integrating); direct-coupled, quiescently at approximately +4 mV; 50 Ω impedance; linear range normally -2 mV to -1 V; protected to ± 50 volts against 1 μsec transients.
Full-Scale Range:	256 pC ± 5%.
Full-Scale Uniformity:	± 5%.
Integral Non-linearity:	± 0.25% of reading ± 0.5 pC for > 500 Ω source.
ADC Resolution:	10 bits (0.1%) somewhat degraded to approx. 0.2% by clock unsynchronized with any specific linear gate input.
Long-Term Stability:	Better than 0.25% of reading ± 0.5 pC/week (at constant temperature).
Temperature Coefficient:	Typical, 0; max., ±(.03% of reading (in pC) +0.002 t) pC/°C (where t=gate duration in nanoseconds, with 50 Ω reverse termination).
ADC Isolation:	A 5-volt, 20 nsec overload pulse in any one ADC disturbs data in any other ADC by no more than 0.25 pC.
Gate Inputs:	Twelve, one per ADC; Lemo-type connectors; 50 Ω impedance; -1.4 V or greater enables; minimum duration, 10 nsec; maximum recommended duration, 200 nsec (actual limit approximately 2 microseconds with reduced accuracy; partial analog input must occur within 0.5 μsec after opening each gate to preserve accuracy), effective opening and closing times; 2 nsec; internal delay, 2 nsec. All gates should occur within 2 μsec of the "start" pulse (other arrangements require internal resistor change). CAUTION: Subsequent gate signals are NOT INHIBITED after receipt of the first one, so care must be taken to externally prevent the application of more than one gate to each channel until a clear is applied.
Start Input:	A NIM level (> -600 mV) signal of a duration exceeding 10 nsec must be applied to start the internal oscillator. It should be applied simultaneous to the earliest gate pulse or should follow it by no more than 100 nsec.
Fast Clear:	One front-panel input common to all ADC's; Lemo-type connector 50 Ω impedance; -600 mV or greater clears, minimum duration, 50 nsec. (Caution: narrower pulses cause partial clearing.) Requires additional 1.5 μsec settling time after clear.
Test Function:	The standard 2249SG does not respond to F(25) and has no test feature. However, on-line test capability is optional at the expense of the CAMAC "Inhibit". With Q7 (the "inhibit" transistor) removed, the leading edge of a pulse applied to the "start" input will cause a fixed charge to be injected onto the 2249SG analog inputs. Coincident with the "start," the 12 gate pulses must be applied of duration approximately 80 nsec. Proportionality constant is -12.5 pC/volt of dc signal applied to P1, P2 or P5 patch points, for an 80 nsec gate. In this test mode, the gates must precede the "start" by 10 nsec.
Digitizing Time:	Approximately 60 μsec.
Readout Time:	Readout may proceed at the fastest rate permitted by the CAMAC standard after digitization is complete.
Readout Control:	Ready for readout when LAM signal appears. Refer to ESONE Committee Report EUR4100e and EUR4600e or IEEE #583 for additional timing details, voltages, logic levels, impedances, and other standards.
Data:	The proper CAMAC function and address command normally gates the 10 binary bits plus overflow bit of the selected channel onto the R1 to R11 (2° to 2¹⁰) Dataway bus lines.
CAMAC Commands:	Z or C: ADC's and LAM are cleared by the CAMAC "Clear" or "Initialize" command; requires S2. Z also disables LAM. I: Gate input is inhibited during CAMAC "Inhibit" command. (Nonfunctional if unit is modified to provide "Test" feature.) Q: A Q=1 response is generated in recognition of an F(0) or F(2) Read function or an F(8) function if LAM is set for a valid "N" and "A", but there will be no response (Q=0) under any other condition. The Q response for empty modules can be suppressed. (See Q and LAM suppression.) X: An X=1 (Command Accepted) response is generated when a valid F, N, and A command is generated. L: A Look-At-Me signal is generated from end of conversion until a module Clear or Clear LAM. LAM is disabled for the duration of N, can be permanently enabled or disabled by the Enable and Disable function command, and can be tested by Test LAM. Standard option causes LAM to be suppressed for empty modules.
CAMAC Function Codes:	F(0): Read registers; requires N and A, A(0) through A(11) are used for channel addresses. F(2): Read registers and Clear module and LAM; requires N and A; (Clears on A(11) only.) F(8): Test Look-At-Me; requires N and any A from A(0) to A(11) independent of Disable Look-At-Me. Q response is generated if LAM is set. F(9): Clear module and LAM; requires N, S2, and any A from A(0) to A(11). F(10): Clear Look-At-Me; requires N, S2, and A from A(0) to A(11). F(24): Disable Look-At-Me; requires N,S2, and any A from A(0) to A(11). F(26): Enable Look-At-Me; requires N, S2, and any A from A(0) to A(11). Remains enabled until Z or F(24) applied. Caution: The state of the LAM mask will be arbitrary after power turn-on.
Q and LAM Suppression:	Adjustable potentiometer (accessed from side of module) sets count level required (from 0 to 100) before data is considered useful. A module in which all channels contain less than set amount will produce no Q-response or LAM and appears during readout as an empty CAMAC slot, thus reducing readout time. A Command Accepted response is still generated. The LAM suppress portion can be disabled with a solder jumper option.
Packaging:	In conformance with CAMAC standard for nuclear modules (ESONE Committee Report EUR4100e or IEEE Report #583). RF-shielded CAMAC #2 module.
Current Requirements:	+24 V at 35 mA; -24 V at 15 mA; + 6 V at 850 mA; -6 V at 200 mA.

TECHNICAL DATA

LeCroy



CAMAC Model 2249W 12 Channel Analog-to-Digital Converter

The LeCroy Model 2249W is a 12 channel, 11-bit integrating-type analog-to-digital converter. It features excellent linearity and unprecedented stability, thus allowing operation at wide gates of up to 10 μ sec. Thus, the 2249W is compatible with CsI and NaI crystal detectors. Its minimum gate of 30 nsec makes its use with organic scintillators and Cerenkov detectors possible in all but the highest rate conditions.

The 2249W has been optimized for dynamic range and linearity. By AC-coupling the input, 11-bit (1980 counts) operation has been achieved with ± 2 count integral linearity. This excellent linearity is maintained from the smallest signal size to signals as large as -2 V.

The test feature allows all 12 ADC's to simultaneously digitize a charge proportional to a DC level provided to a front-panel connector or patched into the CAMAC Dataway connector. In addition, the pedestals alone can be checked on-line by the same test feature by removing the CAMAC inhibit (I) during the test.

The Model 2249W offers an excellent event rate capability through the incorporation of a 2 μ sec fast clear, which permits the ADC's to begin digitizing and then be cleared upon receipt of later trigger information rather than delaying the analog signals with long cables while the trigger decision is being made. In addition, rapid readout is made possible by a convenient Q and LAM suppress feature, side-panel adjustable between 0 and 100 counts. This feature permits an empty 2249W to be overlooked in a CAMAC readout cycle.

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SPECIFICATIONS

CAMAC Model 2249W

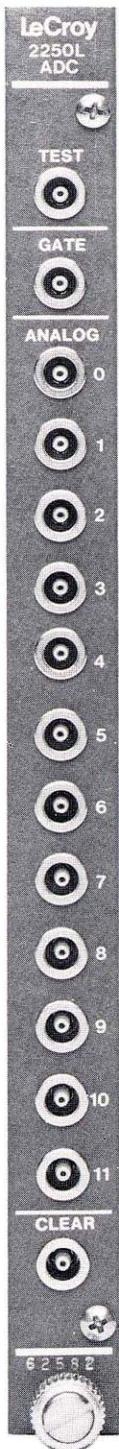
12 CHANNEL ANALOG-TO-DIGITAL CONVERTER

Analog Inputs:	12; Lemo type connectors; charge sensitive (current integrating); AC coupled (2 msec time constant, field changeable); 50 Ω impedance; linear range normally 0 to -2.0 V; protected to ± 50 V against 1 μsec transients.
Gain:	-0.25 pC/count ± 5%
Full-Scale Range:	Approximately -500 pC (maximum count ≈ 1980)
Integral Non-Linearity:	± 0.05% ± (0.5 pC + 0.1%)
ADC Resolution:	0.05% (1980 total counts)
Long Term Stability:	Better than 0.25% of reading ± 0.5 pC/week (at constant temperature)
ADC Isolation:	A 5 V, 20 nsec overload pulse in any one ADC disturbs data in any other ADC by no more than 0.5 pC (2 counts).
Gate Input:	One gate common to all ADC's; Lemo type connector; 50 Ω impedance; -600 mV or greater enables; minimum duration, 30 nsec; maximum recommended duration up to 10 μsec; partial analog input must occur within 0.5 μsec after opening gate to preserve accuracy; effective opening and closing times, 5 nsec; internal delay, 7 nsec.
Fast Clear:	One front panel input common to all ADC's Lemo type connector; 50 Ω impedance; -600 mV or greater clears, minimum duration, 50 nsec. Requires additional 2.0 μ sec settling time.
Pedestal:	Adjustable over approximately 100 counts via side-panel accessed trimmer capacitor. Somewhat higher for wide gate.
Test Function:	With CAMAC I present, the positive DC level applied to front panel "Test" input (internal high impedance connection to +12 V) or optional rear connector P1, P2, or P5 patch points will inject charge with a proportionality constant of -15 pC/V into all inputs at F(25)•S2 time. (With CAMAC I not present, F(25)•S2 will generate the gate only, providing a measure of the pedestal.)
Digitizing Time:	106 μsec
Readout Time:	Readout may proceed at the fastest rate permitted by the CAMAC standard after digitization is complete.
Readout Control:	Ready for readout when LAM signal appears. Refer to ESONE Committee Report EUR4100e and EUR4600e for additional timing details, voltages, logic levels, impedances, and other standards.
Data:	The proper CAMAC function and address command normally gates the 11 binary bits of the selected channel onto the R1 to R11 (2 ⁰ to 2 ¹⁰) Dataway bus lines.
CAMAC Commands:	Z or C: ADC's and LAM are cleared by the CAMAC "Clear" or "Initialize" command; requires S2. Z also disables LAM. I: Gate input is inhibited during CAMAC "Inhibit" command. (Test function is enabled.) Q: A Q = 1 response is generated in recognition of an F(0) or F(2) Read function or an F(8) function if LAM is set for a valid "N" and "A", but there will be no response (Q = 0) under any other condition. The Q response for empty modules can be suppressed (see Q and LAM suppression). X: An X = 1 (Command Accepted) response is generated when a valid F, N, and A command is generated. L: A Look-At-Me signal is generated from end of conversion until a module Clear or Clear LAM. LAM is disabled for the duration of N, can be permanently enabled or disabled by the Enable and Disable function command, and can be tested by test LAM. Standard option causes LAM to be suppressed for empty modules. F(0): Read registers; requires N and A; A(0) through A(11) are used for channel address. F(2): Read registers and Clear module and LAM; requires N and A: (clears on A(11) only). F(8): Test Look-At-Me; requires N and any A from A(0) to A(11) independent of Disable Look-At-Me. Q response is generated if LAM is set. F(9): Clear module and LAM: requires N, S2, and any A from A(0) to A(11). F(10): Clear Look-At-Me; requires N, S2 and any A from A(0) to A(11). F(24): Disable Look-At-Me; requires N, S2, and any A from A(0) to A(11). F(25): Test module; requires N, S2 and any A from A(0) to A(11). F(26): Enable Look-At-Me; requires N, S2 and any A from A(0) to A(11). Remains enabled until Z or F(24) applied. Caution: the state of the LAM mask will be arbitrary after power turn-on.
CAMAC Function Codes:	F(0): Read registers; requires N and A; A(0) through A(11) are used for channel address. F(2): Read registers and Clear module and LAM; requires N and A: (clears on A(11) only). F(8): Test Look-At-Me; requires N and any A from A(0) to A(11) independent of Disable Look-At-Me. Q response is generated if LAM is set. F(9): Clear module and LAM: requires N, S2, and any A from A(0) to A(11). F(10): Clear Look-At-Me; requires N, S2 and any A from A(0) to A(11). F(24): Disable Look-At-Me; requires N, S2, and any A from A(0) to A(11). F(25): Test module; requires N, S2 and any A from A(0) to A(11). F(26): Enable Look-At-Me; requires N, S2 and any A from A(0) to A(11). Remains enabled until Z or F(24) applied. Caution: the state of the LAM mask will be arbitrary after power turn-on.
Q and LAM Suppression:	Adjustable potentiometer (accessed from side of module) sets count level required (from 0 to 100) before data is considered useful. A module in which all channels contain less than set amount will produce no Q-response or LAM and appears during readout as an empty CAMAC slot, thus reducing readout time. A Command Accept response is still generated. The LAM suppress portion can be disabled with a solder jumper option.
Packaging:	In conformance with CAMAC standard for nuclear modules (ESONE Committee Report EUR4100e). RF shielded CAMAC #1 module.
Current Requirements:	143 mA at +24 V; 75 mA at -24 V; 725 mA at +6 V; 155 mA at -6 V

SPECIFICATIONS SUBJECT TO CHANGE

TECHNICAL DATA

LeCroy



CAMAC Model 2250L 12-Channel Buffered ADC

- * 12 independent ADC's in a single #1 CAMAC module
- * Event-buffered, 32-deep memory in each ADC channel
- * High sensitivity (0.5 pC/count)
- * Fast conversion, 9 bits in 9 μ sec.
- * Fast front-panel clear capability
- * Built-in test function
- * Standard CAMAC functions
- * Low power consumption

The LeCroy Model 2250L 12-Channel Analog-to-Digital Converter offers twelve complete integrating ADC's in a single-width CAMAC module. Each ADC channel digitizes to 9 bits the amount of charge received at the analog inputs over the duration of an externally applied common gate pulse. A full-scale output of the 2250L corresponds to an input charge of approximately 248 picocoulombs, providing sensitivity directly compatible with typical photomultiplier anode signals.

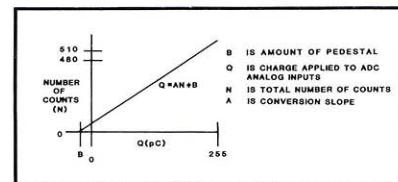
To permit a high rate data-taking capability, the Model 2250L offers a full-scale conversion to 9-bits in 9 microseconds. Within an additional 1 microsecond, the data is transferred to a 32-deep first-in first-out memory (FIFO), and the ADC front end is readied to accept another gate and thus another event. This technique allows 32 successive measurements to be made in each of the 12 ADC channels without necessitating full data readout.

The Model 2250L is part of LeCroy's growing line of data acquisition modules dedicated to the analysis of transient events, high speed, high sensitivity, and high density. Utilizing the widely accepted CAMAC modular design (as described in IEEE Report #583), the 2250L may be powered and housed and interfaced to a variety of computers and readout devices by standard off-the-shelf products from a variety of manufacturers.

November 1982

*Ideal for Thompson scattering experiments using multiple shot lasers!

Conversion Characteristics



SPECIFICATIONS

CAMAC Model 2250L

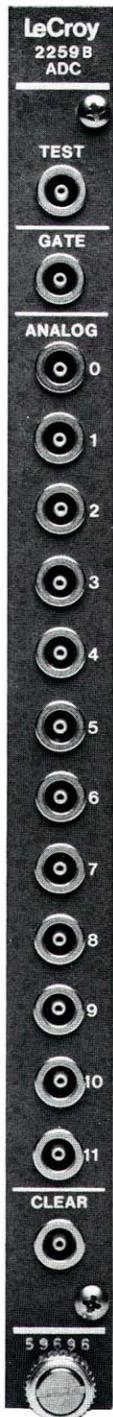
12-CHANNEL BUFFERED ADC

Analog Inputs:	12, Lemo-type connectors; charge-sensitive (current-integrating); direct-coupled; quiescently at approximately +3 mV; 50 Ω impedance; linear range normally 0 to -0.8 volts; protected to ±50 volts against 1 μsec transients.
Full-Scale Range:	Charge Input: Approx. 248 pC; Data Output: Approx. 9 bits (496 ± 10 counts).
Full-Scale Uniformity:	±5%.
Conversion Characteristics:	Linear, approx. 0.5 pC/count.
Integral Non-Linearity:	± 1 count above 10% of full scale; ± 2 counts over full range.
Long-Term Stability:	Better than 0.25% of reading ±2 counts/week (at constant temperature).
Temperature Coefficient:	Less than (0.025% of reading (in pC) + .0005t)pC/°C (where t = gate duration in nsec) with high impedance reverse termination.
ADC Isolation:	A 5-volt, 20 nsec overload pulse in any one ADC disturbs data in any other ADC by no more than 1 count.
Gate Input:	One gate common to all ADC's; Lemo-type connector; 50 Ω impedance; -600 mV or greater enables; minimum duration, 10 nsec; maximum duration, 200 nsec; effective opening and closing times, 2 nsec; automatically inhibits within 100 nsec after trailing edge of gate; input also inhibited for duration of CAMAC Inhibit.
Fast Clear Input:	Lemo-type connector; 50 Ω impedance; -600 mV or greater clears; minimum duration, 50 nsec; 1 μsec settling time.
Residual Pedestal:	Internally adjustable from zero to 10 pC. Factory adjusted to approximately 10 counts.
Test Function:	With CAMAC I present, the positive DC level applied to front panel "Test" input (internal high impedance connection to +12 volts) or optional rear connector P1, P2, or P5 patch points will inject charge with a proportionality constant of -12.5 pC/volt into all inputs at F(25)•S2 time. (With CAMAC I not present, F(25)•S2 will generate an 80 nsec gate only, providing a measure of residual pedestal only.)
Digitizing Time:	9 μsec full scale digitizing time plus 1 μsec transfer time to buffer.
Memory Buffer (FIFO):	32-word first-in-first-out memory for each of the 12 channels.
Readout Time:	Readout may proceed at the fastest rate permitted by the CAMAC standard after buffer transfer is complete. Asynchronous with data taking.
Readout Control:	Data ready to read out when Memory Data Ready (or LAM) appears.* S2 timing pulse of any valid read command readies next channel in sequence (Subaddress A + 1). Refer to ESONE Committee Report EUR4100e or IEEE #583 for additional timing details, voltages, logic levels, impedances, and other standards.
Data:	The proper CAMAC function and address command normally gates 9-bit word into the R1 to R9 Dataway bus lines; overflow condition is indicated by an all "1's" condition on upper five bits.
Conversion-In-Process:	Solder jumper option to desired patch point. Clamp to ground for duration of longest conversion time; maximum current, 16 mA.
Load Memory:	Solder jumper option to desired patch point. Clamp to ground will terminate conversion process, load memory, and clear scaler. Clamp current, 16 mA, minimum duration, 50 nsec; 1 μsec settling time. (Standard mode automatically loads memory and clears scaler 9 μsec after gate.)
Memory Full:	Solder jumper option to desired patch point; provides 16 mA clamp to ground when memory is full (=32 words).
Memory Data Ready:	Solder jumper option to desired patch point or LAM bus; provides clamp to ground when output word is ready (≥1 word).
CAMAC Commands:	Z or C: Scalers and FIFO memory are cleared by the CAMAC "Clear" or "Initialize" command; requires S2. I: Gate input is inhibited during CAMAC "Inhibit" command. Q: A Q=1 response is generated in recognition of an F(0) or F(2) Read function for a valid N and A (and data in FIFO memory), but there will be no response (Q=0) under any other condition. X: An X=1 (Command Accepted) response is generated when and only when a valid F, N, and A command is received. L: A Look-At-Me signal is optionally generated from end of conversion until a module clear. LAM is disabled for the duration of N, and can be permanently enabled or disabled by a solder jumper option.
CAMAC Function Codes:	F(0): Reads first output word in First-In-First-Out (FIFO) memory; requires "N", and "A", A(0) thru A(11) are used for channel addresses. F(0) • A(n - 1) needed to set up first time readout of channel n. F(2): Same as F(0), except also clears FIFO output word and shifts out next word during "S2" time. To readout channel n continuously use F(2) • A(n - 1). F(9): Clear scaler and FIFO memory (and LAM if used); requires "N", "S2", and any "A" from A(0) to A(11). F(25): Test function; provides an internal 80 nsec gate at S2 time (see Test function description); increments FIFO memories to load in test results. Requires "N", "S2", and any "A" from A(0) to A(11).
Packaging:	In conformance with CAMAC standard for nuclear modules (ESONE Committee Report EUR4100e or IEEE #583). RF shielded CAMAC #1 module.
Current Requirements:	+6 V at 1.5 A; -6 V at 180 mA; +24 V at 60 mA; -24 V at 175 mA

*To insure Channel 0 is ready, a F(0) • A(11) • N command could be generated (simultaneously for all N's) prior to a readout. NOTE: N(26) addresses all stations at once in the standard CAMAC interface.

TECHNICAL DATA

LeCroy



CAMAC Model 2259B

12-Channel, 11-Bit Peak-Sensing Analog-to-Digital Converter

For:

- Liquid argon ionization chambers
- NaI pulses
- BGO pulses
- Linear multiwire proportional chambers
- General peak-sensing applications

The Model 2259B 12-Channel CAMAC ADC is based on the design of the widely used Model 2259A. Digital sections are identical, utilizing the same synchronized oscillator circuit and low-power LeCroy Model SC100 Hybrid scaler section, directly interchangeable in either ADC. The analog front end of the 2259B employs the LeCroy Model VT100C Voltage-to-Time Converter, offering superior linearity, stability and peak-sensing/holding over previous versions.

The Model 2259B accepts negative-going analog inputs up to -2 V in amplitude within its linear dynamic range, giving an 11-bit digital output proportional to the peak of the pulse falling within an externally applied gate interval. The resultant ADC sensitivity is approximately -1 mV/count. The analog input signal should have at least a 50 nsec risetime. Because of the nature of the peak detector, the Model 2259B is insensitive to the falltime of the input pulse. The minimum recommended gate duration is 100 nsec, and should enclose the negative peak of the input pulse. Gate widths up to 5 μ sec may be employed. Digitizing time of the 2259B is fixed at approximately 106 μ sec.

In common with all new LeCroy CAMAC data acquisition modules, the 2259B offers a fast clear input (<2 μ sec total clearing time) to permit fast rejection of unwanted data before, during, or after conversion is complete, eliminating the need for long analog delays. In addition, a front panel test feature permits on-line testing of the entire ADC circuit. When F25 is applied, the 2259B generates an internal 100 nsec gate at S2 time. If the CAMAC I is present, the front panel "Test" input will inject a signal with a proportionality constant of -0.167 volt/volt into all inputs. If I is not present, the Test input is disabled; F25 will generate the internal gate at S2, but only the residual pedestal at the gate width will be measured.

The Model 2259B responds to the CAMAC Functions F0, F2, F8, F9, F10, F24, F25 and F26, and accepts or generates the following CAMAC commands: Z or C, I, Q, X, L. Packaging of the 2259B is a #1 width CAMAC module, conforming to IEEE Report 583. Current usage is low enough to permit the use of up to 23 2259B's (276 channels) in a single, standard, powered CAMAC crate.

December 1982

SPECIFICATIONS

Model 2259B

12-CHANNEL PEAK-SENSING ADC

Analog Inputs:	Twelve; Lemo-type connectors; voltage (peak) sensing; direct-coupled, quiescently at approximately + 0.5 mV; 50 Ω impedance protected to ± 100 V against 1 μsec transients; accepts either negative-going pulses of ≥ 50 nsec risetime or bipolar pulses with negative lobe first.
Gain:	(1 ± 0.05) counts/mV
Full-Scale Uniformity:	± 5%
Integral Linearity:	± (0.1% + 1 count) from 7% to 100% of full scale.
ADC Full Scale:	2020 ± 20 counts
Long-Term Stability:	Better than 0.25% of reading ± 4 mV/week (at constant temperature).
Temperature Coefficient:	Typical, 0; max., ± 0.03%/°C of full scale.
ADC Isolation:	A – 5 V, 100 nsec overload pulse in any one ADC disturbs data in any other ADC by no more than 5 mV.
Gate Input:	One gate common to all ADC's; Lemo-type connectors; 50 Ω impedance; – 600 mV or greater enables; minimum duration, 100 nsec; maximum duration, 5 μsec; effective opening and closing times, 2 nsec; internal delay, 5 nsec; must enclose negative peak of input pulse; dependance of position of pulse within the gate < 2 counts/μsec.
Fast Clear:	One front-panel input common to all ADC's Lemo-type connector; 50 Ω impedance; – 600 mV or greater clears; minimum duration, 50 nsec. (Caution narrower pulses cause partial clearing). Requires additional 2 μsec settling time after clear.
Pedestal:	35 ± 25 counts with dependance on gate width < 2 counts/μsec.
Test Function:	With CAMAC I present, the positive DC level applied to front panel "Test" input (internal high impedance connection to ≈ 10V) or optional rear connector P1, P2, or P5 patch points will inject signal with a proportionality constant of – 0.167 volt/volt into all inputs at F(25)•S2 time. (With CAMAC I not present, F(25)•S2 will generate 100 nsec gate only, providing a measure of residual pedestal only).
Digitizing Time:	106 μsec
Readout Time:	Readout may proceed at the fastest rate permitted by the CAMAC standard after digitization is complete.
Readout Control:	Ready for readout when LAM signal appears. Refer to ESONE Committee Report EUR4100e and EUR4600e for additional timing details, voltages, logic levels, impedances, and other standards. (Also IEEE Report 583).
Data:	The proper CAMAC function and address command normally gates the 11 binary bits of the selected channel onto the R1 to R11 (2 ⁰ to 2 ¹⁰) Dataway bus lines.

CAMAC COMMANDS

Z or C:	ADC's and LAM are cleared by the CAMAC "Clear" or "Initialize" command; requires S2.
I:	Gate input is inhibited during CAMAC "Inhibit" command. (Test Function is enabled).
Q:	A Q = 1 response is generated in recognition of an F(0) or F(2) Read function or an F(8) function if LAM is set for a valid "N" and "A", but there will be no response (Q = 0) under any other condition. The Q response for empty modules can be suppressed. (See Q and LAM suppression).
Z:	An X = 1 (Command Accepted) response is generated when a valid F, N and A command is generated.
L:	A Look-at-Me signal is generated from end of conversion until a module Clear or Clear LAM. LAM is disabled for the duration of N, can be permanently enabled or disabled by the Enable and Disable function command, and can be tested by Test LAM. Standard option causes LAM to be suppressed for empty modules.

CAMAC FUNCTION CODES

F(0):	Read registers; requires N and A. A(0) through A(11) are used for channel addresses.
F(2):	Read registers and Clear modules and LAM; requires N and A; (Clears on A(11) only).
F(8):	Test LAM; requires N and any A from A(0) to A(11) independent of Disable LAM. Q-response is generated if LAM is set.
F(9):	Clear module and LAM; requires N, S2, and any A from A(0) to A(11).
F(10):	Clear LAM; requires N, S2 and any A(0) to A(11).
F(24):	Disable LAM; requires N, S2 and any A from A(0) to A(11).
F(25):	Test modules; requires N, S2 and any A from A(0) to A(11).
F(26):	Enable LAM; requires N, S2 and any A from A(11). Caution: The state of the LAM mask will be arbitrary after power turn-on.
Q and LAM Suppression:	Adjustable potentiometer (accessed from side of module) sets count level required (from 0 to 200) before data is considered useful. A module in which all channels contain less than set amount will produce no Q-response or LAM and appears during readout as an empty CAMAC slot, thus reducing readout time. A Command Accepted response is still generated. The LAM suppress portion can be disabled with a solder jumper option.

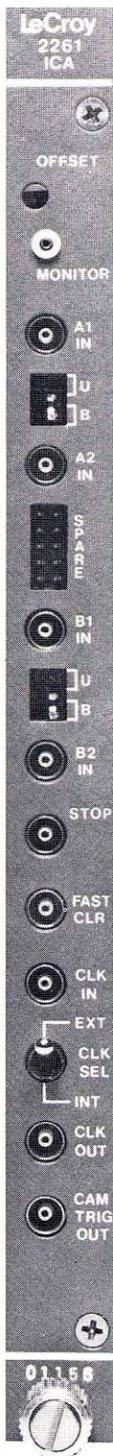
GENERAL

Packaging:	In conformance with CAMAC standard for nuclear modules (ESONE Committee Report EUR4100 or IEEE Report 583. RF-shielded CAMAC #1 module.
Current Requirements:	+ 24 V at 35 mA – 24 V at 15 mA + 6 V at 850 mA – 6 V at 200 mA

SPECIFICATIONS SUBJECT TO CHANGE

TECHNICAL DATA

LeCroy



CAMAC Model 2261 Image Chamber Analyzer

- 11-bit resolution
- 100 MHz sampling
- DC coupled
- CAMAC packaging

The Model 2261 is a CAMAC Image Chamber Analyzer based upon the LeCroy MVV200 high performance CCD. It is intended for readout of imaging devices such as dE/dx detectors, jet chambers and high speed TPC's. It is also a demonstrator for the MVV200, allowing efficient prototyping with the CCD. The Model 2261 provides 11-bit analog-to-digital conversion and clock rates to 100 MHz. This gives dramatically higher resolution than ever before available at such high sampling rates. Programmable logic allows any part of the record in memory to be accessed from the 2261 Memory.

The Model 2261 may be operated in 2 modes: Uniphase and Biphasic. In the Uniphase mode, the device provides 4 inputs and utilizes one CCD channel per input. This gives 320 samples (time buckets) at clock rates to 50 MHz. In the Biphasic mode, the 2261 provides two active inputs, utilizing two CCD channels per input. In this mode, the 2261 offers 640 samples at rates to 100 MHz. Front panel jumpers select between Uniphase and Biphasic modes.

Upon receipt of a NIM Common Stop signal, the Model 2261 begins conversion of the data. The device offers 1 mV least count with a range of 2 V. The operating range is front panel screwdriver adjusted allowing a range of -2 V to 0 V, 0 V to +2 V or any intermediate 2 V range to be selected. A test point at the front panel monitors the offset, indicating the most negative input value to facilitate setting.

Sample clocking is easily configured to specific applications. Any one of a wide range of plug-in hybrid crystal oscillators may be installed as the internal acquisition oscillator providing a stable asynchronous oscillator. For applications requiring synchronous clocking, a user supplied gated oscillator may be employed. In either case, a single reference may be used for a group of 2261s by utilizing the CLK OUT output to the external CLK IN of other 2261 modules.

To provide for special input conditioning requirements a front panel 10-pin header is provided. This header in conjunction with available space and hole patterns behind the front panel allow for user installation of custom designed input conditioning networks.

SPECIFICATIONS

Model 2261

CAMAC ICA MODULE

INPUT

Type: Lemo, impedance 50 Ω
 Number: 4 - Uniphase mode
 2 - Biphasic mode
 Bandwidth: Large signal - >30 MHz, 50 MHz typical. Small signal - 90 mV response in 10 nsec for a 100 mV step input.
 Dynamic Range: 2 V.
 Operating Range: Front panel screwdriver adjustment via front panel monitor point, common to all channels. Selects the lower level of the device range; i.e., the input level corresponding to a null output. Operating range may be set to cover -2 V to 0 V, 0 V to +2 V or anywhere in between.

OUTPUT

Samples: 320 for Uniphase 640 for Biphasic operation.
 Amplitude Resolution: 1 mV ± 10%. Digital format 12 bits. Active 2000 count range depends upon the input range selected. -2 V to 0 V corresponds approximately to 0 to 2000 counts. 0 to +2 V. Approximately to 2000 to 4000 counts.
 Amplitude Gain: 1 ± 3%
 Amplitude Temperature Coefficients: Gain <100 ppm/°C
 Pedestal <1 count/°C
 *Amplitude Linearity: ± 4 counts of best straight line over the operating range.
 *Interchannel Matching: Pedestal <100 counts
 (All four channels) Gain <1%
 *Random Noise: <500 μV rms
 *Spatial Noise: <5 mV p-p. This offset is stable to <1 mV under constant frequency duty cycle and constant temperature operation. The first two buckets and the last 2 buckets are not included in the spatial noise specification.
 Pedestal Droop: A linear change of offset from bin to bin caused by RSO (Rate of Signal Offset) at the CCD output. Increases with ambient temperature and/or acquisition clock rate. <0.03 mV/bin, typically <0.01 mV/bin.
 Interchannel Isolation: >70 dB

CLOCKING

Int/Ext: Front panel switch. Selects the source of the sample clock. Internal or External.
 Int CLK: Crystal controlled oscillator operating at 40 MHz (20 MHz Uniphase). Other crystals may be user installed.
 CLK IN: NIM standard input via a Lemo connector. Impedance 50 Ω Frequency Range: 1 MHz - 100 MHz. Minimum width 5 nsec. Every other negative-going edge causes sampling of the even numbered inputs. Alternate negative going edge samples the odd channels.
 CLK OUT: NIM Lemo 50 Ω Ungated representation of clock used to operate CCD channels in acquisition mode. May be used as monitor or as input source for another 2261 CLK IN, to achieve matching of sampling rates. Propagation delay CLK IN to CLK OUT: 8 nsec, typical.
 Common Stop: NIM Standard input via a Lemo connector. Impedance 50 Ω. Terminates acquisition and begins data conversion. Stop width >100 nsec, <100 μsec.
 CAMAC Trigger: Front panel NIM trigger output. Generates a NIM level of ≥200 nsec duration (equal to the CAMAC S1 pulse). Generated in response to an F(19) command.
 Fast Clear: NIM, Lemo 50 Ω terminates conversion

CAMAC FUNCTION CODES

F(0): Read Interleave Sequence of Biphasic channels; R1 = 0 indicates channel A1 first. R1 = 1 indicates channel A2 (B2) first.
 F(2)•A(0): Read dataword from Uniphase channel A1. Advance to next time bucket; A(8) performs identically.
 F(2)•A(1): Read dataword from Uniphase channel A2. Advance to next time bucket; A(9) performs identically.
 F(2)•A(2): Read dataword from Uniphase channel B1. Advance to next time bucket; A(10) performs identically.
 F(2)•A(3): Read dataword from Uniphase channel B2. Advance to next time bucket; A(11) performs identically.
 F(2)•A(4): Read dataword from Biphasic channel A. Advance to next time bucket; A(5), A(12), A(13) performs identically.
 F(2)•A(6): Read dataword from Biphasic channel B. Advance to next time bucket; A(7), A(14), A(15) performs identically.
 F(9): Enables the unit for data acquisition. Aborts data conversion if in progress. Disables Q response until new conversion is completed.
 F(17): Loads Memory Time Bucket Counter.
 F(19): Triggers CAMAC Trigger Output.
 X: For all F(0), F(2), F(9), F(17) and F(19) commands.
 Q: For all F(2) or F(17) if memory time bucket counter ≤319 on block transfer readout data valid until Q = 0. When Q = 0 response is generated memory time bucket counter automatically set back to 0.
 NOTE: Maximum time bucket counter value may be reduced by hardware option in module for specialized applications, reducing both conversion and readout time.

GENERAL

Digitizing Time: <6 msec
 Power: 550 mA at +6 V 300 mA at +12 V 50 mA at +24 V
 (at 100 MHz Biphasic) 950 mA at -6 V 400 mA at -12 V 25 mA at -24 V
 Packaging: In conformance with CAMAC standard for nuclear modules (ESONE Committee Report EUR4100 and IEEE #583). RF-shielded CAMAC #1 module.

OPTIONAL CRYSTALS

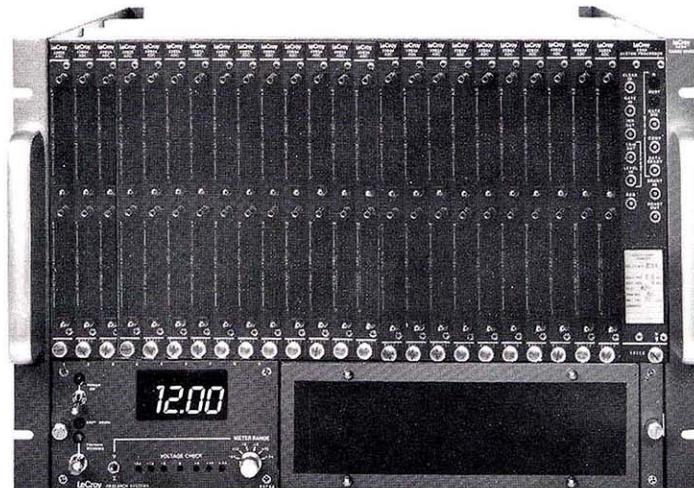
	Uniphase (MHz)	Biphasic (MHz)	Part Number
	10	20	309 040 020
	16	32	309 040 032
	25	50	309 040 050
	31.25	62.5	309 040 062
	35	70	309 040 070
	40	80	882 261 008
Standard	50	100	882 261 001
	20	40	309 040 040

*With respect to best straight line through RSO Characteristic

CAMAC System 2280

High Density ADC Data Acquisition System

- Large scale—low cost
- A complete system
- Up to 48 ADC channels per CAMAC station; 1008 channels per CAMAC crate.
- Data compression
- Wide dynamic range—12 bits
- Exceptional stability
- Automatic pedestal subtraction
- Sensitivity up to 10 counts per pC



LeCroy's System 2280 is a series of high density, low cost, charge ADC's in a configuration optimized for the largescale detector arrays typical of the latest generation of experiments. The elements of the system are the 2280 series ADC modules and the Model 2280 System Processor.

The ADC modules are of the highest density ever offered: Model 2282B offers 48 channels per #1 CAMAC module, while Model 2285A offers 24. This has been achieved through extensive reliance on monolithic technology within the hybrid ADC's. These are separate Wilkinson ADC's. Unlike intricate sample-and-hold designs, the separate ADC-per-channel design is less subject to interchannel cross modulation effects, does not rely on specialized low-leakage components, and is less sensitive to noise and RF pickup.

Lowest possible power consumption is attained by the use of CMOS technology for the scaler sections of the ADC's. This technology affords extremely low operating current.

The 2280 Processor is the heart of the system, managing up to 1008 ADC channels per CAMAC crate. Its purpose is to control the ADC modules and to receive and process data, making it available for conventional CAMAC readout. It unloads data from the modules via the dataway, subtracts pedestal, and loads compacted data into its own memory. This data compression technique allows for the fact that only a small fraction of all ADC channels will contain data for each event. This minimizes readout and computer processing time. During conversion and readout the system must be allowed exclusive access to the dataway. Other modules within the crate may be addressed only when the System Processor is inactive.

System Description

The LeCroy System 2280 consists of 1 to 21 ADC modules of a given type and one System Processor module. The ADC's are from the LeCroy 2280 series. Either peak- or charge-sensitive ADC's are available. System 2280 is configured to fulfill all of the functions of data acquisition for a large-scale experiment. These functions include:

- Data compacting (software selectable)
- Pedestal subtraction (software selectable)
- Test hardware
- Gate and fast-clear fan-out

A gate signal applied to the 2280 processor module is fanned out to the ADC modules by a rear panel ribbon cable called the Auxiliary Signal Bus (ASB). The fast-clear strobe, scaler clock, and other system overhead functions are similarly bused.

The system takes control of the CAMAC crate prior to the gate signal. Upon receipt of the gate, all ADC's begin scaling in parallel. After scaling, data are serially transferred from the ADC modules to the system processor via the dataway. Data are preprocessed by the 2280 module. Use of a hardwired processing scheme, rather than a microprocessor, allows data manipulation to proceed rapidly. Thus, compacted, pedestal-subtracted data are available for CAMAC readout as soon as transfer to the 2280 processor is complete.

ADC Modules

The ADC modules accept front panel input signals. Multicoax connectors provide high density, up to 48 channels per single width CAMAC module. Input signals are digitized in parallel (upon receipt of a common gate signal) by the Wilkinson rundown technique. High sensitivity over a wide dynamic range is achieved by a new series of LeCroy hybrids. These 24-pin dual in-line hybrids contain the circuitry to convert an analog input into a digital number and store that number until the 2280 processor is ready to receive it. Experience has proven that hybridization permits excellent interchannel isolation as well as very high sensitivity due to the reduction of stray capacitance and inductance resulting from the shortening of critical lead lengths.

The ADC's provide prompt, ungated summing outputs, permitting the use of the input signals in a trigger decision. Groups of analog outputs from selected channels may be tied together and then connected to on-board buffer amplifiers, giving rear panel sum signal outputs.

The ADC modules respond to a protocol generated by the 2280 System Processor and cannot be read by the crate controller. Each module has a unique address as defined by board-mounted jumpers. This allows each module to be addressed by the processor. Simultaneous readout of 12 channels at a time by serial transmission on R lines 13 through 24 allow rapid data transfer.

Model 2282B

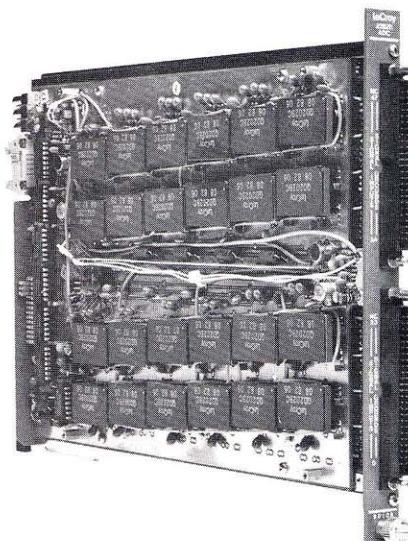
Model 2282B contains forty-eight 12-bit current integrating ADC's in a single width CAMAC module. Both offer excellent linearity over an exceptional dynamic range. The inputs are via two 25-signal connectors accepting $50\ \Omega$ multicoax ribbon cable. DC coupling is employed to eliminate rate effects. The gate is applied via the ASB from the System Processor. For wide gate operation, external AC coupling or high ($>10\ k\Omega$) source impedance is recommended for the inputs.

Use of monolithic technology allows far better component matching than in discrete designs. This allows the ADC to offer unprecedented stability. The 2282B can operate with gate widths up to $5\ \mu\text{sec}$ ($10\ \mu\text{sec}$ with widegate jumper option implemented) while maintaining excellent pedestal stability.

The 2282B provides quasi-differential inputs. This input configuration minimizes sensitivity to hum, common mode noise, and DC offsets. The signal grounds are commonly floated from chassis ground. Up to $\pm 200\ \text{mV}$ offset from chassis ground potential can be accom-

modated. This achieves a common mode rejection ratio of $>50\ \text{dB}$ for DC to $1\ \text{kHz}$. This circuit configuration is of great value in noisy environments typical of most laboratories. It affords excellent resolution even under wide gated DC-coupled operations.

The 2282B also affords channel-to-channel calibration of $<\pm 1\%$ when the Test Feature is exercised by the 2280 Processor.

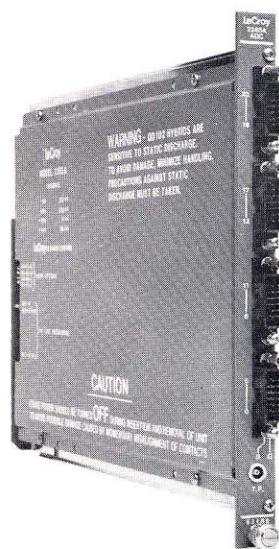


Model 2282B 48 Channel Current Integrating ADC

Each 2282B contains 24 QD202 series, dual channel hybrid ADC's. The circuit employs a LeCroy monolithic front end and a LeCroy monolithic 12-bit CMOS counter/shift register. The CMOS design dissipates less than 1mW per channel during conversion. The 2282B provides three prompt ungated analog sums, each of sixteen channels (0-15, 16-21, 32-47). These sums can be used in a second level trigger.

Model 2285A

The Model 2285A contains 24 current-integrating ADC's in a single-width CAMAC module, allowing up to 504 channels per CAMAC crate.



Model 2285A 24 Channel Current Integrating ADC

It has been designed as the highest performing version of System 2280. A 12-bit analog-to-digital conversion requires ~ 200 μ sec. Data transfer and compacting of an entire crate are accomplished in ~ 450 μ sec. The 2285A also offers quasi-differential inputs to eliminate sensitivity to hum, common-mode noise, and DC offsets.

The 10 counts/pC gain of the 2285A allows lower gain operation of the detector which can yield improved overall linearity of the system. A unique user selectable voltage-controlled gain mode allows the user to tailor the System 2285A to the experimental need. A user option allows higher sensitivity to be voltage programmed. See the performance table below.

2285A Performance Option Table

	10 counts/pC	30 counts/pC
INTEGRAL LINEARITY (0-1000 pC)	$\pm (0.25\% + 0.5 \text{ pC})^*$	$\pm (0.75\% + 0.5 \text{ pC})^*$
INTEGRAL LINEARITY (0-400 pC)	$\pm (0.1\% + 0.5 \text{ pC})$	$\pm (0.25\% + 0.5 \text{ pC})^*$
INTEGRAL LINEARITY (0-50 pC)	$\pm 0.2 \text{ pC}^*$	$\pm 0.2 \text{ pC}$
FAST CLEAR SETTLING (at 1.5 μ sec)	$\pm 0.2 \text{ pC}$	$\pm 0.2 \text{ pC}^*$
FAST CLEAR SETTLING (at 3.0 μ sec)	$\pm 0.1 \text{ pC}^*$	$\pm 0.1 \text{ pC}$
GAIN UNIFORMITY (From Mean)	$\pm 10\%$	$\pm 15\%^*$
RESIDUAL PEDESTAL (at 50 nsec)	$(25 \pm 10)\text{pC}^*$	$(25 \pm 15)\text{pC}^*$
RESIDUAL PEDESTAL (at 1000 nsec)	$(65 \pm 40)\text{pC}^*$	$(65 \pm 50)\text{pC}^*$

*Lot testing only

Each channel of the 2285A offers a prompt ungated analog output on the circuit board. Three rear panel buffer amplifiers allow the user to configure three analog sum outputs. These sums can be used in a second level trigger.

System Processor

The Model 2280 processor is a #2 CAMAC module. It supplies all needed signals to the ADC's by way of the CAMAC dataway and ASB. The ADC modules do not use N, S1 or S2 and are blind to the crate controller. In normal operation, after receiving the proper CAMAC command, the processor assumes control of the crate until after conversion. The crate control is assumed automatically with type A1 controllers or through auxiliary crate controller protocol with A2 controllers. The processor clamps the busy line low while it has control of the crate. During conversion only the processor must be allowed access to the dataway.

2280 Series Test and Maintenance

LeCroy's 2280 Series ADC's are extensively tested before delivery to the customer. The ADC Test System employed is based upon LeCroy's Model 3500 Data Acquisition and Control System. Special CAMAC Test Modules (LeCroy Model 1976 ADC/TDC Tester and 1987A 48 Channel Charge Fan-out) and an extensive software package have been developed to rapidly detect and diagnose malfunctioning ADC channels. This Test System is used by LeCroy Repair Facilities throughout the world to repair and maintain the tens of thousands of ADC channels in the field. Researchers with large numbers of 2280 Series ADC's in their data acquisition systems would find the ADC Test System a convenient and, in some cases, a necessary tool for shaking down, monitoring, and maintaining the performance of their experiment.

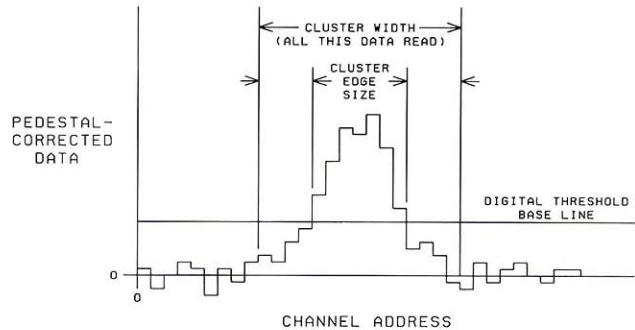
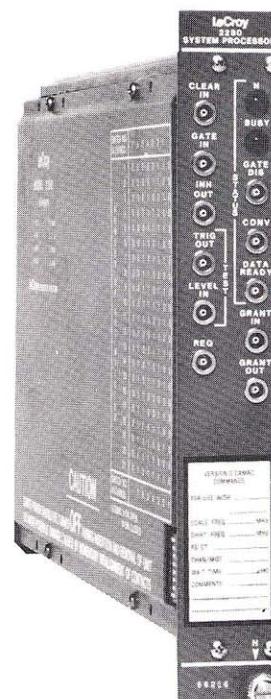


Figure 1—Data compression process. See 2280 System Processor specs.



Model 2280 System Processor

All channels of the ADC are tested at once. A series of tests are done in sequence on a pass/fail basis. A malfunctioning ADC hybrid is flagged on CRT hybrid map by "reversing color". (See Figure 2.) The ADC Test System performs the following tests on each ADC channel in a matter of seconds:

Gross Test is used as a quick initial screening. It picks out ADC channels which are badly malfunctioning. In this test the ADC outputs are recorded for zero and nominally full scale inputs. The difference between these values must fall between two limits. For 12-bit operation, these limits are 3000 to 4000 counts.

Pedestal Test—One pedestal value is measured for each channel at a gate width determined by the tester software. The pedestal value of each ADC must fall within limits. This test is supplemented by a measurement of the pedestal current described below.

Linearity Test—A series of 21 charge amplitudes are applied to all channels. Pulses cover the range Q_0 and Q_{20} in 5% steps. The values of Q_0 and Q_{20} are constants incorporated into the program and are dif-

ferent for the various ADC types. Weighted least squares routine is used to perform the fit. The linearity specification is used to determine the weighting factor. For example, the 2282A linearity specification is $\pm(0.25\% \text{ of reading} + 0.5 \text{ pC})$. As a result, the weighting of the i^{th} point is $(2.5 \times 10^{-3} Q_i + 0.5 \text{ pC})^{-1}$

For each charge amplitude and each channel, the deviation from the best fitted straight line is compared with the specification for the compliance. Any channel out of specification is indicated. The operator may request a more detailed report on any channel.

are found to differ from the asymptotic value by more than the fast clear specification, the ADC is repaired.

Pedestal Current—The pedestal is measured for the gate widths over the specified operating range of the unit. The slope of the resulting line is the input current or pedestal offset current. The value for all channels must lie within specified limits in order for the ADC module to pass.

The Model 3500-based Module Test System is easily expandable to test and maintain other LeCroy Systems, such as the LeCroy 4290 TDC System or the LeCroy HV4032A High Voltage Distribution System. For further information contact your local LeCroy Representative.



LeCroy Model 3500-based Module Test System

A typical response is shown in Figure 3. The horizontal axis represents input charge and the vertical axis represents deviation from linear fit. The vertical bars are the linearity specification so that compliance is indicated by the bar crossing the horizontal axis.

Gain is defined as the slope of the line determined in the linearity routine above. It is measured in counts per pC. If a given channel is not within specified limits, it is replaced or repaired.

Calibration Linearity is a routine similar to the procedure above used to measure input linearity. It employs the test input with voltage programming of the "Test Level In" of the 2280. It employs 21 voltage levels similar to the 21 charge amplitudes. The pass/fail criterion for the test circuit is less stringent than for the charge input.

Calibration Test—Gain data from the Linearity Test and the Calibration Linearity Test are compared. The two values must match to within the calibration accuracy specification.

Rate Test performs a gate-clear-gate sequence. The gate is 500 nsec wide with the fast clear following the gate leading edge by 1 μsec . The time from the clear to the second gate is varied under software control. It covers the range 2 to 8.6 μsec . Twenty times are selected over the range. The asymptotic pedestal is determined as an average of 5 values with an 800 μsec delay to the second gate. If any of the data

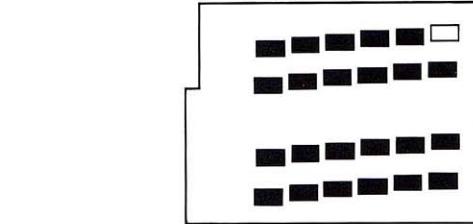


Figure 2—CRT display map of dual-channel ADC hybrids for the 2282A 48 channel ADC.

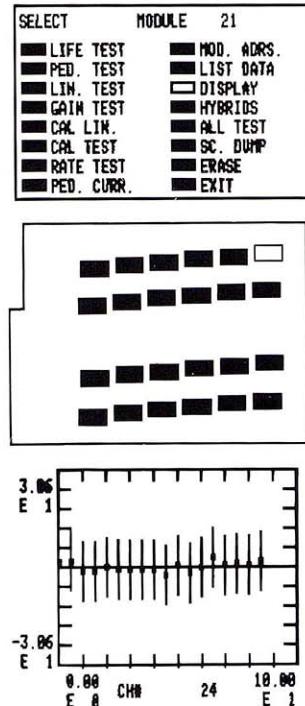


Figure 3—CRT display during ADC linearity testing. TOP: test selection table. MIDDLE: hybrid map. BOTTOM: graph of deviation from perfect linearity and allowable error for one ADC channel.

2280 SERIES ADC HIGHLIGHTS

Model No.	2282B	2285A
Input Sensing	Charge	Charge
ADC Resolution (Bits)	12	12
Channels Per CAMAC Station	48	24
Sensitivity Per Count	0.25 pC	0.10 pC
Gate Width Range (nsec)	50-10000	50-1500
Fast Clear, Full Scale to 1 Count (μsec)	<2	<2
Conversion, Scaling, and Transfer Time (msec)	1.75	0.65

SPECIFICATIONS

CAMAC Model 2282B

48 CHANNEL ADC



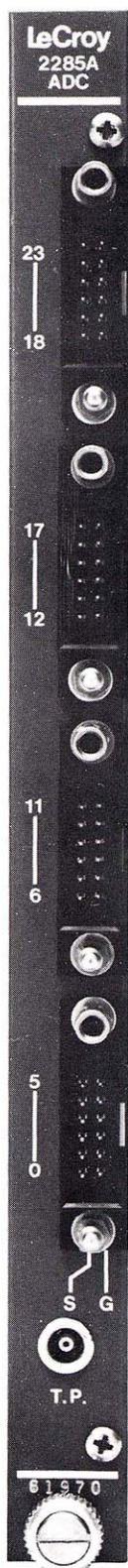
Input Sensing:	Charge (current integrating).
Full Scale:	– 1000 pC \pm 10%.
Gain:	– 4 counts/pC \pm 10%
Input Impedance:	50 Ω \pm 5%; 0 to – 50 mA DC.
Input Protection:	\pm 50 V for 1 μ sec transients.
Input Limitations:	Maximum voltage for linear response, – 1.5 V. For 3 V maximum input linearity is degraded to typically \pm (1% of reading + 0.25 pC).
Common Mode Properties:	Common Mode Rejection Ratio >50 dB for \pm 200 mV (DC to 1 kHz).
Integral Linearity:	Typically \pm (0.1% of reading of + 0.25 pC); worst case \pm (0.25% of reading + 0.5 pC) for signals of slew rate \le 2 mA/nsec. For signals of slew rate 4 mA/nsec linearity is degraded to typically \pm (1% of reading + 0.25 pC).
Differential Linearity:	Typically less than 5%.
Residual Pedestal:	Typically 125 counts (subtracted from data by processor) for a gate width of 100 nsec and high source impedance; 250 counts for 500 nsec gate width.
Pedestal-Gate Width Coefficient:	< \pm 50 fC/nsec for gate widths > 200 nsec plus 25 fC/nsec if wide gate jumper option is selected.
Temperature Coefficient:	Typically (– 0.05% of reading \pm 0.2 counts)/ $^{\circ}$ C for a gate width of \sim 1200 nsec. Coefficient may vary slightly for other gate widths.
Long-Term Stability:	\pm (0.25% of reading + 0.5 pC)/week at constant temperature and voltage.
Operating Temperature:	0 $^{\circ}$ to 40 $^{\circ}$ C.
ADC Resolution:	12 bits.
Conversion Time:	1 msec nominal + 35 μ sec per ADC module.
ADC Isolation:	> 60 dB, including the effects of one input connector.
Gate Input:	One per module, rear panel input driven from nonregenerative driver (via ASB) in 2280 System Processor module.
Gate Width:	50 nsec to 5 μ sec (10 μ sec if wide gate jumper option is implemented). In operation with wide gates, ADC conversion gain depends on pulse position in ADC gate time. This dependence is typically 0.6%/ μ sec.
Gate Timing:	The gate input to the 2280 System Processor must precede the analog inputs by \ge 50 nsec.
Fast Clear:	May be executed any time within 10 μ sec of a gate. Settles to within 1 count in < 2 μ sec.
Digital Clear:	A digital clear is automatically generated by a fast clear \ge 10 μ sec after the gate; requires 3 μ sec to settle.
Test Feature:	Exercised by 2280 System Processor. The charge pulse applied to all channels is proportional to the DC level at the Test Level Input (0 to + 10 V). Channel-to-channel matching of the constant of proportionality is < \pm 1%. For 0.0 V Test Level Input each channel's test input is a fixed value within the range 0 to 10 pC. Requires a gate width of \ge 1 μ sec. For further discussion see Application Note 1.
Analog Outputs:	Current outputs proportional to input (0.5 mA/mA). Risetime > 25 nsec, 10–90%. The three output buffers on rear panel are factory wired to sum three groups of 16 channels (0–15, 16–31, 32–47). Gate feedthrough is typically 80 mV (into 50 Ω) for 16 channels, recovered in approximately 120 nsec. Maximum output current for any buffer is 90 mA.
Readout and Control:	Requires one Model 2280/82A Processor per CAMAC crate. LeCroy 2282B's are compatible with 2282A's in the same crate.
Packaging:	No. 1 RF-shielded CAMAC module conforming to ESONE Report EUR 4100 and IEEE Standard 583.
Power Requirement:	770 mA at + 6 V 160 mA at + 24 V (Plus 1.5 times average input current) 750 mA at – 6 V 0 at – 24 V
Analog Input Connector:	AMP 102550-1 bulkhead-mounting 25-pair connector. Mates with AMP 2-226651-5 cable connector (AMP-latch series).
Analog Input Cable:	LeCroy Model DK25/50-Length. Includes AMP 2-226298-5 twenty-five signal ribbon coaxial cable with termination by AMP 2-226651-5 connectors at both ends (AMP-latch series), plus one AMP 102550-1 one bulkhead-mounting 25-pair connector.

SPECIFICATIONS SUBJECT TO CHANGE

SPECIFICATIONS

CAMAC Model 2285A

24 CHANNEL ADC



Input Sensing:	Charge (current integrating).
ADC Resolution: [†]	12 bits.
Full Scale: [†]	- 400 pC \pm 10%.
Common Mode Properties:	For \pm 100 mV, CMRR of 40 dB at 60 Hz, 30 dB at 1 kHz for source impedance $\geq 50 \Omega$.
Gain Variations: [†]	\pm 10% deviation from mean.
Input Impedance:	$50 \Omega \pm 5\%$; 0 to - 60 mA.
Input Protection:	± 25 V for 1 μ sec transients.
Input Limitations:	Maximum voltage for linear response, - 1.5 V. For 3 V maximum input linearity is degraded to typically \pm (1% of reading + 0.5 pC).
Integral Linearity: [†]	Typically \pm (0.1% of reading of + 0.25 pC); worst case \pm (0.25% of reading + 0.5 pC) for signals of slew rate ≤ 2 mA/nsec. For signals of slew rate 4 mA/nsec linearity is degraded to typically \pm (1% of reading + 0.5 pC).
Differential Linearity:	Typically 25%.
Residual Pedestal: [†]	Typically 50 pC (subtracted from data by processor) for a gate width of 200 nsec and a high source impedance.
Pedestal-Gate Width Coefficient:	$< \pm 50$ fC/nsec for gate widths > 100 nsec.
Temperature Coefficient:	Typically \pm (0.1% of reading + 0.00025 pC Δt)/ $^{\circ}$ C where Δt = gate width in nsec.
Long-Term Stability:	\pm (0.25% of reading + 0.5 pC)/week at constant temperature and voltage.
Conversion Time: [†]	200 μ sec nominal + 22 μ sec per ADC module.
Operating Temperature:	0 $^{\circ}$ to 40 $^{\circ}$ C.
ADC Isolation:	> 60 dB, including the effects of one input connector.
Gate Input:	One per module, rear panel input driven from nonregenerative driver (via ASB) in 2280 System Processor module.
Gate Width:	50 nsec to 1500 nsec. In operation with wide gates, ADC conversion gain depends on pulse position in ADC gate time. This dependence is typically 0.6%/ μ sec.
Gate Timing:	The gate input to the 2280 System Processor must precede the analog inputs by ≥ 50 nsec.
Fast Clear: [†]	May be executed any time. Settles from full scale to within 1 count (100 fC) in < 2 μ sec.
Digital Clear:	A digital clear is automatically generated by a fast clear ≥ 6 μ sec after the gate. Requires 3 μ sec to settle.
Test Feature:	Exercised by 2280 System Processor. All channels have a test pulse applied. The amplitude of the pulse is proportional to a DC level applied to the Test Input (0 to + 8 V), typically 47 pC/volt. Matching to nominal of the test pulse is \pm 10%. Requires a gate width of ≥ 300 nsec.
Analog Outputs:	Current outputs proportional to input (~ 0.5 mA/mA) available at each hybrid for summing by user. Risetime > 25 nsec, 10-90%. Three output buffers on rear panel allow option for additional current summing. Gate feedthrough is typically 80 mV (into 50Ω) for 16 channels, recovered in 80 nsec.
Readout and Control:	Requires one Model 2280/85 Processor per CAMAC crate.
Packaging:	No. 1 RF-shielded CAMAC module conforming to ESONE Report EUR 4100 and IEEE Standard 583.
Power Requirement:	770 mA at + 6 V 160 mA at + 24 V (plus 1.5 times average input current) 325 mA at - 6 V 0 at - 24 V
Special Options:	15-bit operation and variable gain. Specially modified System Processor (Model 2280/85/15) allows 15-bit conversion. Side panel accessed jumpers allow external voltage programming of ADC gain over the range 10 to 30 counts/pC. Voltage range + 6.3 V to 2.1 V. The model 2285A/15 is tested at both 12- and 15-bit operation and at both 10 and 30 fC per count. Model 2285A specifications include only 12-bit 10 count/pC gain operation. CAUTION: Sensitivity should be selected to give a full scale of 1000 pC or less.
Analog Input Cable:	LeCroy Model DK6/50-Length. 4 per module. Includes AMP 226298-6 six-pair ribbon coaxial cable with termination by AMP 226651-6 connectors at both ends, plus one AMP 87606-2 bulkhead-mounting 6-pair connector.

[†]Specifications marked with a [†] are based upon gain of 10 counts/pC (nominal), 12-bit dynamic range, and ambient temperature = 25 $^{\circ}$ C. For 15-bit operation see 2285A Performance Option Table on page 3.

SPECIFICATIONS SUBJECT TO CHANGE

SPECIFICATIONS

CAMAC Model 2280

SYSTEM PROCESSOR



FRONT PANEL INPUTS (LEMO TYPE CONNECTORS)

Gate: 50 Ω impedance. – 600 mV or greater enables. Distributed to ADC modules via ASB. Gates received after start of conversion are locked out. Use of gate disabled output recommended to avoid partial gating during enabling or fast clearing. 50 nsec minimum width.

Clear: Common to all ADC's. 50 Ω impedance. – 600 mV or greater enables. 50 nsec minimum width. (See individual ADC specifications for settling time.) Distributed to ADC modules via the ASB.

Test Level: During the test cycle a signal proportional to the applied voltage (internal high impedance connection to + 8 V) will be present at all ADC inputs about 20 nsec after gate opening. Distributed via ASB.

Grant In: Requires TTL clamp to ground (for Type A2 CAMAC controller).

FRONT PANEL LED's

(Internally stretched to 1 msec minimum)

N Light: Indicates when unit is being addressed.

Busy Light: Indicates when the Model 2280 has seized control of the CAMAC dataway.

FRONT PANEL OUTPUTS (LEMO TYPE CONNECTORS)

Test Trigger: Provides NIM level signal of 1 μ sec duration to trigger external gate logic when processor receives F(25)•A(1)

Gate Disabled: Provides TTL clamp to ground whenever processor is not ready to receive a gate.

Conversion: Provides TTL clamp to ground from trailing edge of gate until end of conversion.

Data Ready: Provides TTL clamp to ground from end of conversion, if data was stored in memory, until last word is read or unit is cleared.

Request: Provides TTL clamp to ground (for Type A2 CAMAC controller).

Grant Out: Provides TTL clamp to ground (for Type A2 CAMAC controller).

SYSTEM OPERATION

Conversion (Scaling & Data Transfer):

The System must first be enabled by an F(26)•A(4). This command causes the processor to take control of the CAMAC crate, which then causes the CAMAC BUSY to be clamped, resets the ADC's, and permits acceptance of an external gate to the processor (which is transmitted to the ADC's via the ASB). After a "wait" time (to allow for a fast clear) the processor supplies the scalar clock train required by the ADC's followed by readout of each module. Data of groups of twelve ADC channels are simultaneously shifted out serially to the processor via dataway buses R13 - R24. The data are converted to parallel form, preprocessed (see Pedestal Subtraction and Data Compression), and stored in the data memory. When all data are processed, the processor is automatically disabled, the BUSY line is released, and a LAM is generated.

The processor contains a 1024-word by 12-bit pedestal memory. This memory is loaded from the dataway by sequentially writing up to 1008 pedestal values using F(16)•A(0). If pedestal subtraction has been selected via coding of the F(16)•A(3) control word, incoming ADC data is automatically corrected before being loaded into the processor's memory.

Data Compression:	Data compression is performed by analyzing the data according to a user-entered digital threshold and cluster edge size. All data \geq threshold are stored in the data memory plus up to 15 channels of data on either edge of the region over threshold. Cluster blocks, which can be any length, are preceded in memory by the address of the first word in the cluster.
Reading of Actual Pedestal:	The control word register should be formulated so that Data Compression is not enabled, Pedestal Subtraction is not enabled, Data Transfer is enabled, and the Test Mode is not enabled. With no signal being applied to the analog inputs, a data-taking sequence, which can be initiated with F(25•A(1), will cause actual pedestal values to be stored in the data memory. Readout is accomplished via F(2)•A(0).
Reading of Stored Pedestal:	The control word register should specify that Data Compression is not enabled, Pedestal Subtraction is enabled, and Data Transfer is not enabled. A data-taking sequence will cause stored pedestal values to be stored in the data memory. Readout is accomplished via F(2)•A(0). The data will be a 16-bit two's complement of the actual pedestal value. This would be read by many 16-bit computers as "Pedestal."
Clearing:	Upon being enabled, the processor always fully clears the system to prepare it for a data-taking cycle.
CAMAC CONTROLS AND READOUT OF 2280 PROCESSOR	
CAMAC Readout:	Readout may proceed at the fastest rate permitted by the CAMAC standard after scaling and transfer are complete. (See CAMAC Function Codes.)
CAMAC Data:	The proper CAMAC function gates 16-bit data or status words into the CAMAC dataway. ADC data is presented with a starting address followed by consecutive data words gated onto the R1 to R15 bus lines. Overflow is indicated by all ADC bits being set high (4095 for a 12-bit ADC). R16 is a sign bit (1 = neg. data, as a result of pedestal subtraction from noisy data) and R15 is address flag (0 = address flag if R16 = 1).
CAMAC Commands:	<ul style="list-style-type: none"> C: Clear System; initializes data memory address register, word count register, pedestal memory address register, and LAM. Also issues analog (fast) clear to ADC modules. If the processor is enabled, a digital (slow) reset is also applied to the ADC modules. Z: Initialize system: same as C except also disables processor and LAM. Will not issue a digital reset to ADC modules. I: Gate Input of controller is inhibited during CAMAC "inhibit" command. (Connected via a jumper.) Q: A Q = 1 response is generated for all valid F(0) or F(2) commands (if data is contained in the data memory), all valid F(1) and F(16) commands, an F(27)•A(0) (if LAM is set independent of LAM mask), or an F(8)•A(0) if LAM is set and enabled. L: A Look-At-Me signal (when enabled) is generated as soon as the data of all ADC channels in the crate have been processed. LAM is cleared as soon as the first data word is read with F(2)•A(0). User jumper option allows LAM to remain true until all valid data words have been read. (Extended LAM).
CAMAC Function Codes:	<ul style="list-style-type: none"> F(0)•A(0): Read Data without advancing Address Register. F(2)•A(0): Read Data and advance Address Register; clears LAM. F(2)•A(1): Read Cluster Edge Size. F(2)•A(2): Read Digital Threshold. F(2)•A(3): Read Data Set Size (# of address and data words remaining in memory). F(8)•A(0): Test L; Q = 1 is generated if LAM is set and is not disabled by LAM mask. F(9)•A(0): Clear System: same as C above. F(10)•A(0): Clear LAM. Inoperative if extended LAM option is selected. F(16)•A(0): Write sequentially \leq 1008 12-bit pedestal values. Pedestal values are written in reverse order to data readout. Write "minus pedestal" in two's complement form. (Must be preceded by C, Z or F(9)•A(0) to initialize pedestal address register.) F(16)•A(1): Write Cluster Size; 4-bit word. F(16)•A(2): Write Digital Threshold; 16-bit word. F(16)•A(3): Write Control Word; 5-bit selects control option. W5 = Enable Positive Pedestal Mode. W4 = Enable Calibration Input. W3 = Enable Data Transfer (ADC's to processor). W2 = Enable Pedestal Subtraction. W1 = Enable Data Compression. F(24)•A(0): Disable L (mask LAM). F(25)•A(1): Enable Processor; generates 1 μsec test trigger pulse; independent of "Enable Calibration Input" control word option. F(26)•A(0): Enable L (mask LAM). F(26)•A(4): Enable Processor for data taking.

For proper system operation it is imperative that while a conversion is in progress no activity caused by the crate controller occurs on the dataway.

SPECIFICATIONS SUBJECT TO CHANGE
April, 1984



CAMAC Model 2323

Programmable Dual Gate and Delay Generator

- No dead time
- Accepts NIM, TTL or ECL inputs
- Programmable width
- Range 50 nsec to 10 sec
- Programmable delayed signal
- Manual or CAMAC control

LeCroy's CAMAC Model 2323 is a fully programmable gate and delay generator packaged with two channels in a double width CAMAC module. Its gate duration is programmable over the range 100 nsec to 10 seconds, covering a dynamic range of eight orders of magnitude. Outputs as short as 50 nsec can be selected at the expense of accuracy and stability. All settings may be programmed under CAMAC control or via front panel switches. Under CAMAC control, settings are overwritten whereas they are incremented under manual control. The Model 2323 offers excellent stability and jitter properties with 0.2% of Full Scale accuracy in the gate setting.

The Model 2323 offers both Start and Stop inputs. This allows the output pulse width to be determined by the Start - Stop time difference in the latched mode or by the internal timer in the preset mode. A Blanking NIM input causes a notch to be taken out of the gate, equal in duration to the blanking input. This is especially useful to gate off data acquisition during spurious periods. Conversely, a NIM OR input causes all outputs to be set to true for the duration of the OR inputs.

The unit offers NIM and NIM outputs equal in duration to the gate width selected. In addition, a DELAY output is produced at the trailing edge of the Gate pulse. The Model 2323 also provides a differential ECL output and a TTL output capable of driving a NIM Bin Gate. Both the ECL and TTL outputs may be driven from either the Gate or Delay circuit. These options are selected by board mounted shorting plugs.

The gate duration and width of the Delayed output are programmable under CAMAC control. Each of the two channels may be set independently. All values which are loaded into the Model 2323 may also be read back via CAMAC. Programming of the delay involves a ten bit "mantissa" and a three bit "characteristic".

The Start input is normally configured to accept NIM signals. A bridged high impedance input is employed to allow the trigger of more than one channel of 2323. The front end of the Start input consists of a comparator circuit, factory adjusted to trigger at -400 ± 50 mV. A front panel accessed multiple turn potentiometer allows the user to adjust the threshold over the range -3 V to $+3$ V. This allows the unit to be triggered by NIM, ECL, TTL or other standard logic signals. A front panel accessed switch selects either the positive-going or negative-going edge as the trigger. The stop input accepts NIM standard pulses.

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SPECIFICATIONS

CAMAC Model 2323

DUAL PROGRAMMABLE GATE AND DELAY GENERATOR

Gate Width

Range: 100 nsec to 10 sec; pulses to 50 nsec at reduced accuracy and stability
 Accuracy: $\pm 0.2\%$ of full scale (mantissa)
 Temperature Stability: $<200 \text{ ppm}/^\circ\text{C}$
 Jitter: $<0.2\%$ of setting
 Resolution: 0.1% of full scale (mantissa)

Delay Width

Range: 10 nsec to 300 nsec
 Width Options: 10 nsec, 30 nsec, 100 nsec, 300 nsec
 Accuracy: $\pm 20\%$

Inputs

START: Bridged high impedance pair. Lemo-type connectors. Input trigger level adjustable over the range $\pm 3 \text{ V}$ via front panel potentiometer. As supplied, the input is set to trigger at $-400 \pm 50 \text{ mV}$ with a negative going edge. Action of the input is to initiate the timing cycle.
 STOP: Standard NIM. Impedance 50Ω . Lemo-type connectors. Action of the input is to terminate the timing cycle in the latched mode. Active in both latched and preset modes. The delay is $<20 \text{ nsec}$.
 OR: Standard NIM input via Lemo-type connector. Input impedance 50Ω . Produces NIM, $\overline{\text{NIM}}$, ECL, and TTL outputs as long as the OR signal is asserted.
 BLANK: Standard NIM input via Lemo-type connector. Input impedance 50Ω . Cancels NIM, $\overline{\text{NIM}}$, ECL, and TTL outputs as long as the BLANK signal is asserted. Overrides OR input.

Outputs

BUSY LED: Indicates unit is active; duration stretched to 1 msec minimum.
 NIM: Standard NIM (-16 mA) signal via a Lemo-type connector. Goes low for gate duration. Risetime $\leq 2 \text{ nsec}$. Falltime $\leq 2.5 \text{ nsec}$.
 $\overline{\text{NIM}}$: Standard NIM (-16 mA) signal via a Lemo-type connector. Goes high for gate duration. Risetime $\leq 2 \text{ nsec}$. Falltime $\leq 2.5 \text{ nsec}$.
 ECL: One per section. Complementary ECL levels via a 2-pin connector. PC mounted shorting plug allows this output to be logically identical to the GATE or DELAY pulse or their complements.
 TTL: One per section. An FET open drain output ($+35 \text{ V Max}, 250 \text{ mA}, 0.5 \text{ W Max}$). PC mounted shorting plug allows this output to be logically identical to the GATE or DELAY pulse or their complements.
 DELAY: Standard NIM (-16 mA). Lemo-type connector. Delayed from start of NIM by the gate width. (Goes low at trailing edge of gate). Programmable for 10, 30, 100 or 300 nsec duration. Risetime $\leq 2 \text{ nsec}$.

CAMAC COMMANDS

F(1) • A(0) Read channel A programming word.
 F(1) • A(1) Read channel B programming word.
 F(9) • A(0) Stop channel A gate.
 F(9) • A(1) Stop channel B gate.
 F(17) • A(0) Write channel A programming word.
 F(17) • A(1) Write channel B programming word.
 F(25) • A(0) Start channel A gate.
 F(25) • A(1) Start channel B gate.
 C or Z Stops channels A and B gates.

Programming Word

M = mantissa
 C = characteristic
 L = latch bit
 D = delayed pulse width



Programmable mode: ($L=0$). Duration = $M \cdot 10^c \text{ nsec}$. (For $100 \leq M \leq 1023$). Settings of $50 \leq M < 100$ at reduced accuracy and stability.

Latched mode: ($L=1$). Duration = time between STOP and START inputs.

Delay Options:

D	Width
00	10 nsec
01	30 nsec
10	100 nsec
11	300 nsec

General

Input-Output Delay: 24 nsec (Start input to NIM output).
 Recovery time: None. The unit may be retriggered any time after the timing cycle has been completed.
 Packaging: Double width module in conformance with CAMAC standard for nuclear modules. (ESONE Report EUR4100 or IEEE Report #583.). RF shielded CAMAC #2 module.
 Power Consumption: 1.8 A @ +6 V
 1.3 A @ -6 V
 50 mA @ +24 V
 75 mA @ -24 V

SPECIFICATIONS SUBJECT TO CHANGE



CAMAC ECLine Model 2365 Octal Logic Matrix; 16 × 8

- CAMAC logic
- ≥ 75 MHz throughput
- 16 inputs per #1 CAMAC
- Logic fan-in
- Coincidence
- Complementing input and output
- Fast veto
- Continuous memory – battery backup
- Analog multiplicity output

The Model 2365 Octal Logic Matrix is a versatile programmable 100 MHz logic unit designed for trigger applications involving high speed logic arrays. It allows complete programmability of all of the logic functions which it provides. The unit is ideal for specifying triggers based upon roadways through hodoscope arrays. An analog multiplicity output via a front panel Lemo Connector is provided for triggering on multi track events.

The Model 2365 accepts 16 differential ECL inputs. These signals are applied to each of the eight independent logic channels. The outputs are differential ECL levels on a standard ECLline header. Two outputs are provided per channel. The 16-bit input size is most useful for large counter arrays. Wide 16-bit input width minimizes the need for cascading of logic units. This results in lower cost and shorter overall trigger propagation delay.

The logic matrix for the Model 2365 is shown in figure 1. Each channel is comprised of a series of programmable select gates which allow a wide variety of boolean logic combinations to be assigned. These functions include:

- Input selection** — switchyard
- Complementing** — input and output
- OR** — logic fan-in
- AND** — coincidence
- Veto** — via complementing function

A CAMAC-loadable Test Register, CTR, in the Model 2365 adds to the versatility of the unit. This register may be used as one of the diagnostics for complete CAMAC checkout of the trigger logic. The 16-bit pattern, loaded into the Test Register, may be applied to the inputs of the logic matrix by a CAMAC command, thereby deselecting 16 front panel logic inputs. This operation simulates logic inputs for testing purposes. The eight outputs of the logic matrix may also be read via CAMAC.

The CTR also allows for a sophisticated veto. A consequence of the versatility of the Logic Matrix is that the quiescent states of its outputs are defined by the application. For this reason, the Test Register is used in the veto circuit. Application of a fast front panel ECL Veto Enable signal sets the inputs to the pattern stored in the Test Register for the duration of the Veto Enable pulse (≥ 10 nsec). If the quiescent input levels are loaded in the Test Register, proper veto operation is achieved.

The Model 2365 provides many logic functions never before feasible in such a compact format. Together with the other members of the ECLline logic family, it allows an economical and versatile prompt trigger to be configured under computer control.

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SPECIFICATIONS

ECLine Model 2365

OCTAL LOGIC MATRIX; 16 × 8

INPUT CHARACTERISTICS

Number of Inputs:	16, direct coupled; 100 Ω, high Z by user option; reflections < 10% for signals of ≥ 2 nsec risetime.
Input Width:	≥ 5 nsec fwhm
Maximum Rate:	≥ 75 MHz
Input Connector:	17-pair front-panel header
Veto Enable:	Differential ECL input via two pin header. Input impedance 100 Ω, high Z by simple user modification. When asserted, the contents of the 16-bit CAMAC-programmable test register (CTR) are applied to the logic matrix overriding the front panel inputs. Minimum width 5 nsec. Must precede the Input by ≥ 5 nsec.

OUTPUT CHARACTERISTICS

Logic Outputs:	Two per channel, sixteen total; ECL levels via a 34-pin header with pinouts to match the ECLine standard. Output width equals duration of logic condition.
Output Rate:	≥ 75 MHz
Propagation Delay:	< 10 nsec
Analog Multiplicity:	Front panel Lemo output provides 2 mA for each logic matrix output in the logical 1 state. Rise and falltime < 4 nsec.

MEMORY PROTECTION

Continuous Memory:	Memory battery back up. This feature preserves contents of memory and CTR during CAMAC power down. Life of the battery is two years of operation.
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MODE CONTROL

Front Panel:	The sixteen ECL input levels are applied to the octal logic matrix (8LM). Selected by the CAMAC Mode Selector bit.
Test:	The contents of the 16-bit CTR are applied to the 8LM. Selected by the Mode Selector bit.
Veto:	The contents of the CTR are applied to the 8LM. Selected via front panel Veto Enable input.

SOFTWARE SELECTED LOGIC COEFFICIENTS (See Figure 1)

A _{i,j}	AND Selector. When set to logical 1, routes the compliment of the i th input to the j th logic matrix OR. When A _{i,j} = 0, compliment unused.
B _{i,j}	OR Selector. When set to logical 1, routes the i th input to the j th logic matrix OR. When B _{i,j} = 0 normal signal unused.
C _j	Output Complimentor. When set to logical 1, routes the compliment of the j th logic matrix OR to the i th output. When C _j = 0, the normal OR is used.

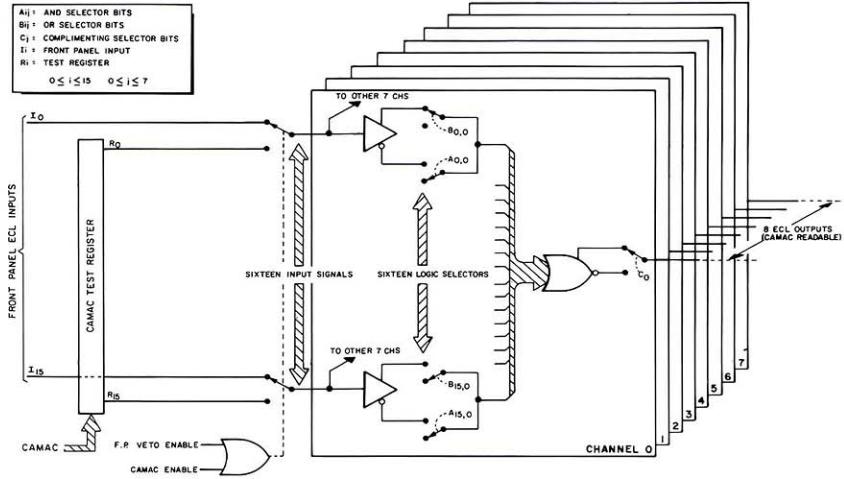
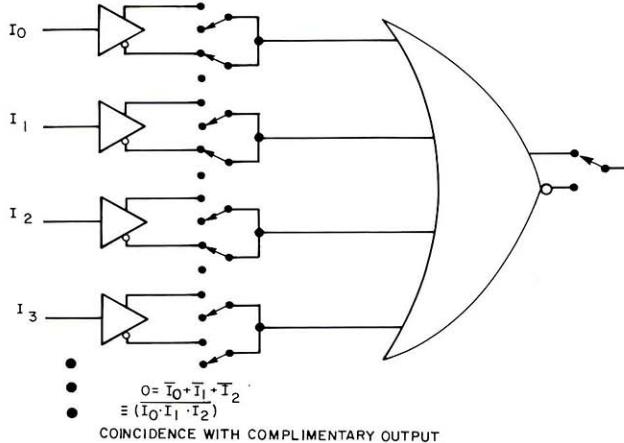
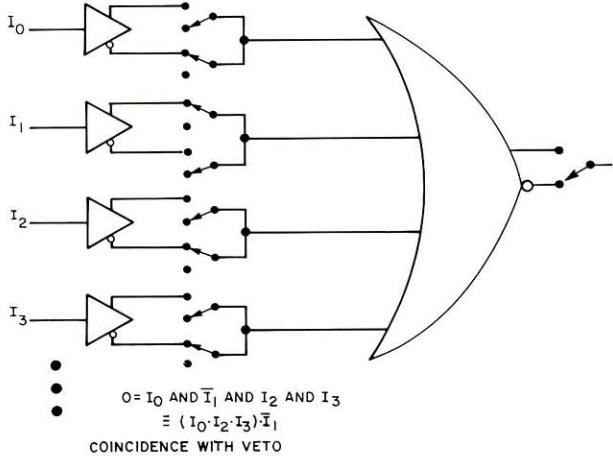
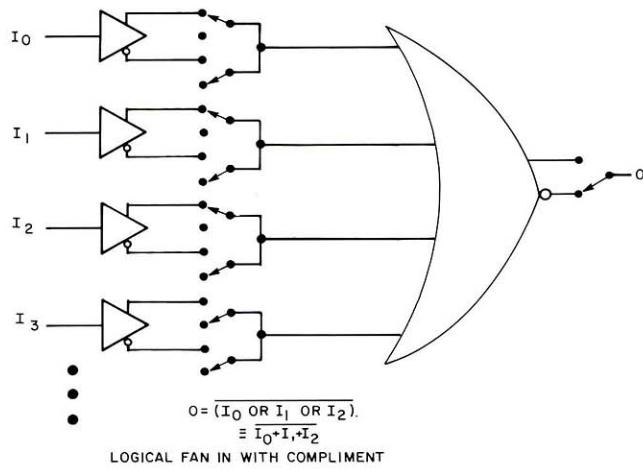
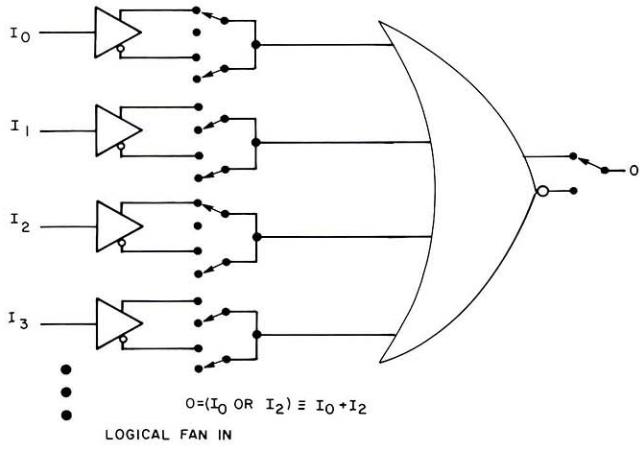


Figure 1

APPLICATION EXAMPLES



BIT MAP

Logical Designation	Logic Coefficient Word (16 bits)			Programming Designation
B _{i,0}	B _{15,0}	•	•	PW0
A _{i,0}	A _{15,0}	•	•	PW1
B _{i,1}	B _{15,1}	•	•	PW2
•	•	•	•	•
•	•	•	•	•
•	•	•	•	•
A _{1,7}	A _{15,7}	•	•	PW15
C _j	X • • • X	C ₇	• • •	PW16
T _i	T ₁₅	•	•	PW17

CAMAC COMMANDS

- F(0)•A(0): Read 18 sixteen-bit programming words. Eighteen successive read commands must be done to complete read operation and reinitialize the 2365 for logical operation.
- F(0)•A(1): Read 16-bit input pattern. The ECL logic levels at the input must be static during the read cycle.
- F(0)•A(2): Read 8-bit output word. Outputs must be static during the read cycle.
- F(0)•A(3): Read Mode Selector bit (0 indicates Front Panel mode, 1 indicates Test mode).
- F(9)•A(0): Initialize the 2365. This operation is required on power up.
- F(16)•A(0): Write eighteen 16-bit programming words. Requires 18 successive write commands.
- F(16)•A(3): Write Mode Selector bit (0 indicates Front Panel mode, 1 indicates Test mode).
- X: An X = 1 response is generated for any valid N•F•A.
- Q: A Q = 1 response is generated for F(0)•A(0) and F(16)•A(0). A Q = 0 response is generated at the 18th successive command (terminal count). This Q response is valid only if a F(9)•A(0) has been performed at power up.

GENERAL

- Packaging: In comformance with CAMAC standard for nuclear modules (ESONE Committee Report EUR4100 or IEEE Report 583. RF-shielded CAMAC #1 module.
- Current Requirements: < 400 mA at + 6V
 < 2.5 A at - 6V

SPECIFICATIONS SUBJECT TO CHANGE



CAMAC Model 2372

Memory Lookup Unit

- For trigger processors and complex triggers
- Arbitrary user defined transfer function
- High capacity/speed
- Transparent or strobed mode
- 64 K-bit dual-ported RAM
- Access time 60 nsec
- Battery backup—2 year integrity
- 16-bit front panel Data-in, Data-out connectors

The Model 2372 is a 64 K-bit dual-ported random access memory based upon the Fermilab module ECL-2. Its access time is ≤ 60 nsec. Packaged in a single-width CAMAC module, the unit offers an exceptionally high capacity/speed product while dissipating < 12 W. Battery backup maintains the integrity of the data within the 2372 (for 2 years) when the CAMAC crate is shut off. This continuous memory feature is particularly useful during the startup phases of an experiment. The MLU serves as a fundamental element of a trigger processor. It also may be used to provide complex functions required of trigger logic.

In normal use, the MLU is first downloaded with the required trigger data and then verified via CAMAC. This information, which defines the function of the MLU, is accessed via the front panel for real time applications. The Model 2372 offers 16-bit front panel Data-In and Data-Out connectors, although not all 32 bits may be used at once. The dimensionality of the Model 2372 is selected via CAMAC to serve the application. The dimensionality options are:

DIMENSIONALITY	INPUT WORD SIZE	MEMORY SIZE (WORDS)	OUTPUT WORD SIZE
0	16	64 K	1
1	15	32 K	2
2	14	16 K	4
3	13	8 K	8
4	12	4 K	16

The function of the MLU may be user defined to meet the application. The required function is downloaded via CAMAC. Virtually any function may be defined: angle logic or clusterized track multiplicity are examples of complex trigger functions. When used as a trigger processor element, the MLU may be used for any operation which is a one-to-one mapping. In conjunction with an ADC, the MLU can be loaded with the calibration to energy. The MLU can also be loaded with a digital comparator function or any arithmetic calculation, e.g. $E_1 + E_2$, $E/c \sin\theta$, $(X^2 + Y^2)$.

The strobe facilities of the Model 2372 are used in the software selectable Strobed Mode. In this mode, the MLU is strobed by the ECL Input Enable signals, coming from previous logic unit(s). After 60 nsec, the output "word" of the MLU becomes valid along with four ECL Output Ready signals which may be used to strobe the output word into other modules like the 2372. The output word remains static until another Input Enable is received. This automatically accounts for the propagation delay of the unit. Four Output Ready's are supplied to allow the 2372 to drive multiple logic units. Four Input Enables are provided with an Enable condition being defined as their coincidence (unused inputs are set to logical 1).

The Model 2372 may also be used without regard to the strobe logic. In the Transparent Mode, the output of the Model 2372 may change without regard for the Input Enables. This mode bypasses the latch circuitry and thus provides a slight speed advantage, offering a throughput time of only 55 nsec. This difference is reflected in the Input Enable, Output Ready timing when the Transparent Mode is selected.

October 1982

SPECIFICATIONS

CAMAC Model 2372

MEMORY LOOKUP UNIT

INPUTS

Input Word:

Up to 16 bits, ECL levels via 17-pair header. Pin-outs match ECL Standard. Impedance $100 \Omega \pm 5\%$, high impedance by simple user modification. Minimum width 10 nsec in the Strobed mode or 65 nsec in the Transparent mode. Number of active bits depends upon Dimensionality.

Input Enable:

Four differential ECL inputs via 2-pin headers. Required only in Strobed mode. Must arrive ≥ 2 nsec after Input word is settled. Minimum width—Strobed mode: 10 nsec, Transparent mode: 65 nsec (if used).

OUTPUTS

Output Word:

Up to 16 bits, ECL levels via 17-pair header. Pin-outs match the ECL Standard. Output width depends upon Operating mode. Number of active bits depends upon Dimensionality.

Output Ready:

Four differential ECL outputs via 2-pin headers. Occurs ≥ 5 nsec after the outputs are settled.

Propagation Delay:

60 nsec. Input Enable to Output Ready—Strobed mode. Transparent mode: 20 nsec after a new Input word becomes valid, the Output word becomes indeterminate. The correct Output word appears within 55 nsec of the new Input word.

CONTROL

Dimensionality Control:

CAMAC selected via CAMAC Control Register (CCR). Defines the number of inputs and outputs.

Mode Control:

CAMAC selected via CCR.

Strobed Mode—The leading Edge of Enable condition (and of four Input Enables, unused inputs set to logical 1 state) latches Input word. Output Ready's become false within 30 nsec. Output word becomes invalid within 30 nsec. New Output word settled and Output Ready's true within ≤ 60 nsec. Ready and Output word remain until the next Enable condition.

Transparent Mode—operates without regard to Input Enables. Output word present for duration of input word after approximately ≤ 55 nsec delay.

Inhibit Mode—disables front panel inputs to allow CAMAC programming of memory.

MEMORY PROTECTION

Continuous Memory:

Memory battery back-up. This feature preserves contents of memory and CCR during CAMAC power down. Life of the battery is two years of operation.

CAMAC COMMANDS

F(0)•A(0):

Read 1 to 16-bit Output word addressed by CAMAC Address Register (CAR). Increment CAR. Requires operation in Inhibit mode. Inactive bits are not masked and are arbitrary.

F(0)•A(1):

Read 16-bit CAR address. Requires operation in Inhibit mode. Inactive bits are set to 1 if F(16)•A(1) was executed after power up.

F(0)•A(2):

Read 5-bit CCR word.

F(0)•A(3):

Read 1 to 16-bit Output word addressed by front panel Input word. Inactive bits are not masked and are arbitrary.

F(0)•A(4):

Read 12 to 16-bit front panel Input Word.

F(16)•A(0):

Write 16-bit word into memory location addressed by CAR. Requires operation in Inhibit mode. Write commands are performed with dimensionality of four. See Owner's Manual.

F(16)•A(1):

Write 12 to 16-bit CAR address. Dataword at ECL output will change accordingly. Requires operation in Inhibit mode.

F(16)•A(2):

Write 5-bit CCR word.

Q:

A Q=1 response is generated for F(16)•A(0) and F(0)•A(0), A Q=0 response is generated for these commands when CAR reaches terminal count. This Q Response is valid only when CAR has been loaded via F(16)•A(1) after power up.

An X=1 response is generated for any valid N•F•A.

PROGRAMMING WORDS

CAMAC Control Register (CCR)

D = Dimensionality
M = Mode Control

W5	W4	W3	W2	W1
M	D			

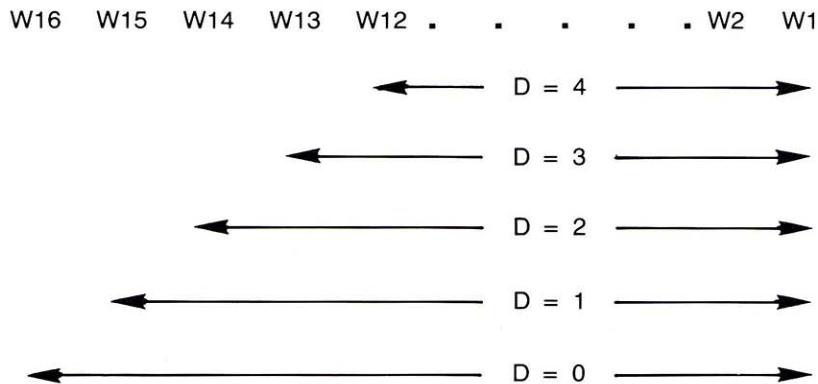
DIMENSIONALITY OPTIONS

D	Dimensionality
0 0 0	0 ; 16 in/1 out
0 0 1	1 ; 15 in/2 out
0 1 0	2 ; 14 in/4 out
0 1 1	3 ; 13 in/8 out
1 X X	4 ; 12 in/16 out

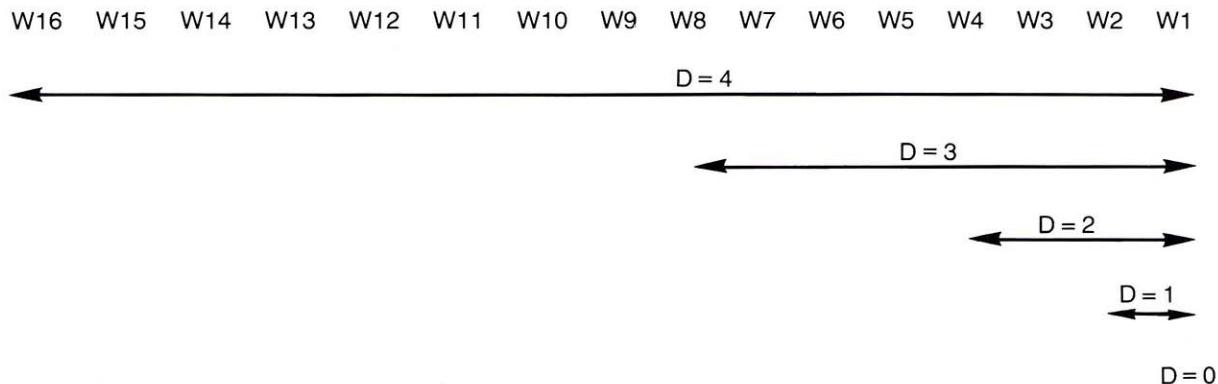
MODE OPTIONS

M	Mode
0 0	Strobed
0 1	Transparent
1 X	Inhibit

CAMAC Address Register (CAR)



Output Word (OW)



GENERAL

Packaging:

In conformance with CAMAC Standard for Nuclear Modules (ESONE Committee Report EUR4100). RF shielded CAMAC 1 Module.

Power:

< 1.25 A at + 6 V
< 850 mA at - 6 V

SPECIFICATIONS SUBJECT TO CHANGE



ECLine Model 2375 Data Stack Module

- Trigger Processing
- Multiple Event Buffer
- High Speed: 50 nsec cycle time
- High Density: 256 sixteen-bit words
- Dual Ported: simultaneous read/write
- Self Sequencing

The Model 2375 is a Data Stack designed for use with the LeCroy family of ECLline Trigger Processor modules. It is a fast 256×16 memory with separate read and write ECLports, based upon the Fermilab ECL 4 module. A block diagram of the Stack is shown below. The Model 2375 is ideal for rapid processing of lists of data from a variety of sources, such as the ECLport outputs of the PCOS III and FERA system. It may also be used as an Event Buffer in conjunction with these data acquisition systems.

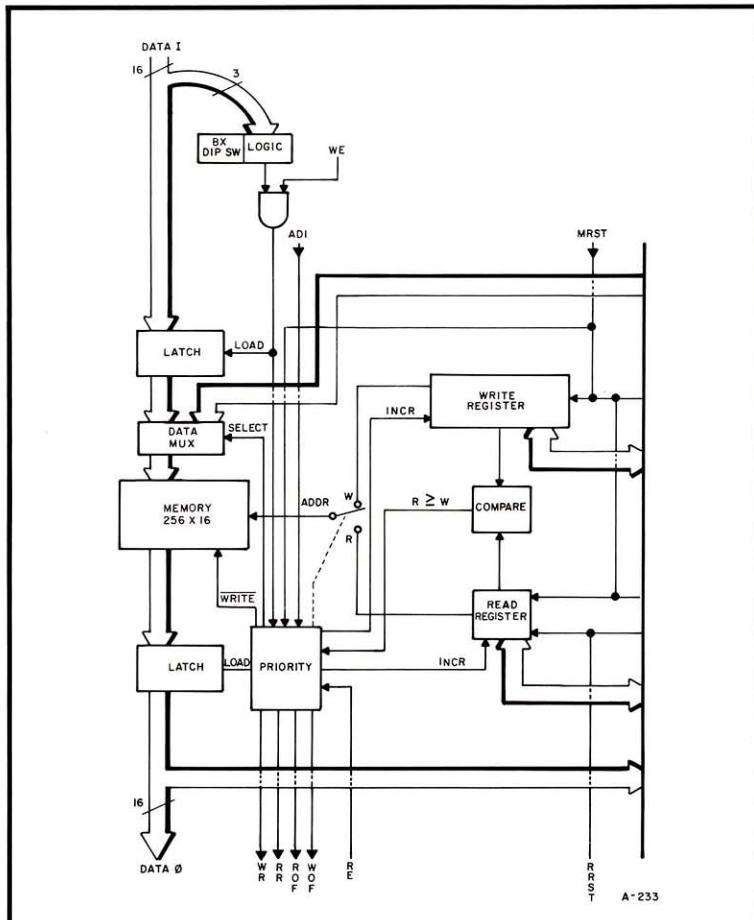
The Write ECLport of the Model 2375 is initialized by a Master Reset (MRST) pulse which resets the internal Read and Write Pointers (RP and WP). The Write ECLport accepts 16-bit datawords at up to a 20 MHz rate. Datawords are latched into the port by an ECL Write Enable (WE) edge and loaded into sequential locations beginning with zero. Fifty nsec later a Write Output Ready (WR) level is asserted. If the write operation is performed during a read operation, the write is delayed by up to 35 nsec. Both operations are correctly performed, however. The upper 3 bits of the dataword may be used by the write Steering Logic to accept or reject the write strobe. A side-panel switch allows each of the eight possibilities to be separately enabled. This allows the stack to be loaded with one type of data (e.g. x) while ignoring another type (e.g. y).

The Model 2375 offers sequential readout. Read operations are initiated by read enable RE. Within 35 nsec, the appropriate dataword is returned along with a Read Ready signal called RR. The Read ECLport may be used without regard to the operation of the Write ECLport. If the read operation is performed during a write operation, the read is delayed by up to 50 nsec. Both operations are correctly performed, however.

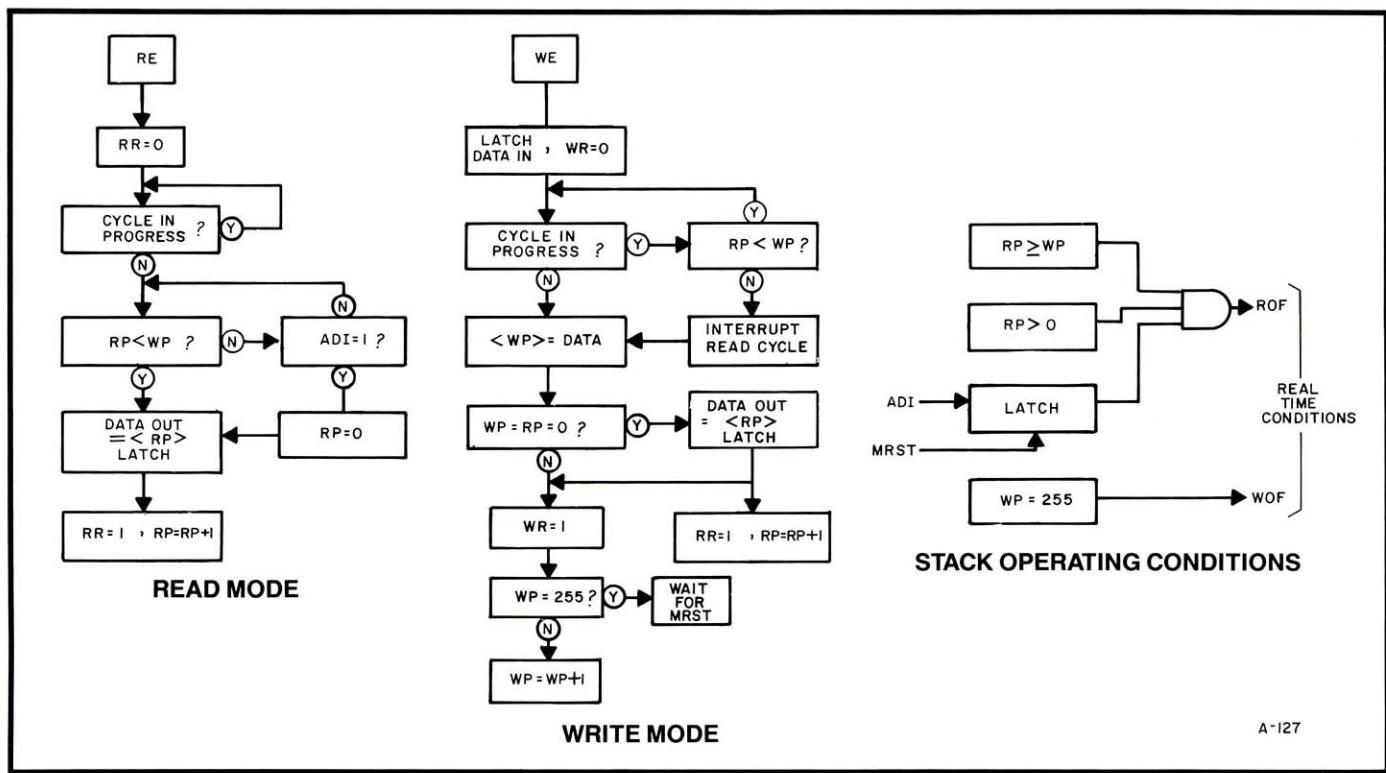
Read operations may commence before the write operations have been completed. The All Data In (ADI) signal at the Write ECLport is used to signal that the Write operation is complete.

Application of RE pulse returns the dataword and an RR edge and advances the internal Read Pointer. If the Write Pointer is less than the Read Pointer, the Data Stack suspends the dataword response, pending either another write operation or an ADI (all data in) edge. If another dataword is loaded into the Model 2375, it is output in response to the read command alone with an RR edge. If an ADI level is received, Read Overflow (ROF) edge is output. The ROF also resets the Read Pointer so that a subsequent read operation causes the stack to "wrap around" and return the dataword in the bottom of the memory. Stack modules can be wired to act as a series of Nested Do Loops. See Application Note AN-24A.

The Model 2375 is packaged in a single-width CAMAC module. It employs the popular ECLline standard for signals. It provides versatility and sophistication to trigger logic.



STACK BLOCK DIAGRAM



STACK FLOW CHART

SPECIFICATIONS

ECLline Model 2375

DATA STACK MODULE

GLOSSARY OF TERMS

ADI: All Data In—Input
MRST: Master Reset—Input
ROF: Read Overflow—Output
RP: Read Pointer—Internal
RE: Read Enable—Input
RR: Read Ready—Output
RRST: Read Reset—Input
WOF: Stack Full (write overflow)—Output
WE: Write Enable—Input
WP: Write Pointer—Internal
WR: Write Ready—Output

WRITE ECLport

Write Reset (MRST):

A front-panel differential ECL input via a two-pin connector. Used to set the Write Address Pointer and Read Address Pointer to zero. Minimum width 10 nsec. Reset time 30 nsec.

Write Enable (WE):

A front-panel differential ECL input via two bridged 2-pin connectors. Used to actuate a write operation. The action of the WE leading edge is to write the Dataword presented at the W ECLport and advance the Write Address Pointer by 1. Write operation requires 50 nsec.

W Dataword (DATA I):

A front-panel differential ECL input for a 16-bit dataword. Supplied via an ECLline standard 17-pair header. The Data I must be settled before application of the WE strobe. Minimum duration: 10 nsec.

All Data In (ADI):

A front-panel differential ECL input via two bridged 2-pin connectors. When unused, it is set to the logical 1 condition. An ADI = 0 suspends responses to a Read request if the read address exceeds the Write Address Pointer. A response occurs either when ADI = 1 or after another write operation is performed. If ADI = 1 and the read address exceeds the Write Address Pointer, an ROF pulse is returned and the Read Address pointer is set to zero. Cleared by MRST.

Write Ready (WR):

A front-panel differential ECL output via two bridged 2-pin connectors to indicate the completion of a write operation.

Write Overflow (WOF):

A front-panel differential ECL output level via a 2-pin connector indicates that 256 writes have been performed.

READ ECLport

Read Reset (RRST):

A front-panel differential ECL input via a 2-pin connector used to set the Read Address Pointer to zero. Minimum width: 10 nsec. Reset time 30 nsec.

Read Enable (RE):

A front-panel differential ECL input via two bridged 2-pin connectors. Used to initiate a Stack Read operation and to advance the Read Address Pointer by 1. The leading edge of the RE provides the dataword addressed by the Read Address Pointer at the Read ECLport's Data O Connector. An RR edge is provided 5 nsec after the Data O word is settled. Read operation requires 35 nsec.

R Dataword (Data O):

A front-panel differential ECL output of a 16-bit dataword. Supplied via an ECLline standard 17-pair header.

Read Overflow (ROF):

A front-panel differential ECL output via 2-pin connector. Indicates that the read address exceeds the maximum address written into since the last MRST operation.

Read Ready (RR):

A front-panel differential ECL output via two bridged 2-pin connectors. Indicates that the read operation is complete and that data is valid at the Data O connector.

CAMAC COMMANDS

F(0)•A(0):	Read 16-bit dataword from memory as addressed by Read Pointer (RP). Increment RP.
F(0)•A(1):	Read 8-bit RP
F(0)•A(4):	Read 8-bit Write Pointer (WP)
F(9)•A(0):	Master Reset (MRST)
F(16)•A(0):	Write 16-bit dataword to memory location addressed by WP. Increment WP.
F(16)•A(1):	Write 8-bit RP
F(16)•A(4):	Write 8-bit WP
Q:	A Q = 1 response is generated for F(0)•A(0) and F(16)•A(0). A Q = 0 response is generated for F(0)•A(0) when the RP ≥ WP and RP > 0. A Q = 0 response is generated for F(16)•A(0) when WP = 255.
X:	An X = 1 response is generated for any valid N•F•A.

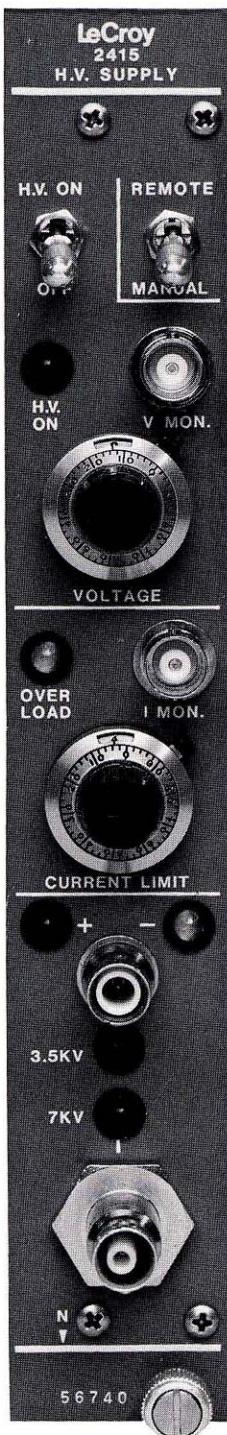
GENERAL

Packaging:	In conformance with CAMAC standard for nuclear modules (ESONE Committee Report EUR4100 or IEEE Report 583.) RF-shielded CAMAC #1 module.
Power Requirements:	± 6 V, <25 W

SPECIFICATIONS SUBJECT TO CHANGE

TECHNICAL DATA

LeCroy



CAMAC Model 2415

Programmable High Voltage Supply

- ± 3.5 or ± 7 kV scales
- 14-bit CAMAC voltage programming
- ADC voltage/current monitor
- 8-bit current limit CAMAC programming

The LeCroy Model 2415 is a versatile, general purpose high voltage power supply packaged in a #2 CAMAC module. The output voltage and the maximum output current can be set via front panel multi-turn potentiometers or via CAMAC programming. The front panel voltage and current settings serve as hardware limits for the CAMAC demand values. This eliminates the possibility of detector damage due to inadvertent software errors or computer failures. The unit offers front panel BNC voltage and current monitor outputs. A built-in ADC allows both to be read via CAMAC.

The Model 2415 offers circuit-board mounted jumpers which allow the unit to be operated in several modes. One set of jumpers selects the output polarity. The other set selects the output range: 3.5 kV or 7 kV maximum. Front panel LEDs indicate the mode selected. The high and low level outputs are provided at separate output connectors.

When used in the ± 3.5 kV ranges, the Model 2415 offers 0.25 V CAMAC voltage programming resolution with a voltage monitor resolution of 1 V. It provides an output current of up to 2.5 mA with current monitor resolution of 0.625 μ A.

When used in the ± 7 kV ranges, the Model 2415 offers 0.5 V CAMAC voltage programming resolution with a voltage monitor resolution of 2 V. It provides an output current of up to 1.0 mA with a current monitor resolution of 250 nA.

Special attention has been given to the current monitor circuitry. In the 7 kV CAMAC mode, the device can register a current of less than 1 μ A. This allows accurate diagnostics of proportional and drift chambers. In this way, a chamber system may be repaired before data are lost or catastrophic damage is done to the chamber.

The Model 2415 has been designed as a versatile, general purpose instrument and finds use in a variety of laboratory applications.

January 1981

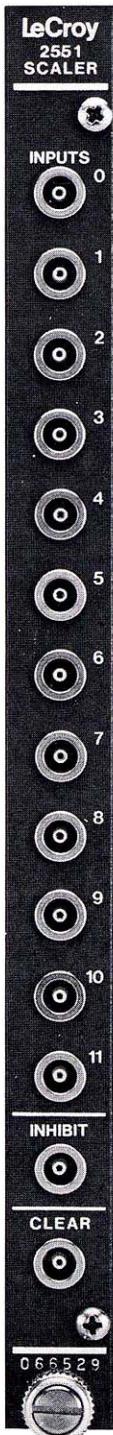
SPECIFICATIONS

CAMAC Model 2415

PROGRAMMABLE HIGH VOLTAGE SUPPLY

	$\pm 3.5 \text{ kV}$ Configuration	$\pm 7 \text{ kV}$ Configuration
Voltage Control		
Range	100-3500 V	200-7000 V
CAMAC Programming	14-bits	14-bits
CAMAC Programming Step	0.25 V	0.5 V
CAMAC Programming Accuracy	$\leq \pm(1.5 \text{ V} + 0.1\%)$	$\leq \pm(3 \text{ V} + 0.1\%)$
Front Panel Adjustment	Ten-turn vernier potentiometer.	
CAMAC Monitor	500 V/turn	1000 V/turn
CAMAC Monitor Resolution	12-bit ADC	12-bit ADC
CAMAC Monitor Offset (Response to 0 V output)	1 V	2 V
CAMAC Monitor Accuracy	0-2 counts	0-2 counts
Front Panel Monitor	$\pm 0.2\%$	$\pm 0.2\%$
Front Panel Monitor Scale	Low Impedance ($< 10 \Omega$) voltage output, suitable for driving a meter; BNC connector. $2 \text{ V/kV} \pm 0.5\%$	$1 \text{ V/kV} \pm 0.5\%$
Front Panel Monitor Offset (value for 0 V output)	$\leq \pm 4 \text{ V}$ referred to HV Output	$\leq \pm 8 \text{ V}$ referred to HV Output
Current Control		
Range	0-2.5 mA	0-1 mA
CAMAC Programming	8-bits	8-bits
CAMAC Programming Step	10 μA	4 μA
CAMAC Programming Accuracy	$\pm(1\% + 12 \mu\text{A})$	$\pm(1\% + 5 \mu\text{A})$
Front Panel Adjustment	Ten-turn vernier potentiometer.	
CAMAC Monitor	250 $\mu\text{A}/\text{turn}$	100 $\mu\text{A}/\text{turn}$
CAMAC Monitor Resolution	12-bit ADC	12-bit ADC
CAMAC Monitor Offset (Response to 0 μA load)	625 nA	250 nA
CAMAC Monitor Accuracy	1 or 2 counts	1 or 2 counts
Front Panel Monitor	$\pm 0.5\%$	$\pm 0.5\%$
Front Panel Monitor Scale	Low Impedance ($< 10 \Omega$) voltage output, suitable for driving a meter; BNC connector. $4 \text{ V/mA} \pm 0.5\%$	$10 \text{ V/mA} \pm 0.5\%$
Front Panel Monitor Offset (value for 0 V output)	$\leq \pm 4 \mu\text{A}$	$\leq \pm 2 \mu\text{A}$
General		
Output Power Rating	7 W	7 W
Output Ripple (at maximum current)	$<50 \text{ mV rms}$	$<50 \text{ mV rms}$
Output Temperature Coefficient	Typically $\pm 50 \text{ ppm/}^\circ\text{C}$, $\pm 100 \text{ ppm/}^\circ\text{C}$ maximum	
Voltage Regulation	$<0.5 \text{ V}$ (0 to 2.5 mA)	$<1 \text{ V}$ (0 to 1 mA)
Short Circuit Protection	Yes	Yes
Output Connector	SHV	Reynolds 1064-1
Controls		
HV On/Off:	Toggle switch. Turns On/Off HV output.	
Manual/Remote:	Selects front panel or CAMAC operation of voltage and current set.	
ADC:	12-bits; conversion time $<30 \mu\text{sec}$.	
Indicator Lamps		
HV On:	Voltage present at output	
Overload:	Supply in current-limiting mode	
Positive:	Positive output configuration	
Negative:	Negative output configuration	
3.5 kV	3.5 kV configuration	
7 kV	7 kV configuration.	
CAMAC Commands:	Z: Clear LAM, demand voltage and current limit registers. (also occurs on CAMAC powerup)	
	Q: A Q=1 signal for F(0) indicates A/D conversion complete and valid data at R1...R12. A Q=1 signal for F(8) indicates LAM is set and an overload condition has occurred since the last F(10).	
	X: An X=1 (command accepted) is generated when a valid N, F command is received. (Some commands which are acknowledged by X have null function. Validity of A is not taken into account).	
	L: A Look-At-Me signal is generated (if enabled by on-board jumper) when LAM is set, indicating that an overload condition has occurred since the last F(10). L is inhibited when module is addressed.	
	F(0): Read ADC data via R1...R12 A Q=1 response indicates ADC conversion is complete.	
	F(8): Test LAM. If the LAM is true, responds with Q = 1.	
	F(10): Clear LAM. (LAM is set by overload condition)	
	F(16)·A(0): Write demand voltage via W1...W14	
	F(16)·A(1): Write current limit via W1...W8	
	F(26)·A(0): Convert output voltage to digital.	
	F(26)·A(1): Convert output current to digital. 350 mA @ +24 V 350 mA @ -24 V 350 mA @ +6 V	
Power Requirements:		

SPECIFICATIONS SUBJECT TO CHANGE.



CAMAC Model 2551 12-Channel 100 MHz Scaler

- **Compact packaging**—12 channels per single-width module means fewer crates, smaller systems, less inhibit fan-out.
- **Low cost**—The high density hybrid circuit design allow common functions to serve a greater number of channels, thus lowering the cost per channel.
- **Fast clear input**—Enables fast rejection of unwanted data without dataway operations.
- **Less than 10 ns double-pulse resolution**—100 MHz counting rates.
- **Direct-coupled inputs**—Input sensitivity or rate capability are not dependent upon risetime.
- **Input inhibit**—Common inhibit disables inputs without injecting counts.
- **Test mode**—Increment mode permits testing all scalers simultaneously without removing cables.
- **Full LAM functions**—Signals impending overflow condition.
- **Full provision to cascade channels**—provides > 24-bit capacity when needed.

The LRS Model 2551 contains 12 identical 24-bit binary scalers especially designed for use in high-speed nuclear counting applications. This dramatic increase in channel density over conventional 4-channel designs is made possible by state-of-the art hybrid circuits which offer reliability-enhancing low power dissipation in addition to compact packaging.

Each scaler is equipped with an extremely wideband input circuit which responds to NIM level logic signals of any duration down to 5 ns, without multiple-pulsing (in the case of wide inputs) and without counting down. The ability to recognize narrow input signals at an equivalent rate of >100 MHz is an important feature, since it assures that the scaler will accurately accumulate any output signal generated by standard discriminator and logic circuits.

Each module is provided with a high-speed fast inhibit which permits simultaneous rejection of input signals at a rate equivalent to 100 MHz. The CAMAC Inhibit (I) provides inhibit control via the rear connector. The inhibit signal must overlap the input signal, but toggling the inhibit will not cause pulses to be counted.

Fast rejection of unwanted data is provided by the fast clear input. This input allows the entire scaler to be reset by application of a NIM level clear pulse without the need to perform any dataway operations.

The Model 2551 provides a full set of LAM functions. When enabled, setting of the 24th bit of any of the 12 channels is flagged by generation of LAM.

The Model 2551 has a built-in test circuit which allows all registers to be checked simultaneously. Application of the CAMAC Increment F(25) Function Code causes each scaler to advance by one count for each S2 timing signal received. The test circuit may be used without disconnecting cables if the Input or CAMAC I Inhibit is on. The 24-bit data from any scaler is read in parallel to the common dataway via the rear card-edge connector. Individual channel non-destructive readout is accomplished by generating a CAMAC Read F(0) and the appropriate address. Using Read and Clear F(2), the channels will be automatically zeroed after reading the last channel. Clear F(9), CAMAC Clear C, or Initialize Z will zero all channels.

The LRS Model 2551 12-Channel 100 MHz Scaler embodies refinements developed over years of experience with wideband direct-coupled discrimination and counting circuits, and, as a result, offers flexibility, reliability, and performance unmatched by any other available equipment.

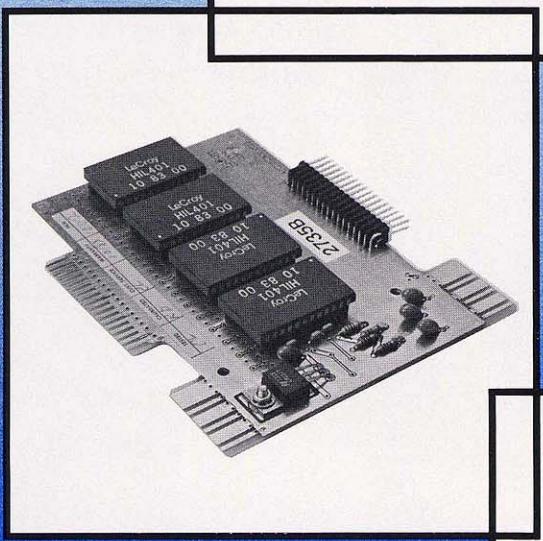
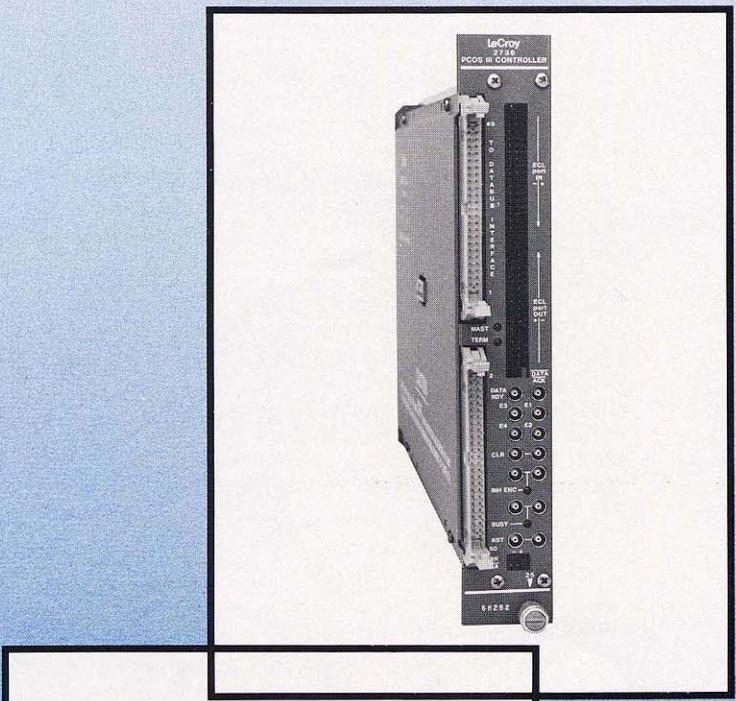
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SPECIFICATIONS

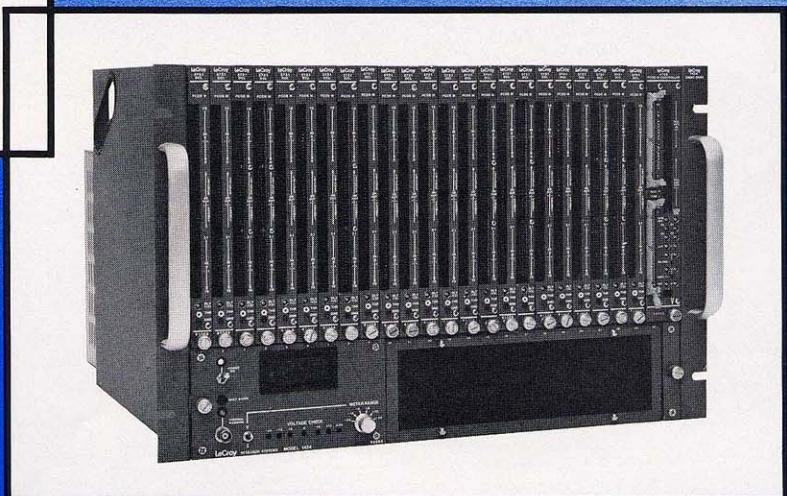
CAMAC Model 2551

12-CHANNEL 100 MHz SCALER

Signal Input (each channel):	Threshold: > -600 mV (NIM logic levels). Impedance: 50Ω , direct-coupled. Reflection: $< 10\%$ typical at 1 ns risetime. Protection: ± 5 volt transients. Minimum Pulse Width: 7 ns FWHM at -600 mV input amplitude; 5 ns FWHM at > -700 mV input amplitude. Multiple-Pulse Resolution: 10 ns. Counting Rate: DC to 100 MHz.
Signal Inhibit:	Common input, -500 mV threshold, 5 ns minimum width, impedance 50Ω . Inhibit signal stretches internally by approx. 5 ns and must precede input signal by 10 ns. Inhibit pulses will not be counter by scaler.
Half Scale Flag:	Any scaler generates LAM when 24th bit is set.
Front-Panel Clear:	Common input, -500 mV threshold, 50 ns minimum width clears all channels with $1 \mu s$.
Capacity:	24 binary bits (16,777,216), (or 48 bits by cascading channels).
Cascading of Channels:	By internal wire jumper option, each even-numbered channel (i.e., 0, 2, 4, 6, 8, 10) may be cascaded with the subsequent odd-numbered channel to provide one 48-bit scaler. In this mode of operation, no LAM will be generated by either of the cascaded channels.
CAMAC Commands:	C or Z: All scalers and LAM are cleared by the CAMAC "Clear" or "Initialize" command; requires S2. Z also disables LAM. I: All Scaler inputs are inhibited during CAMAC "Inhibit" command. Q: A Q=1 response is generated in recognition of an F(0) or F(2) Read function, or an F(8) if LAM set set for a valid N and A, but there will be no response (Q=0) under any other condition. X: An X=1 (Command Accepted) response is generated when a valid F, N, and A command is generated. L: A Look-At-Me signal is generated from time when first 24th bit is set until a module Clear command. LAM is disabled for the duration of N, can be permanently enabled or disabled by the Enable and Disable function command, and can be tested by Test LAM.
CAMAC Function Codes:	F(0): Read registers; requires N and A, A(0) through A(11) are used for channel addresses. F(2): Read registers and Clear module and LAM; requires N and A; (Clears on A(11) only.) F(8): Test Look-At-Me; requires N, and any A from A(0) to A(11) independent of LAM disable; Q response is generated if LAM is set. (F(9): Clear All scaler channels simultaneously; requires N, S2, and A from A(0) to A(11). F(24): Disable Look-At-Me; requires N, S2, and any A from A(0) to A(11). F(25): Increment all scalers; requires N, S2, and any A from A(0) to A(11). (Inhibit should be true to prevent input pulses from being counted). F(26): Enable Look-At-Me; requires N, S2, and any A from A(0) to A(11). Remains enabled until Z or F(24). CAUTION: The state of the LAM mark will be arbitrary after power turn-on.
Packaging:	In conformance with CAMAC standard for nuclear modules (ESONE Committee Report EUR4100e). RF shielded CAMAC #1 module.
Current Requirements:	+6 V at 1.2 A -6 V at 100 mA



August 1984



PCOS III...

Multiwire Proportional Chamber System

LeCroy

Introduction

PCOS III is a complete, multiwire **Proportional Chamber Operating System**. It is a third generation system built upon the experience gained with PCOS I and PCOS II. High performance and simplicity are achieved through the use of new, large-scale custom integrated circuits which have been in design for three years. Four-channel amplifier, discriminator and delay circuits have each been designed to give PCOS III the ultimate simplicity. Its design structure will allow the system to be easily upgraded to the *FASTBUS* standard in the future.

PCOS III employs chamber-mounted amplifier/discriminators and remote delay, latch, and readout. This configuration allows much of the electronics to be located remote from the detector if access is restricted. The delay, latch, and encoding circuitry can also be located near the detector to minimize cable runs and, hence, overall cost.

Special emphasis has been placed on the system's ability to handle high rates. A unique *RIPPLETHRU* circuit offers programmable delay of up to 682.5 nsec and allows input rates > 10 MHz. Use of fast parallel encoding allows the system to process valid events

extremely rapidly. Multiple levels of digital buffering affords the fastest possible CAMAC readout.

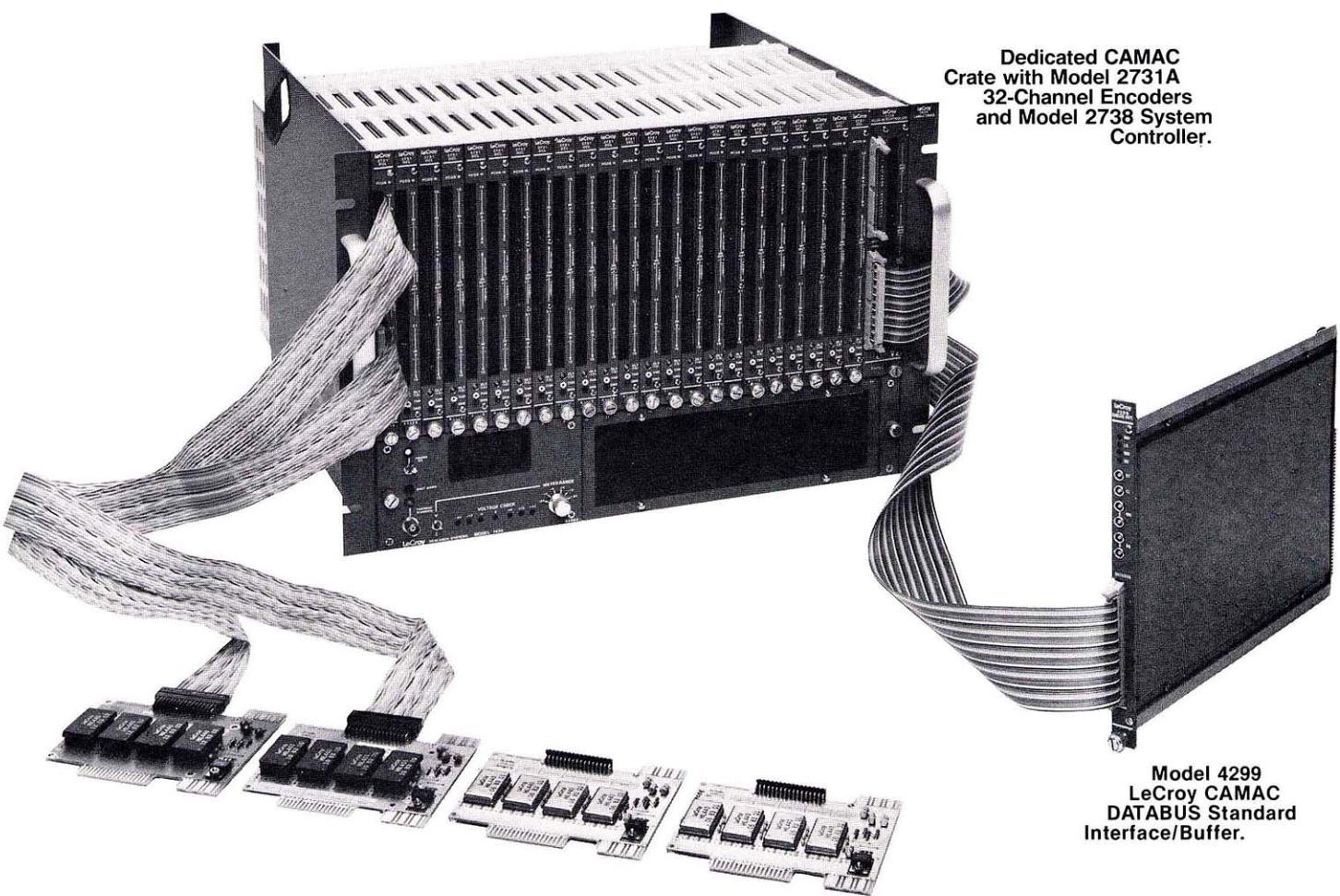
PCOS III allows use of chamber signals in the trigger decision. It offers prompt and latched logic outputs. Both are provided to match the LeCroy ECLline logic system, allowing maximum flexibility and speed. A test input allows any pattern to be gated to the wire inputs after the line receivers.

The versatility of PCOS III is further enhanced by a high-speed ECLport, allowing addresses of clusters to be transmitted to a modern trigger processor for track recognition analysis.

PCOS III offers computer control of discriminator thresholds and of the *RIPPLETHRU* delays. This allows for "plateau" of the chamber cards and "electronic cable cutting" for coincidence timing, both under software control.

Use of exciting new technology and innovative design concepts has made PCOS III an advance for modern experiments and also an economical solution to high-performance MWPC encoding needs.

Dedicated CAMAC Crate with Model 2731A 32-Channel Encoders and Model 2738 System Controller.



Model 2735B
16-Channel Chamber Cards.

General Description

PCOS III contains the circuitry to amplify, discriminate, delay, latch and encode multiwire proportional chamber signals. The elements of PCOS III are shown in Figure 1. The system includes 16-channel chamber-mounted amplifier/discriminator cards (Model 2735B), 32-channel delay, and latch modules (Model 2731A) and a System Controller (Model 2738). Up to 23 of the Model 2731A modules (736 wires) can be operated in a dedicated CAMAC crate with a Model 2738 System Controller.

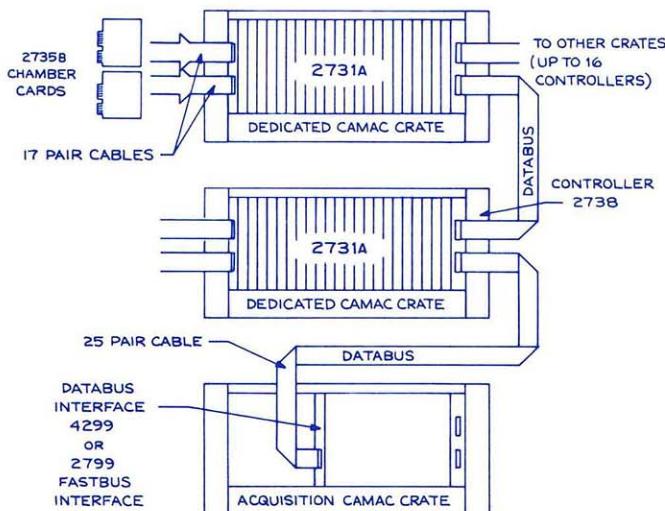
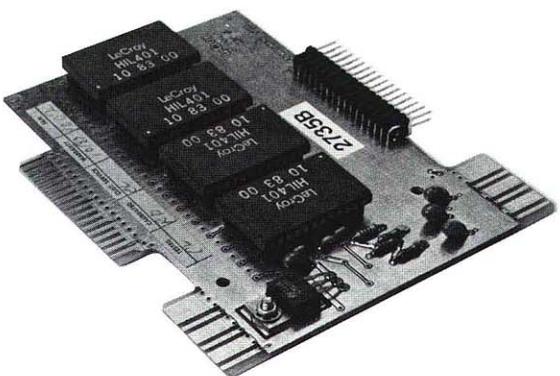


Figure 1

CHAMBER CARDS

The Model 2735B has been designed as an economical yet high-performance chamber card. It is based upon two LeCroy integrated circuits, a four-channel chamber amplifier and a four-channel, time-over-threshold discriminator, together offering four wire chamber discriminator channels with low threshold ($< 2 \mu\text{A}$) and excellent timing properties (typically $< 4 \text{ nsec}$ slewing from 2x to 20x threshold). Outputs are ECLline drivers on a 34-pin header.

The amplifier section of each 2735B channel is a unique differential transresistance amplifier, ideally suited to low threshold wire chamber applications. Its low impedance ($< 100 \Omega$) current-sensitive input monitors the current output of the chamber, not the voltage across an input



Model 2735B
16-Channel Chamber Card

resistor, providing negligible integration of wire pulses. Pulses are faster and thus larger in current amplitude, resulting in improved signal-to-noise ratio. The 2735B card can be used with either positive or negative inputs for cathode or anode signals. Input polarity is jumper-selectable.

The power dissipation of the 2735B is less than 340 mW per channel. This, along with the minimum parts count of the device, means high reliability and cool operation. Thus, the 2735B is ideal for chamber-mounted operation.

RECEIVER MODULES

Chamber pulses are discriminated by the Model 2735B, and transmitted to the Model 2731A receiver module via twisted-pair ribbon cable. The threshold of each pair of 2731A cards may be separately programmed using a DAC within Model 2731A.

Programmable Delay

In order to account for the decision time of the trigger logic, the Model 2731A contains a programmable delay for each channel. The delay of all channels of each 2731A module may be commonly set over the range 300-682.5 nsec in 1.5 nsec. steps. The circuit employed is LeCroy's RIPPLETHRU circuit, a stable computer-controlled delay. Unlike older monostable delays, it does not generate a deadtime equal to the delay. In fact, the RIPPLETHRU can operate at $> 10 \text{ MHz}$ rates. See Figure 2. RIPPLETHRU provides the same high rate capability of cable delay, yet also offers economy and programmability. When the experiment is complete, cable delays are discarded, whereas RIPPLETHRU delays are retained. RIPPLETHRU also allows the system to be configured without having to guess the trigger decision time. The correct value may be programmed at run time.

Two Coincidence Gates are distributed to the 2731A modules via the CAMAC Dataway. Two gate inputs are provided on each Model 2731A to allow for chambers with variable wire spacing. A board-mounted jumper assigns Gate 1 or Gate 2 to the module. The Model 2738 provides NIM-to-ECL conversion and drives the Dataway. The programmability of the delay allows timing variations within the system to be accounted for under computer control.

Readout

The hit-wire data contained within the Model 2731A are stored as a 32-bit word. The Models 2731A and 2738 communicate via 32-bit data transfers 10 times the maximum rate defined by the CAMAC standard. The Model 2731A provides LAM signals to allow only those modules containing hits to be read.

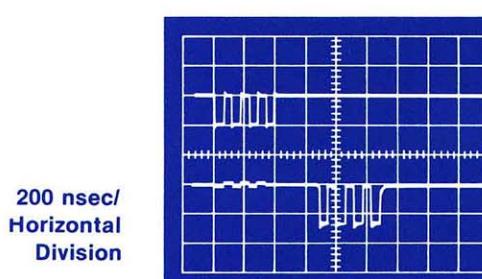
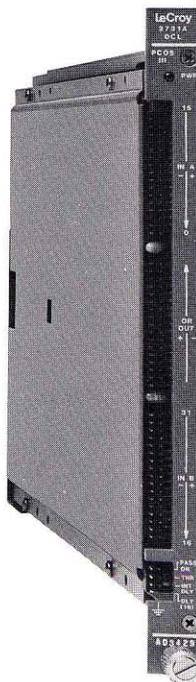


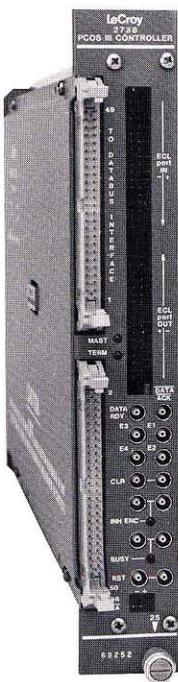
Figure 2
RIPPLETHRU Delay

Test Feature

A 32-bit pattern may be down-loaded into each Model 2731A, causing the selected inputs to be strobed by the test input of the Model 2738. This allows the hardware processors and the 2731A-2738 encoding logic to be completely exercised. The Model 2738 provides NIM-to-ECL conversion and distributes the Test Signals via the Dataway. Coincidence Gates must be provided with the appropriate delay.



Model 2731A
32-Channel Encoder



Model 2738
System Controller

Fast Clear

A reset pulse applied to the Model 2738 is distributed to the 2731A modules via the Dataway. The action of this pulse is to clear the latches within 100 nsec, making the PCOS III system ready to accept another event.

Trigger Aids

The Model 2731A provides signals which allow the wire chambers to be used both in the fast trigger and in the second level trigger. The PCOS III System also has been designed to be used with fast track recognition circuits.

For first-level trigger applications, the Model 2731A provides up to 16 Prompt OR outputs. These are regenerated ORs of two to thirty-two wire discriminator inputs taken before the RIPPLETHRU delay. Internal wire wrap posts allow the user to pairwise wire-OR the inputs. The Model 2731A provides 16 differential ECL outputs via a front panel header. These may be used for both Prompt and Latched ORs. These outputs are compatible with LeCroy's growing ECLline family of logic units.

For second-level trigger applications, the Model 2731A provides up to 8 latched OR outputs. Levels are valid, within 50 nsec of the trailing edge of the coincidence gate. Internal wire wrap posts allow the user to configure four-fold to thirty-two-fold Latched ORs on the OR output header along with the Prompt ORs.

SYSTEM READOUT

The LeCroy DATABUS System is employed for CAMAC readout of the PCOS III System. Up to 16 dedicated crates can be read out via CAMAC using a single Model 4299 DATABUS Interface, located on the data acquisition branch. Dedicated crates of other LeCroy DATABUS Systems may be used along with the PCOS III crates. A FASTBUS interface, Model 2799, is in the early design stages. This will allow simple upgrade to the new standard. See Figure 3.

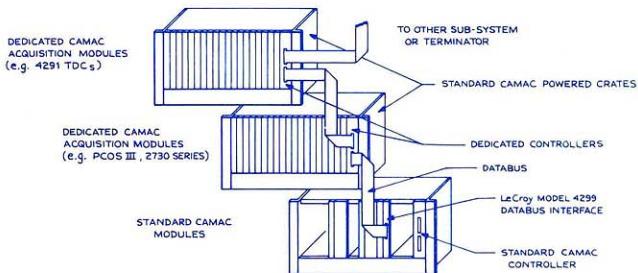


Figure 3

The Model 2738 in each dedicated crate rapidly scans the LAM status of 2731A modules and encodes the address of clusters of hit wires. Only those modules containing hits are read. Data are loaded into a memory for subsequent CAMAC readout. Addresses are also presented at a front panel ECLport, allowing the data to be transmitted to a trigger processor for track analysis.

A block diagram of the Model 2738 controller is shown in Figure 4. It performs the readout and encoding of the hit wires. The unit compacts the data by encoding up to 15 adjacent hits as a cluster. If clusters of more than 15 adjacent hits are encountered, they are treated as multiple clusters. The ECLport Wire In/Out on the Model 2738 allows multiple crates to be cascaded. The ECLport allows the data to be transmitted to a high speed data handler, such as trigger processor or a fast readout system.



The two NIM Coincidence Gates, two Test signals and Clear Signal received by the Model 2738 are restandardized and transmitted to the 2731A modules via the Dataway. The trailing edge of the Gate 1 activates the readout sequence. The 2731A modules containing hit wires request readout via the L lines within the CAMAC crate. The Model 2738 can scan the LAM status of all modules in 100 nsec. Readout of hit 2731A modules is then performed under control of the Model 2738 at a readout rate of 100 nsec per module.

Thirty-two bits are transmitted to the processor at once. The Model 2738 is double-buffered, allowing a second module to be read immediately while data from the first 2731A module are being processed by a fast priority encoder. The addresses of hit wires are generated at the rate of 100 nsec per cycle. Because of the double-buffering, hit addresses are generated at 10 megawords per second. Owing to the bus structure of the ECLport system, 100 nsec is required to skip each crate containing no hits.

Model 4299 DATABUS Interface

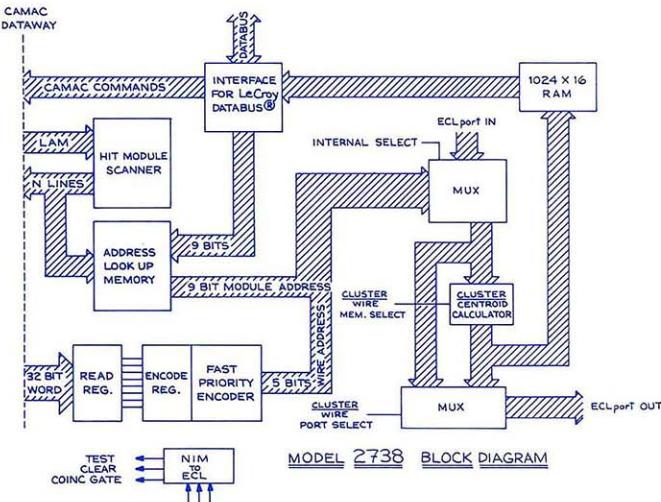


Figure 4

From the trailing edge of Coincidence Gate 1 until the first hit word is transmitted to the ECLport of Crate 1 is 300 nsec. A 100 nsec delay is introduced between the encoding logic and the ECLport output. Each of the successive hits presented requires an additional 100 nsec. An additional 100 nsec is introduced into the datastream for each empty crate after crate 1. If the clusterized data is sent to the ECLport, it is valid 200 nsec after the last hit of the cluster (i.e. the first cluster is presented 600 nsec after the gate. Two words (width and centroid respectively) are presented sequentially, separated by 100 nsec.

The Model 2738 contains a look-up memory to allow the user to assign logical addresses to the modules within the PCOS III crates. This system offers several advantages:

1. The readout format can be tailored to the experiment. For example, the system wire address scheme can be assigned to match the scheme used for a Monte Carlo simulation.
2. Wire addresses of a system using one crate for two or more wire planes can be assigned to eliminate the possibility of confusing the cluster/centroid calculator by events at the boundary.
3. Wire addresses of a chamber which requires more than one crate of PCOS III circuitry can be numbered sequentially over crate boundaries.

The encoded 14-bit addresses of hit wires (logical module address and wire subaddress) are transmitted to a cluster scanner as they are encoded. When activated, the circuit identifies clusters, two or more contiguous hit wires. Two 16-bit words define the cluster. The first contains the 4-bit cluster width and a flag bit to identify it as a cluster word. The second contains the logical address of the cluster centroid. It consists of the 14-bit logical address of the cluster centroid as well as an additional half wire bit set to 1 if the cluster width is even and to 0 if the width is odd.

The Wire In/Out ECLport allows the internal 16-bit digital DATABUS of the Model 2738 to be extended external to the controller. See Figure 5. Multiple crates of PCOS III may therefore be cascaded by connecting their ECLports. A control-daisy chain arbitrates with priorities determined by the position on the bus. Upon receipt of a Coincidence Gate, encoding of all crates begins in parallel. After the LAMs are processed and the first

module read is performed, the highest priority 2738 module takes control of the ECL bus, transferring data to the cluster compacters. After the first crate is entirely read, the second crate follows. Because all the 2738 modules perform their first read in parallel, encoded data from the second crate follow as soon as control of the ECL bus is transferred.

The Cluster/Centroid calculator of the highest priority Model 2738 receives the encoded logical addresses of all hit wires. As a result, the cluster-compacted data can be presented at the ECLport of the 2738 module and loaded into its 1k X 16-bit 2738 memory.

Conventional communication with the PCOS III crates is made via the LeCroy DATABUS. It allows the compacted, formatted data to be automatically transferred from the memory in the Model 2738 to the Model 4299 and then to the attendant computer by CAMAC readout. Data may also be written into the Model 2738. It accepts the logical addresses of the 23 modules it controls and the readout options desired. It also accepts CAMAC commands which are transmitted to the 2731A modules to set threshold and delay settings.

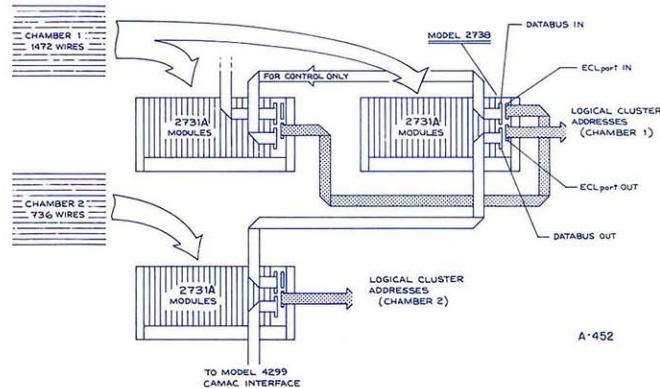


Figure 5

Hit wire or cluster data from a PCOS III crate can be presented at the ECLports of each 2738 module. Data are 16-bit differential ECL with a Data Ready strobe. The addresses are presented as they are calculated, affording highest speed operation of the track recognition logic and eliminating the speed limitations of conventional CAMAC readout.

An unconditional transfer or double handshake scheme can be selected for the ECLport System allowing the readout to be controlled by the 2738 modules. Data and strobe are presented at the ECLports at a rate determined by the internal scan rate of the PCOS III System. For unconditional transfer, cable delay due to extended bussing will cause the output datastream to be displaced in time but will not have any effect on the readout rate. This configuration, along with the operational characteristics afforded by the 2731A modules makes feasible the remote operation of the system.

PCOS III can accommodate wire chambers which have more wires than can be processed by one CAMAC crate of 2731A modules. Multiple crates can be daisy-chained via the ECLports. The master 2738 receives logical hit wire addresses from all crates which are daisy-chained via their ECLports. It processes the data, identifies clusters and presents them at its ECLport.

Test Facilities

PCOS III Offers many built-in test features. Included are facilities for a variety of on-line tests as well as diagnostic facilities. LeCroy also offers a microprocessor-based test system which performs complete tests and diagnoses of each element of PCOS III. The same test system can be used with LeCroy ADCs, TDCs, and drift chamber encoders.

Each 2735B card offers a test input, allowing the user to apply analog signals to the inputs. In this way, a complete system test can be performed on each channel, exercising the front-end card, the cabling, and the Models 2731A, 2738, and 4299. In addition, the PCOS III System accepts a test input at the Model 2738, fanning it out to the 2731A modules. By exercising the test feature of the Model 2731A, the electronics remote from the detector can be independently tested.



LeCroy Model 3500-based Module Test System.

The Model 2731A provides a front-panel Lemo Delay Output, providing channel 15 sampled at the input to the latch, after the *RIPPLETHRU* delays. This provides a method for manually setting the system timing and checking the *RIPPLETHRU*. In addition, each 2731A module offers a front panel test point providing a test level equal to the threshold programming voltage.

For production, test and field service, LeCroy has developed a series of CAMAC test instruments. These are used in conjunction with the LeCroy Model 3500C, Data Acquisition and Control System. Extensive software has also been developed. This LeCroy test system has become a powerful tool, providing automated test and diagnosis of a variety of LeCroy products.

A LeCroy test system has been configured for PCOS III. It allows test of all the features of the MWPC System, including *RIPPLETHRU* calibration and linearity, coincidence resolution of the latch, and operation of the readout. In addition, the Model 171 has been designed to allow quick test of a 2731A module, independent of the system readout hardware. It is an extender module which allows the Model 2731A to operate in a standard CAMAC crate.

The test system is available for sale to customers. It will allow the users to diagnose any problems with the PCOS III System. The test system can be connected to a PCOS III data crate to exercise and test all modules. Such a system can greatly diminish the magnitude of the tasks of system maintenance. The System will also be installed at LeCroy repair facilities near major customers worldwide.

PCOS III Dedicated CAMAC Model 2730

32 Channel Latch

- **Edge Triggered Latch:** For minimum coincidence resolving time
- **Latched OR Outputs:** User configured
- **Programmable Threshold:** For chamber cards
- **Programmable Test Registers:** For hardware processor tests

The LeCroy Model 2730 is a 32 channel LATCH designed for MWPC encoding systems using the LeCroy Proportional Chamber Operating System PCOS III. Each 2730 module accepts 32 differential ECL inputs on two LeCroy ECLline standard 17-pair front panel headers. The Wire-In data are latched by coincidence gates as short as 20 nsec. Latched data are readout using standard LeCroy Model 2738 PCOS III Controllers.

Using the Model 2730, the latched wire chamber data can be incorporated into second level trigger decisions. User-configured OR'ed combinations of the latched data are available at a front panel ECLline output connector.

Thresholds of the wire chamber discriminators can be adjusted under computer control using the Model 2730. The threshold programming voltage is available on the 17th pair of each of the two Wire-In 34-pin headers. This configuration is directly compatible with the LeCroy Models 2735 and 7791 wire chamber amplifier/discriminator cards which feature remote programming of the wire chamber threshold.

System Self-Testing capabilities are a feature of PCOS III. All PCOS III latch modules have 32-bit test registers for enabling selected Wire-In inputs. A Test pulse E3 issued from the Model 2738 PCOS III Controller is used to apply the 32-bit register pattern to the inputs of the Model 2730. Using PCOS III control signals E1, E2, and E3, the logical OR of the test register pattern and the Wire-In data can be performed. Thus, full system diagnostics of the readout electronics and trigger logic are possible.

The Model 2730 is used in a Dedicated CAMAC crate with the PCOS III Model 2738 in slots 24 and 25. Latched wire chamber data from the Model 2730 is readout in excess of 20X CAMAC speed at 100 nsec per 32-bit word. Conforming to the PCOS III protocol, only those latch modules containing data from hit wires are readout. A maximum of 16 dedicated crates of LeCroy DATABUS compatible systems may be connected to a single Model 4299 DATABUS Interface and Memory.

The LeCroy PCOS III has three levels of event buffering. The first level is the latch modules themselves which could be viewed as a 32, 1-bit word, buffer. The second level is the memory of the Model 2738 PCOS III Controller. Priority-encoded data are present in a 1 K, 16-bit word memory in the Model 2738 either as a list of the addresses of hit wires or as cluster-compacted data consisting of the address of the cluster centroid and the cluster width. The third level of event buffering is the 4 K, 16-bit word memory of the Model 4299. These three levels of event buffering allow maximum data acquisition rates throughout the entire Proportional Chamber Operating System.

SPECIFICATIONS

Dedicated CAMAC Model 2730

32 CHANNEL LATCH

INPUTS

Wire-In:	32 differential ECL inputs via two 17-pair front panel headers. Input impedance $112 \pm 2 \Omega$. Input configuration compatible with LeCroy ECLine logic standard. Minimum pulse width 10 nsec.
Coincidence Gate:	Two differential ECL inputs applied from the Model 2738 via the CAMAC DATAWAY. Board-mounted jumper selects E1 or E2. Minimum width 20 nsec.
Test Input:	Two differential ECL inputs applied from the Model 2738 via the CAMAC DATAWAY. Board-mounted jumper select E3 or E4. Minimum width 20 nsec. Applies a test input via a pattern register that may be logically OR'ed with the Wire-In data.
Clear:	Applied via CAMAC DATAWAY. ECL pulse transmitted via the CAMAC DATAWAY. Clears all latches within 20 nsec. Minimum width 20 nsec.

THRESHOLD CONTROL

Threshold Programming:	An 8-bit control word is used to program the threshold level which is available on the 17th pair of the Wire-In input header. Pin 34 is the programmed voltage level and pin 33 is ground. Used with a Model 2735 Chamber Card, the threshold level corresponds the $0.06 \mu\text{A}$ per step. Used with a Model 7791 Chamber Card, the threshold level corresponds to $6 \mu\text{V}$ per step. The threshold level has a range of $\pm 7.68 \text{ V}$ (30 mV per step).
Threshold Monitor:	Two front panel test points, threshold and ground, are provided. Used with the Model 2735 Chamber Card the monitor level is $0.5 \text{ V}/\mu\text{A}$. Used with the Model 7791 Chamber Card the monitor level is $-5 \text{ mV}/\mu\text{V}$.
Threshold Polarity:	An internal jumper selects the threshold polarity. Factory wired for positive polarity to be compatible with the Model 2735.

TRIGGER LOGIC

Latched Outputs:	Open collector drivers, at each of the 32 latch outputs, may be wired OR'ed in any configuration. This wire-wrap configuration is available at the front panel on an ECLine-standard connector. Levels are valid within 20 nsec of the trailing edge of the coincidence gate.
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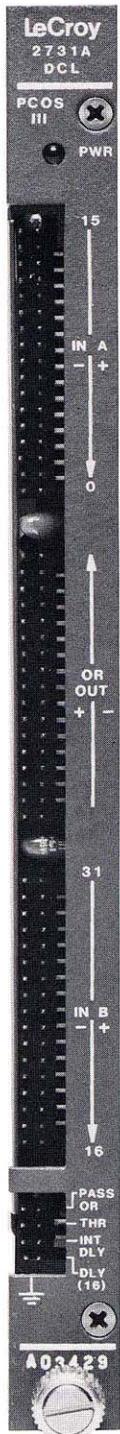
GENERAL

Controls:	Leftmost module must have termination of all control lines. Termination via two 8-pin SIP resistor arrays. All modules shipped with SIP's installed. See side panel for location.
Voltages Used:	$\pm 6 \text{ V}$, $\pm 24 \text{ V}$.
Packaging:	In conformance with CAMAC standard for nuclear modules (ESONE Committee Report EUR4100). RF shielded CAMAC #1 module.
Caution:	Power up this module only when a PCOS III Controller, Model 2738, is in the controller position.

SPECIFICATIONS SUBJECT TO CHANGE

TECHNICAL DATA

LeCroy



PCOS III Dedicated CAMAC Model 2731A 32 Channel Delay and Latch

- **Programmable Ripplethru® Delay:** 300-750 nsec
- **Edge Triggered Latch:** For minimum coincidence resolving time
- **Prompt OR Outputs:** User configured
- **Latched OR outputs:** User configured
- **OR Carry:** For OR's crossing module boundaries
- **Programmable Threshold:** For chamber cards
- **Programmable Test Registers:** For hardware system tests

The LeCroy Model 2731A has been designed as a central element for MWPC encoding. Each 2731A module accepts 32 differential ECL inputs on two ECLline standard 17-pair front-panel headers. Using LeCroy's unique Ripplethru delay, each signal input is delayed by a programmable interval from 300 to 750 nsec. The delayed data are presented to edge-triggered latches which can be activated by coincidence gates as short as 25 nsec.

Computer control of the threshold of chamber discriminators is provided in the Model 2731A via an 8-bit digital-to-analog converter. This threshold programming voltage is provided at both signal input headers. The LeCroy 2735-Series chamber cards use this voltage for setting the chamber threshold.

The Model 2731A allows inclusion of the wire chamber data in the first and second level triggers. On-board prompt and latched signals may be wired OR'd in an arbitrary way. Additionally, two front-panel PASS OR pins may be used to allow the Prompt and Latched OR's to cross module boundaries. In this way, up to 16 signals are generated, which are available at the front panel as differential ECL outputs for trigger purposes. These provisions allow the Model 2731A to be custom-tailored to the experimental trigger.

LeCroy's Ripplethru circuit provides delay with little dead time. It offers 300 nsec to 750 nsec of delay with a double pulse resolution of typically 100 nsec. This unique delay scheme offers excellent stability and interchannel matching ($<\pm 10$ nsec) while providing CAMAC programmability or "electronic cable cutting." The Coincidence Gate, Test Input Signal, and Fast Clear inputs are applied to the 2731A module via the CAMAC Dataway, eliminating the need for costly fanout. The signals are applied to the Model 2738 PCOS III Controller which controls the Dataway. The Coincidence Gate defines the time interval for which the "wire" latches are active. Wire discriminator signals which are received and passed through the Ripplethru delay are latched within the Model 2731A by a Coincidence Gate.

Comprehensive test circuits have been built into the PCOS III System. In addition to test inputs on the chamber card, the 2731A can be separately tested. It has provisions for application of logic pulses to the 32 inputs. A 32-bit mask allows each of the test inputs to be separately enabled and disabled. In this way, the 2731A circuitry and the external track recognition circuitry can both be tested. Also, a front-panel auxiliary test connector facilitates testing of threshold voltage, internal delay and total delay (2731A delay plus external cabling delay).

The Model 2731A is to be used in a dedicated CAMAC crate using the Model 2738 in the controller station. In this configuration, the 2731A modules can be read out at $10 \times$ CAMAC speed, 100 nsec per 32-bit word. Data may then be cluster-compactred by the Model 2738. The concentrated cluster data may then be transferred to a LeCroy standard DATABUS for readout via a Model 4299 DATABUS Interface. Up to 16 system controllers may be connected to a single 4299. In addition, other LeCroy DATABUS systems may be read out along with the 2738 crates.

The Model 2731A is an advanced version of the PCOS III Delay and Latch module and is fully downward compatible with previous PCOS III hardware and software modules.

Preliminary

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SPECIFICATIONS

Dedicated CAMAC Model 2731A

32 CHANNEL DELAY AND LATCH

INPUTS

- IN_A, IN_B: 32 differential ECL inputs via two 17-pair front-panel headers. Input impedance $112 \pm 2 \Omega$. Input configuration compatible with LeCroy ECLine logic standard. Minimum pulse width 10 nsec.
- Coincidence Gate: Two differential ECL inputs applied from the Model 2738 via the CAMAC connector. Board-mounted jumper selects input E1 or input E2. Minimum width 30 nsec.
- Test Input: Two differential ECL inputs applied from the Model 2738 via the CAMAC connector. Board mounted jumper selects input E3 or input E4. Minimum width 60 nsec. Applies a test input via the 32 pattern gates to the Ripplethru inputs. Test level must be logical "zero" for data acquisition. Model 2731A should be inhibited during Test.
- Clear: Applied by the 2738 via CAMAC Dataway. Transmitted as an ECL pulse. Clears all latches within 30 nsec. Minimum width 100 nsec.
- Inhibit: Applied by the 2738 via the CAMAC Dataway. Common inhibit line set via programmable bit in the 2738 disables all 32 ECL inputs. Should be set when applying Test pulse.

RIPPLETHRU DELAY CIRCUIT

- Delay Variations: ± 5 nsec typical, ± 10 nsec maximum channel to channel and module to module.
- Temperature Coefficient: Typically 100 psec/ $^{\circ}$ C.
- Range: 300-750 nsec in two jumper-selectable ranges: 300-682.5 nsec and 330-750 nsec.
- Programming: 8 bits, 1.5 or 1.65 nsec (jumper selectable) nsec steps. Set via the Model 2738. Separate delay register per 2731A module.
- Double Pulse Resolution: 100 nsec typically. 150 nsec maximum.
- Delay 16: One front-panel output. Provides channel 16 logic signal of amplitude ≈ 5 mV after the Ripplethru delay. Used to check approximate Ripplethru delay. Must be terminated in 50Ω for correct output pulse shape. May be unterminated when not in use.
- Internal Delay: 500 kHz front-panel signal with low level width equal to the delay setting. Amplitude approximately 25 mV into 50Ω .

THRESHOLD CONTROL

- Threshold Programming: 8 bits, 0.06μ A steps when used with the 2735 Series. Set via the Model 2738. Separate threshold register per 2731A module. Programming level and ground applied to the chamber cards via a single pair of pins on each of the signal input headers. Pin 33 is ground and Pin 34 is the programmed level.
- Threshold Monitor: A 2-pin header labeled THR on the front panel. Provides a level of $0.5 \text{ V}/\mu\text{A}$ when used with 2735 Series Chamber Card.
- Threshold Polarity Select: Internal wire-wrap option. Factory wired positive.

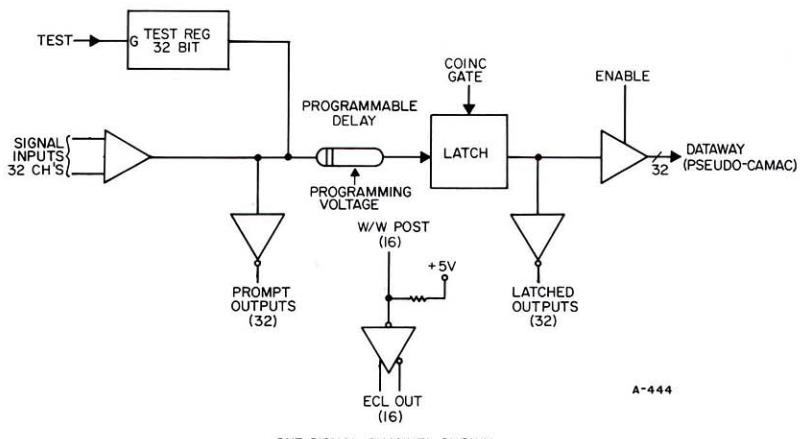
OUTPUTS

- OR Outputs: 16 differential ECL outputs. Internal wire wrap options allow prompt or latched OR signal (1 to 32-fold) to be connected to any of the OR outputs.
- Prompt OR Outputs: 32 open-collector OR signals preceding the Ripplethru delay. Available on wire wrap posts within the Model 2731A. May be arbitrarily wired OR'd to the 16-position internal options connector. Signals are approximately equal to the input width plus 35 nsec. Available within 30 nsec of the input.
- Auxiliary Latched OR Outputs: Thirty-two open-collector OR signals representing the status of each of the 32 latches. Available on wire wrap posts within the Model 2731A. May be arbitrarily wired OR'd to the 16-position internal options connector. Levels are valid within 30 nsec of the trailing edge of the coincidence gate.

GENERAL

- Controls: Leftmost module must have termination of all control lines. Termination via two 8-pin SIP resistor arrays. All modules shipped with SIP's installed. See cut in the side panel for location.
- Power Requirements: <950 mA at + 6 V.
 <900 mA at - 6 V.
 <210 mA at + 24 V.
 < 20 mA at - 24 V.
 If prompt and latched OR's are not required, ECL drivers may be removed, saving 400 mA at - 6 V and 70 mA at + 6 V.
- Packaging: In conformance with CAMAC standard for nuclear modules (ESONE Committee Report EUR4100e). RF shielded CAMAC #1 module.
- Caution: Power up this module when a PCOS III System Controller, Model 2738, is in the controller position.

SPECIFICATIONS SUBJECT TO CHANGE



ONE SIGNAL CHANNEL SHOWN

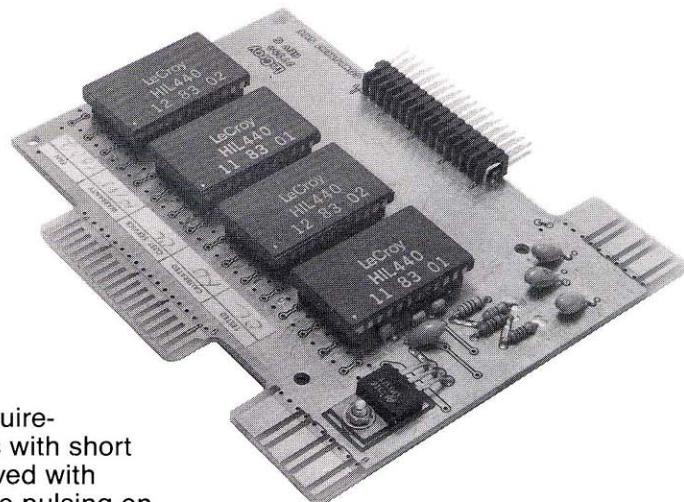
Simplified Block Diagram of 2731A

PCOS III Model 2735A

16 Channel Wire Chamber Discriminator Card

- Compact, low power
- Optimized for drift chambers and timing applications
- Appropriate for chamber mounting on MWPC's with short signal durations
 - $-2 \mu\text{A}$ minimum threshold, remotely settable
- Simple and reliable—custom monolithic and hybrid circuit based
- Negative or positive versions
- Protected against HV discharge

The Model 2735A is an amplifier/discriminator optimized with short time constants for low slewing applications. It is intended for drift chambers with high resolution timing requirements and also useful for multiwire proportional chambers with short signal falltimes. The low threshold of $-2 \mu\text{A}$ can be achieved with chamber-mounted operation without oscillations or multiple pulsing on threshold-level signals provided that signal falltimes are less than approximately 30 nsec. The 2735A is also appropriate for leading-edge-triggered, single hit drift chamber readout without the above shape restrictions on the chamber signals.



The 2735A accepts 16 negative inputs via a PC edge connector. For large quantity requirements, a positive version is also available (Model 2735A/P). The inputs are protected against discharges of up to 3 kV from 250 pF. The threshold of the 16 channels can be commonly adjusted via a control voltage at the power connector or at the output connector. The latter allows the 2735A card to be programmed from the Model 2731A or Model 2730 PCOS III Receiver modules.

The use of multichannel custom integrated circuits and hybrid packaging has resulted in simplicity and hence reliability and economy. The main component of the 2735A card is the Model HIL440 Amplifier/Discriminator hybrid. It contains one each of the custom monolithics Model TRA401 Amplifier and Model MVL407 Comparator. The use of these circuit elements results in high sensitivity and a power dissipation of less than 375 mW per channel. The positive version (2735A/P) is based upon the HIL441 hybrid.

The front end amplifier of the 2735A card was designed for wire chamber inputs. Its low impedance, current-sensitive inputs are uniquely suited to chamber applications, providing no extensive pulse integration as characteristic of FET designs. This offers high rate capability and optimum sensitivity to charge pulses from wire chambers.

The card offers a high impedance test input on the power connector. Application of a triangular waveshape at this point injects a signal into all channels of the 2735A card. This allows the card to be tested in place.

The outputs of the 2735A card are differential ECL, suitable for driving a twisted pair cable. They are presented at a standard 34-pin header. The output duration is equal to the time over threshold with a 7 nsec minimum.

SPECIFICATIONS

Model 2735A

16 CHANNEL WIRE CHAMBER DISCRIMINATOR CARD

Input Pulse = 5 nsec risetime, 20 nsec decay constant, threshold set to $-2 \mu\text{A}$ unless stated otherwise.

Number of Channels:	16
Input Impedance:	$<100 \Omega$
Input Protection:	Protected against discharge of up to 3 kV from 250 pF.
Input Sensitivity:	Negative. Positive version available for quantities of >250 (Model 2735A/P).
Threshold Control Voltage:	$+500 \text{ mV}/\mu\text{A} \pm 20\%$ inputs. Applied via power connector or output connector.
Minimum Threshold:	$-2.0 \mu\text{A}$ (typically $-1.0 \mu\text{A}$ bench test).
Input Coupling:	Must be externally AC coupled, unless driven from a high impedance source.
Interchannel Isolation:	>40 dB for 10 nsec risetime. Better for slower signals.
Opposite Polarity Pulse Rejection:	$>50 \mu\text{A}$
Propagation Delay:	<17 nsec at $2 \times$ threshold <12 nsec at $20 \times$ threshold
Slewing:	<4 nsec typical, <5 nsec maximum ($2 \times$ to $20 \times$ threshold).
Double Pulse Resolution:	<20 nsec at $5 \times$ threshold for 5 nsec wide input pulses.
Output Pulse Width:	Equal to time over threshold, except for effects of hysteresis and shaper time constant 7 nsec minimum.
Minimum Input Pulse Width:	Approximately 5 nsec at $2 \times$ threshold
Test Input:	Via power connector. Minimum dV/dt for $2 \mu\text{A}$ input, approximately 20 mV/nsec; recommended width, 100 nsec.
Input Connector:	36-contact PC card-edge connector (0.254 cm centers), mates with Viking 3VH18/1JND5, LeCroy 455660036 (wire wrap) or Viking 3VH18/1JV5 (solder tail).
Power Connector:	20-contact PC card-edge connector (0.254 cm centers) mates with LeCroy CK20P.
Output Connector:	34-pin header. Mates with LeCroy CK34.
Dimensions:	12.0 cm \times 9.1 cm overall.
Power Requirements:	0.52 A at +5 V (+4.75 to +5.25) maximum 0.68 A at -5 V (-4.75 to -5.5 V) maximum

SPECIFICATIONS SUBJECT TO CHANGE

PCOS III Model 2735B 16 Channel MWPC Discriminator Card

- **Compact:** 16 channel card
- **Low Power:** <375 mW/channel
- **High Sensitivity:** 1 μ A threshold, bench
- **High Stability:** even with input cables
- **Input Protection:** against HV discharge
- **Remote Testing:** via test input
- **High Reliability:** minimum parts count

The Model 2735B is an amplifier/discriminator card optimized for use in multiwire proportional chamber applications. It offers a minimum threshold of 1 μ A on bench testing, and can achieve a practical field operating threshold as low as 2 μ A with stable operation through special attention selection of differentiating and integrating time constants. With a slewing specification of 8 nsec (2 \times to 20 \times threshold), it is ideal for low threshold MWPC work without multiple pulsing even when not directly chamber mounted.

The 2735B card accepts 16 negative-going inputs via a PC edge connector. A card for positive inputs is also available as a special option for large quantity requirements (Model 2735B/P). The 2735B is protected against discharge of up to 3 kV from 250 pF.

Use of multichannel custom integrated circuits and hybrid packaging has resulted in simplicity and hence reliability and economy. The monolithic Models TRA401 and MVL407 are 4 channel amplifiers and discriminators respectively. These are employed in the HIL401 four channel wire chamber amplifier/discriminator hybrids which are the basic visible element of the cards. The use of these special components results in high sensitivity and a power dissipation of <375 mW per channel.

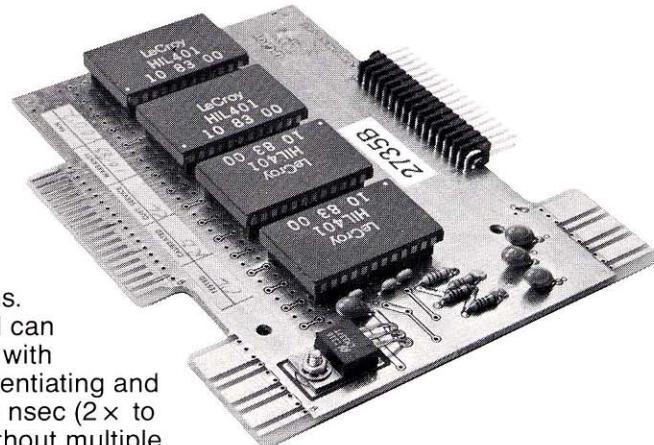
The front end amplifier of the 2735B card was designed for wire chamber inputs. Its low impedance current-sensitive inputs are uniquely suited to chamber applications, providing no extensive pulse integration as characteristic of FET high impedance designs. This offers high rate capability and optimum sensitivity to charge pulses from wire chambers.

The card offers a high impedance test input on the power connector. Application of a triangular waveshape at this point injects a signal into all channels of the 2735B card. This allows the card to be tested in place.

The threshold of the 2735B card is voltage programmable. The DC programming voltage may be applied either at the power connector or at the output connector. The latter allows the 2725B card to be programmed from the Model 2731A PCOS III Delay/Coincidence Register or 2730 PCOS III Latch modules.

The outputs of the 2735B card are differential ECL, suitable for driving a twisted pair cable. They are presented at an ECLline standard 34-pin header. The output duration is equal to the time over threshold with a 12 nsec minimum.

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SPECIFICATIONS

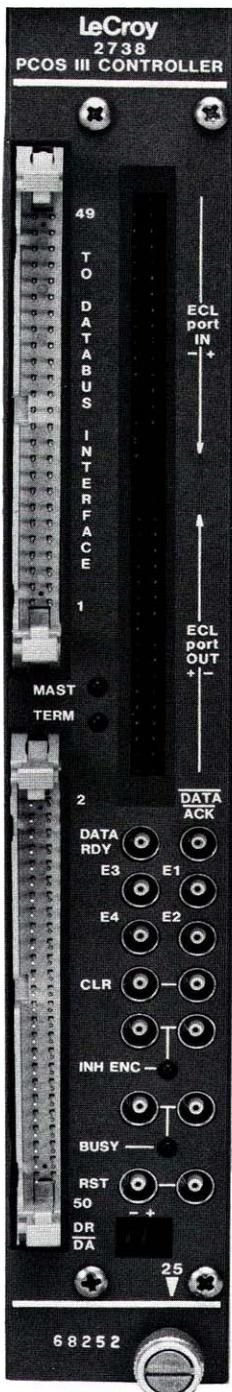
Model 2735B

16 CHANNEL MWPC DISCRIMINATOR CARD

NOTE: Unless otherwise stated, all specifications at Input pulse = 5 nsec risetime, 100 nsec decay constant, threshold set to $-2 \mu\text{A}$.

Channels:	16.
Input Impedance:	$<100 \Omega$
Input Protection:	Protected against discharge of up to 3 kV from 250 pF.
Input Sensitivity:	Negative. (Positive version available for quantities of 250 or more, Model 2735B/P).
Threshold Control Voltage:	$+500 \text{ mV}/\mu\text{A} \pm 20\%$. Applied via power connector or output connector.
Minimum Threshold:	$-2.0 \mu\text{A}$ maximum (typically $-1.0 \mu\text{A}$ bench test).
Input Coupling:	Must be externally AC coupled, unless driven from a high impedance source.
Interchannel Isolation:	$>40 \text{ dB}$.
Opposite Polarity Pulse Rejection:	$>50 \mu\text{A}$. Improved for faster pulses.
Propagation Delay:	$<20 \text{ nsec}$ at $2 \times$ threshold. $<12 \text{ nsec}$ at $20 \times$ threshold.
Slewing:	$<8 \text{ nsec}$ ($2 \times$ to $20 \times$ threshold).
Double Pulse Resolution:	$<35 \text{ nsec}$ at $5 \times$ threshold for 8 nsec wide input pulses.
Output Pulse Width:	Equal to time over threshold except for effects of hysteresis and shaper time constant. 12 nsec minimum.
Minimum Input Pulse Width:	Approximately 8 nsec at $2 \times$ threshold.
Test Input:	Via power connector. Minimum dV/dt for $2 \mu\text{A}$ input, approximately 20 mV/nsec; recommended width, 100 nsec.
Input Connector:	36-contact PC card-edge connector (0.254 cm centers), mates with Viking 3VH18/1JND5, LeCroy 455-660-036 (wire wrap) or Viking 3VH18/1JV5 (solder tail).
Power Connector:	20-contact PC card-edge connector (0.254 cm centers) mates with LeCroy CK20P.
Output Connector:	34-pin header. Mates with LeCroy CK34.
Dimensions:	12.0 cm \times 9.1 cm overall.
Power Requirements:	0.52 A at +5 V (+4.75 to +5.25) max. 0.68 A at -5 V (-4.75 to -5.5 V) max.

SPECIFICATIONS SUBJECT TO CHANGE



PCOS III Dedicated CAMAC Model 2738 MWPC Digital Readout Controller

The LeCroy Model 2738 is the system controller for MWPC encoding with the PCOS III System. One Model 2738 double width CAMAC module occupies station numbers 24 and 25 of a dedicated crate of LeCroy Model 2731 32-Channel Delay and Latch modules for a maximum of 736 wires per crate. The Model 2738 System Controller performs the readout, encoding, and control functions for the 2731 modules and serves as a interface to the LeCroy DATABUS. Communication is achieved via either a LeCroy Model 4299 DATABUS Interface and Memory Module which is resident in the CAMAC data acquisition system or a user-supplied fast ECL interface using the Model 2738 ECLport out connector.

The Model 2738 offers both ECLport readout encoding and data compacting at 10 megawords per second, ten times the maximum CAMAC data transfer rate. The Model 2738 determines the addresses of all wires which were hit and then stores these addresses in a 1k by 16 buffer memory which is interfaced to the LeCroy DATABUS for lower rate transmission of the hit wire addresses via the Model 4299. Internal switches in the Model 2738 allow the implementation of a hardwired cluster centroid calculator. In this mode of operation, the address of the cluster centroid (14 bits) and the width of the cluster (4 bits) are transmitted as successive data words. The internal switches determine whether clustered or unclusterized data is available at both the DATABUS port and the ECLport.

The ECLports of the Model 2738 PCOS III System Controller can be used for both cluster calculations that transcend dedicated crate boundaries and track recognition logic. Master/Terminal switches set the status of each 2738 module in a multirate system. Cluster calculations transcending a crate boundary can then be achieved by connections between the ECLport OUT and ECLport IN of the crates in question. If all of the crates in a PCOS III System were connected together via the ECLports, the master crate (the crate closest to the Model 4299) becomes a master controller. Even with this arrangement it is still possible to communicate to the track recognition logic via the ECLport OUT of the master crate.

The Model 2738 accepts NIM control signals and distributes them to the 2731 modules via the CAMAC Dataway. The system accepts four control lines: E1, E2, E3, E4 and a bridged high-impedance Clear Input. The receiver modules may be assigned to the control lines via internal jumpers.

The value of the chamber discriminator card thresholds (LeCroy Models 2735 or 7791), the value of the delay settings for the LeCroy Model 2731 Delay and Latch, the module addresses for the Model 2731s, and the test patterns are transmitted as datawords from the data acquisition system via the LeCroy Model 4299 DATABUS Control Module to the PCOS III System Controller. This protocol allows the user to determine chamber plateaus, to optimize the required delay ("electronic cable cutting"), to assign any 9-bit address to any 2731 module for complete system control, and to OR a test pattern with the model 2731 wire inputs for system tests.

SPECIFICATIONS

Dedicated CAMAC Model 2738

PCOS III CONTROLLER

CONTROL INPUTS AND OUTPUTS

- E1, E2, E3, E4: NIM level inputs (≤ -600 mV). Input impedance $50\ \Omega$; selection of E1, E2, E3, E4 via jumper option in receiver modules; trailing edge of E1 initiates encoding. See receiver module specifications for minimum widths and usage.
- Clear Encode: NIM level input (≤ -600 mV) clears the encoder section of the Model 2738 and 2731 latches within 100 nsec. High impedance front panel bridged Lemo pair suitable for daisy chain operation may be applied at any time. Minimum width 100 nsec.
- INH Encode: NIM level input (≤ -600 mV) prevents encoding; may not be asserted after encoding has begun. High impedance front panel bridged Lemo pair suitable for daisy chain operation.
- Busy Encode: NIM level output (≥ 16 mA) indicates encoding in process. Lemo connector bridged suitable for daisy chain to indicate total system status. Busy is asserted ≤ 100 nsec after the trailing edge of gate 1 until the encode cycle is complete.
- Reset: NIM input (≤ -600 mV) clears Model 2731 latches and 2738 memory within 100 nsec. High impedance front panel bridged Lemo pair suitable for daisy chain operation. If applied during DATABUS readout, the Model 4299 must be reset via its RT input.

USER OPTION SWITCHES—SIDE PANEL ACCESSED

- Address: Four, 2-position switches, #1, 2, 3, 4. Defines the address of Model 2738 for communication via DATABUS. Address = 4321. “Open” = “1”.
- LAM Enable: Two position switch, #5. Generates LAM Request in 4299 at end of readout cycle. “Closed” to disable LAM Request.
- DATABUS Control: Two position switch, #6. Automatic readout of the data in the buffer memory to the Model 4299. The 2738 local memory can be at any time read by using the 2738 Reread Command. “Closed” for automatic readout.
- Terminal: Two Position Switch, #7. Turns on the front panel “Terminal” LED. This indicates that this controller is furthest from Master. It serves to terminate Data Encoding. If there is no ECLport daisy chain both Master and Terminal switches must be on. “Closed” turns on Terminal LED.
- Master: Two Position Switch, #8. Turns on the front panel “Master” LED. This indicates that this controller processes all data on the ECLport daisy chain and stores the data for readout. “Closed” turns on Master LED.
- ECLport Source: Two position switch, #9. Selects data before or after Data Pipeline. “Closed” to select data before Data Pipeline.
- Pipeline Mode: Two position switch #10. Enables the clusterizing mode of the Data Pipeline. Internal memory always reads the output of the Data Pipeline. “Closed” for non-clusterizing mode.
- ECLport:**
- Data Ready: NIM level (≥ 16 mA) indicates data at ECLport are valid. Data Ready is asserted 30 nsec after ECLport data are valid.

- Data ACK: NIM level (≤ -600 mV) inhibits data transfer to ECLport. Left open, data appear at ECLport at 10 M words/sec. If Data ACK is driven to the 0 mA state for 20 to 80 nsec, one word is transmitted to ECLport output. If Data ACK is in the 0 mA state for > 80 nsec, > 1 word may be presented at ECLport.
- ECLport In: 17-pair header; accepts 16-bit differential ECL signals from ECLport out of the previous Model 2738 in an ECLport chain.
- ECLport Out: 17-pair header provides 16-bit differential ECL signals in same format as CAMAC data, see below (delimiter word not transmitted). Output configuration defined by the ECLline standard. See LeCroy ECLline application note.

2738 COMMANDS

Commands via the Databus cable are based upon simple binary coding as follows:

Symbol Definitions:

A : 4-bit Controller Number:	A ₁ -A ₄
S : 9-bit Logical Address:	S ₁ -S ₉
N : 5-bit CAMAC Station:	N ₁ -N ₅
V : 8-bit Register Value:	V ₁ -V ₈
R : 3-bit Register	R ₁ -R ₃
X : Don't Care	

Consult the DATABUS Interface manual for details of data transfer.

- Wire Inhibit: Disables all data inputs. used during exercise of test pattern.
I=1 implies wire inhibit. I must be maintained in all subsequent command words.

0	x	A ₄	A ₃	A ₂	A ₁	x	x	x	x	x	0	I	0	0	x
---	---	----------------	----------------	----------------	----------------	---	---	---	---	---	---	---	---	---	---

Assign Logical Address:

Transmit 3 words:

Word 1	0	x	A ₄	A ₃	A ₂	A ₁	x	x	x	x	x	0	I	0	1	x
Word 2	1	x	x	x	x	x	x	S ₈	S ₇	S ₆	S ₅	S ₄	S ₃	S ₂	S ₁	
Word 3	1	x	x	x	x	x	x	N ₅	N ₄	N ₃	N ₂	N ₁	x	x	S ₉	

Module Write:

Eight-bit value, V, sets Threshold, Delay, or pattern. Transmit 3 words:

Word 1	0	x	A ₄	A ₃	A ₂	A ₁	x	x	x	x	x	0	I	1	0	x
Word 2	1	x	x	x	x	x	x	V ₈	V ₇	V ₆	V ₅	V ₄	V ₃	V ₂	V ₁	
Word 3	1	x	x	x	x	x	x	N ₅	N ₄	N ₃	N ₂	N ₁	R ₃	R ₂	R ₁	

Register (R)	Description
0 (000)	Delay 300-682.5 nsec in 1.5 nsec steps.
1 (001)	Threshold 0-15.3 μ A in 0.06 μ A steps
2 (010)	Test patterns wires 0-7
3 (011)	Test patterns wires 8-15
4 (100)	Test patterns wires 16-23
5 (101)	Test patterns wires 24-31

Reread Command:	Causes transfer of present contents of buffer memory to the Model 4299.																
	<table border="1" style="margin-left: auto; margin-right: auto;"> <tr><td>0</td><td>x</td><td>A₄</td><td>A₃</td><td>A₂</td><td>A₁</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>1</td><td>I</td><td>0</td><td>0</td><td>0</td></tr> </table>	0	x	A ₄	A ₃	A ₂	A ₁	x	x	x	x	x	1	I	0	0	0
0	x	A ₄	A ₃	A ₂	A ₁	x	x	x	x	x	1	I	0	0	0		

Master Reset: Used to clear 2738 and enable for data taking. Initialed by F(9)•A(0)+A(1)) applied to Model 4299.

OUTPUT FORMAT

Returns wire address, W, plus logical module address S. Wire address includes "half wire" bit, h, from centroid calculation. H is width of Cluster.

Clusterized Data:	<table border="1" style="margin-left: auto; margin-right: auto;"> <tr><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>H₄</td><td>H₃</td><td>H₂</td><td>H₁</td></tr> </table>	1	0	0	0	0	0	0	0	0	0	0	H ₄	H ₃	H ₂	H ₁	width	
1	0	0	0	0	0	0	0	0	0	0	H ₄	H ₃	H ₂	H ₁				
	<table border="1" style="margin-left: auto; margin-right: auto;"> <tr><td>0</td><td>S₉</td><td>S₈</td><td>S₇</td><td>S₆</td><td>S₅</td><td>S₄</td><td>S₃</td><td>S₂</td><td>S₁</td><td>W₅</td><td>W₄</td><td>W₃</td><td>W₂</td><td>W₁</td><td>h</td></tr> </table>	0	S ₉	S ₈	S ₇	S ₆	S ₅	S ₄	S ₃	S ₂	S ₁	W ₅	W ₄	W ₃	W ₂	W ₁	h	address
0	S ₉	S ₈	S ₇	S ₆	S ₅	S ₄	S ₃	S ₂	S ₁	W ₅	W ₄	W ₃	W ₂	W ₁	h			
	:	width																
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	<table border="1" style="margin-left: auto; margin-right: auto;"> <tr><td>1</td><td>1</td><td>A₄</td><td>A₃</td><td>A₂</td><td>A₁</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr> </table>	1	1	A ₄	A ₃	A ₂	A ₁	0	0	0	0	0	0	0	0	0	0	delimiter word
1	1	A ₄	A ₃	A ₂	A ₁	0	0	0	0	0	0	0	0	0	0			
Non-Clusterized Data:	<table border="1" style="margin-left: auto; margin-right: auto;"> <tr><td>0</td><td>S₉</td><td>S₈</td><td>S₇</td><td>S₆</td><td>S₅</td><td>S₄</td><td>S₃</td><td>S₂</td><td>S₁</td><td>W₅</td><td>W₄</td><td>W₃</td><td>W₂</td><td>W₁</td><td>0</td></tr> </table>	0	S ₉	S ₈	S ₇	S ₆	S ₅	S ₄	S ₃	S ₂	S ₁	W ₅	W ₄	W ₃	W ₂	W ₁	0	address
0	S ₉	S ₈	S ₇	S ₆	S ₅	S ₄	S ₃	S ₂	S ₁	W ₅	W ₄	W ₃	W ₂	W ₁	0			
	:	address																
	:	address																
	<table border="1" style="margin-left: auto; margin-right: auto;"> <tr><td>1</td><td>1</td><td>A₄</td><td>A₃</td><td>A₂</td><td>A₁</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr> </table>	1	1	A ₄	A ₃	A ₂	A ₁	0	0	0	0	0	0	0	0	0	0	delimiter word
1	1	A ₄	A ₃	A ₂	A ₁	0	0	0	0	0	0	0	0	0	0			

GENERAL

Voltages Used:	+ 6 V at 5.3 A. - 6 V at 1.0 A.
Packaging:	In conformance with CAMAC standard for nuclear modules (ESONE Committee Report EUR 4100e) RF shielded CAMAC #2 module.

SPECIFICATIONS SUBJECT TO CHANGE.

TECHNICAL DATA

LeCroy



CAMAC Model 4201

High Precision, Wide Range, Fast Encoding TDC

FEATURES

- **Encoding time:** less than 1 μ sec.
- **Time Range:** up to 655 μ sec,
- **Number of bits read:** up to 16 bits (out of the internal 24 bits), this number can be changed to any smaller number by CAMAC control.
- **High resolution:** 156.2 psec at a minimum, the resolution can be set to larger values by CAMAC control (15 ranges available).
- **One level of data buffer:** to derandomize input rate.
- **Symmetrical to start-stop timing:** provides positive or negative rate.
- **CAMAC settable offset.**
- **Externally applicable time window of interest.**
- **Adjustable threshold discriminator on the start and stop inputs.**
- **CAMAC and LeCroy 3500 compatible.**
- **Permits customer extensions to function with histogramming memory and/or time range expansion.**
- **CAMAC settable time overflow.**

The LeCroy Model 4201 Fast Encoding, Time-to-Digital Converter is intended to cover a large class of time measurement phenomena. Housed in a single-width CAMAC module, it can be read either via CAMAC, or by a faster acquisition system such as the LeCroy 3500.

The Model 4201 has great flexibility, permitting the customer to extend its uses to a variety of special applications requiring an interface with a histogramming memory buffer and/or where time range expansion is required.

The unique features and high quality of this TDC make it an extremely useful tool in a wide range of applications.

APPLICATIONS

- Crystallography
- Mass Spectroscopy
- Time of flight experiments
- Decay phenomena in nuclear, atomic, and molecular measurements
- Response time measurements in bio-medical research
- Chromatography
- Laser ranging

December 1982

SPECIFICATIONS

CAMAC Model 4201

HIGH PRECISION, WIDE RANGE, FAST ENCODING TDC

INPUT CHARACTERISTICS

Start/Stop:

Two paralleled Lemo-type connectors per each function, for cascading start/stop pulses; high input impedance (≥ 50 k Ω), unused inputs must be terminated; independent threshold on start and stop inputs adjustable by front panel potentiometers in the range of -1.5 to $+1.5$ V; threshold precision ± 20 mV, two front panel test points allow a $10\times$ threshold monitor, minimum input pulse width of 1 nsec.

A switch option permits differential drive of the start and/or stop inputs; in which case each of the input connectors receives one pulse of the differential pair as indicated on the front panel; input impedance is $50\ \Omega$ AC each input to ground; $100\ \Omega$ DC between the two inputs; common mode swing is ± 2.5 V; fixed threshold is ± 10 mV; suitable for complementary ECL pulses.

A second switch option selects either the leading or trailing edge of the input pulses as start/stop.

Gate Start, Gate Stop, Clear:

Two parallel Lemo-type connectors for each; high input impedance; accepts positive or negative pulses, in particular, NIM or TTL; threshold is -0.4 V for negative, $+1.4$ V for positive pulses.

Gate Start:

Applies a time window to the start pulse; a switch option permits this input to be used as a veto; minimum pulse width is 10 nsec.

Clear:

A 10 nsec minimum width pulse, applicable at any time, clears the last event only (either the event in process or last processed); clear time is less than 500 nsec.

Operation Modes:

In addition to use as a normal start-stop TDC, a suitable connection to the front panel allows measurement of time intervals when the start and stop pulses are traveling on the same cable, as well as when the time interval is defined by a pulse width, or be the rise or fall time of a signal.

Multiple Start Capacity:

Many modules may be externally interconnected so that they respond in common to a stop pulse, but individually to different start pulses traveling on the same cable, thus providing separate readouts for each start.

Acquisition Rate Speed Up:

Use of several modules suitably interconnected by external cable allows the basic acquisition rate (greater than 1 MHz) to be multiplied by a factor which is proportional to the number of modules.

Data Acquisition:

CAMAC and LeCroy System 3500 compatible.

Range Option:

Position of internal switches permits choice of either only positive or only negative time intervals.

CAMAC COMMANDS AND FUNCTIONS

C:

Clear last event.

Z:

Initialize module.

I:

Inhibit module.

LAM:

A Look-at-Me is generated as soon as the module has valid data to be read.

Q:

A Q response is generated if the requested function can be executed.

F(0)•A(0-3):

Read data, 16 bits.

F(2)•A(0-3):

Read data as S1, reset register and LAM at S2.

F(2)•A(8):

Same as F(2)•A(0-3) plus start test "0" at S2; a following read function will read result of the test.

F(2)•A(9):

Same as above, but for test "1."*

F(2)•A(10):

Same as above, but for test "2."*

F(2)•A(11):

Same as above, but for test "3."*

F(8)•A(0-3):

Test LAM, generate Q response if LAM is ON.

F(10)•A(0-3):

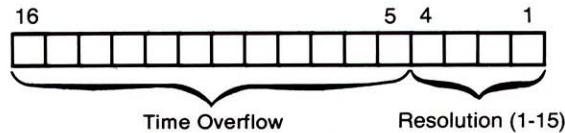
Clear LAM and data register.

F(16)•A(0-3):

Write offset register, 16 bits.

F(18)•A(0-3):

Write command word with the following format:



F(24)•A(0-3):

Disable module. (In this state, the offset value can be read with F(0) or F(2)).

F(26)•A(0-3):

Enable module.

OUTPUT CHARACTERISTICS

BUSY:

Two paralleled Lemo-type connectors provide switchable option for either 32 mA ($2 \times$ NIM) outputs, or 20 mA ($2 \times$ TTL) outputs; the BUSY output changes state as soon as either a start or a stop input arrives, and it stays on until the conversion is done or the second stop or start input completes the event (switchable). Delay between input and busy signals is less than 8 nsec. A BUSY LED is provided on the front panel.

DATA READY:

Two parallel Lemo-type connectors provide switchable option for either 32 mA ($2 \times$ NIM) outputs or 20 mA ($2 \times$ TTL) outputs. The DATA READY output changes state as soon as data is ready to be read. A DATA READY LED monitor is provided on the front panel.

GENERAL

Time Range:

$\pm 655\ \mu\text{sec}$ maximum. Defined by 24-bit coding; and subset may be read out by appropriate CAMAC command to redefine the maximum time range. Circuit symmetry relative to start and stop times permits negative time measurements.

Time Resolution:

156.2 psec minimum. 15 resolution values from 156.2 psec (1 LSB) to 2560 nsec are CAMAC selectable.

Precision:

$\sigma < 0.8$ counts for 156.2 psec resolution.
 10^{-8} long term stability.

Average Conversion Time:

Typically 0.5 μsec for zero time measurement.

Offset Register:

A 16-bit CAMAC loaded offset value may be added to any measured time.

Time Overflow Setting:

Time overflow value, CAMAC controlled over a range of 160 nsec to 655 μsec , in steps of 160 nsec, aborts or stops conversions when overflow occurs. (Switchable)

Buffer Memory:

One level of memory permits a second event to be acquired before the first event has been read out.

LAM Generation:

A DATA READY condition causes generation of a LAM signal.

Packaging:

One single-width CAMAC module without customer board; double width is required for customer board.

Power Consumption:

+6 V at 1.1 A; -6 V at 2.5 A, +24 V at 30 mA, -24 V at 60 mA.

Module Extension:

The module can be equipped with a customer board containing the interface for a customer defined histogramming memory and/or time range expansion.

*These are factory calibration tests, not normally for customer use.

TECHNICAL DATA

LeCroy



CAMAC Model 4204 Multi-Source, Fast Encoding Time Interval Meter

FEATURES

- **Encoding time:** less than 1 μ sec.
- **Time range:** up to 167 msec, 24-bit accuracy (out of the internal 32 bits).
- **High resolution:** minimum 156.2 psec, larger values set by CAMAC.
- **One level of data buffer:** to derandomize input rate.
- **Completely symmetrical to the Start-Stop timing:** gives positive or negative time interval measurement.
- **CAMAC settable offset and time overflow.**
- **Externally set time window of interest.**
- **Multi source:** up to 16 different sources of START (or STOP).
- **Multi-source hit pattern:** read by CAMAC, Reset option for more than one source present.
- **CAMAC and LeCroy Model 3500 compatible.**
- **CAMAC programmable 15-bit time resolved router:** either externally controllable or controlled by multi-source channel number.
- **Simple front panel connection to LeCroy histogramming memory modules.**

The Model 4204 Time Interval Meter (Time-to-Digital Converter, TDC) is a general purpose time measurement instrument designed for research and industrial monitoring applications requiring fast encoding or conversion times, high precision, and long time ranges.

This versatile instrument, an extended version of the Model 4201 TDC, provides many new features including wider range, an externally controlled router for time resolved applications, and optional multi-channel inputs for the source of either the start or stop of the time interval measured.

Readout of the measured time interval may proceed via CAMAC, the LeCroy Model 3500 Multichannel Analyzer System, or the GPIB IEEE-488 Bus (with LeCroy Model 8901 GPIB Interface). The potential 1 MHz data throughput rate may be used even without a fast data acquisition system via LeCroy histogramming memory modules.

APPLICATIONS

- Time of flight experiments
- Material analysis
- Crystallography
- Laser and radar ranging
- Muon spin rotation
- Decay phenomena in nuclear, atomic and molecular systems
- Astronomy
- Nuclear fusion
- Chromatography
- Particle beam monitoring
- Mass spectroscopy

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The Model 4204 Time Interval Meter encodes the measured time interval in less than a microsecond into a 32-bit word. By selecting the required resolution (down to 156.2 psec), a specific subset of 24 bits of the data word may be read. Several overflow options are included and both the designated overflow and an overall data offset can be set via CAMAC.

An externally controlled fast routing system permits the acquisition of data in a time-resolved environment. The acquired data may be accumulated with a preprogrammed offset and then shifted by a fixed amount each time the externally triggered router is pulsed. A total of 256 time slices may be accumulated.

For applications which do not have CAMAC or a CAMAC system fast enough to use the 1 MHz throughput rate of the Model 4204, LeCroy histogramming memory modules may be connected via a front panel auxiliary bus. The histogramming memories may then be read out at lower speeds via CAMAC or through the LeCroy Model 8901, GPIB (IEEE-488) Interface. Data loaded into the histogramming memory units retain all the above features including programmable offset and router.

The Model 4204 may accept up to 16 different sources of STOP (or START) to make one time-interval measurement. The 16 sources are OR'ed together inside the module and an OR output is provided. This OR output may be used to STOP (or START) the TDC. The pattern of the sources providing the STOP (or START) within a given time window is stored in the 4204 and is CAMAC readable. When more than one source is present within the time window, an overflow may be generated to reset the unit. Finally, the channel router, permitting the acquisition of separate spectra for each input.

SPECIFICATIONS CAMAC Model 4204 MULTI-SOURCE, FAST ENCODING TIME INTERVAL METER

INPUT CHARACTERISTICS

Multi-source Input:

16 in a rear panel, 34-pin connector; accepts complementary ECL pulses, 100 Ω input impedance; ECLline compatible; minimum pulse width 10 nsec; receives signals from 16 possible sources of STOPS (or STARTS).

The leading edges of the inputs occurring during the gate time (GATE/INCR) will be registered. The channel number of the first hit is also recorded. This channel will be the one generating the time encoded into the TDC when the OR output is connected to the START or STOP input (see below).

The channel number of the first hit also directs the internal router so the time data may be accumulated in separate histograms for each input source. If the router increment (see description of CAMAC function F(17)) has been set to 0, only one histogram is generated.

Start/Stop:

Two paralleled Lemo type connectors per function, for cascading START/STOP pulses; high input impedance ($>50\text{ k}\Omega$), unused inputs must be terminated; independent threshold on START and STOP input, adjustable by front panel potentiometers, in a range –1.5 V to +1.5 V; threshold precision $\pm 20\text{ mV}$; two front-panel test points allow a $10 \times$ threshold monitor; minimum pulse width 1 nsec.

A side panel switch permits selection of differential drive of the START and/or the STOP inputs. In this case each of the input connectors receives one pulse of the differential pair; input impedance $50\text{ }\Omega$ AC each input to ground, $100\text{ }\Omega$ DC between the two inputs; common mode swing $\pm 2.5\text{ V}$; fixed threshold $\pm 10\text{ mV}$; suitable for complementary ECL pulses.

A second side panel switch selects as START/STOP either the leading or trailing edges of the input pulses.

Gate Start, Gate Stop, Clear, Reset, Gate/Incr:

Two paralleled Lemo type connectors for each; high input impedance; accept positive or negative pulses, in particular NIM or TTL; threshold –0.4 V for negative, +1.4 V for positive pulses.

Gate Start:

Applies a time window to the START pulse; a side-panel switch permits use of this input as a veto; minimum pulse width is 10 nsec.

Gate Stop:

Applies a time window to the STOP pulse; a side-panel switch permits use of this input as a veto; minimum pulse width is 10 nsec.

Clear:

A 10 nsec minimum width pulse, applicable at any time, permits the clearing of only the last event either being processed or already processed; clear time <500 nsec.

Reset:

Sets the router register to zero; in multi-source mode, clears the hit pattern word, and clears only the last event either being processed or already processed; clear time <500 nsec; minimum pulse width 10 nsec.

Gate/Incr:

Increment the router register by a quantity fixed by the router increment register; minimum pulse width 10 nsec.

When multi-source mode is used, acts as the GATE for the rear panel inputs; minimum pulse width 15 nsec.

OUTPUT CHARACTERISTICS

OR:

One Lemo type connector producing NIM levels when terminated in $50\text{ }\Omega$; provides the logical OR of the 16 rear panel multi-source inputs; must be connected to either STOP or START for multi-source operation. The time jitter of the OR output is less than 100 psec.

Busy: Two paralleled Lemo type connectors provide either 32 mA NIM outputs or 20 mA TTL outputs; side panel switch selectable; the busy output changes state as soon as either a START or STOP input pulse arrives, and stays on until the conversion is finished; 8 nsec delay between input and busy signals. A front-panel BUSY LED monitor is provided.

A side-panel switch permits selection of the BUSY interval to run from the START (STOP) to the STOP (START) time only.

Data Ready: Two parallel Lemo type connectors provide either 32 mA NIM outputs or 20 mA TTL outputs; side panel switch selectable; the DATA READY output changes state as soon as data is ready to be read; the DATA READY is generated when both the GATE/INCR signal has ended and the conversion is finished. A front-panel DATA READY LED monitor is provided.

TIME OVF: Two paralleled Lemo type connectors provide either 32 mA NIM outputs or 20 mA TTL outputs; side-panel switch selectable; the overflow output generates a pulse when the time has reached the preset overflow; also set in multi-source mode when more than one input has occurred on rear panel connector (see F(17) description below).

CAMAC COMMANDS AND FUNCTIONS

C: Clears last event (same as CLEAR Input)

Z: Initializes modules

I: Inhibits module (Inhibits START, STOP, and Multi-source ECL Input)

LAM: A Look-At-Me is generated as soon as the module has valid data to be read.

Q: A Q response is generated if the requested function can be executed.

F(0)•A(0-3): Reads time interval data, 24 bits

F(1)•A(0-3): Reads multi-source hit word; the multi-source hit word is never erased and may always be read. It is over-written by the next event.

Data format:

0	S	CH. NUMBER	HIT PATTERN	
R24	R22	R20	R16	R1

Bit 1 to 16: Hit pattern of multi-source input.

Bit 17 to 20: Channel number – 1 of the multi-source input used for the time interval measurement (first channel hit).

Bit 21: Set if a second pulse arrives on the same multi-source input channel that was first hit (double pulse resolution 50 nsec).

F(2)•A(0-3): Reads time interval data (24 bits) at S1, resets register and LAM at S2.

F(2)•A(8): Same as F(2)•A(0-3) plus starts test “0” at S2; a subsequent read function will read the result of the test.*

F(2)•A(9): Same as above, but for test “1”*

F(2)•A(10): Same as above, but for test “2”*

F(2)•A(11): Same as above, but for test “3”*

F(8)•(0-3): Tests LAM, Q response if LAM on.

F(9)•A(0-3): Sets the router register to zero; in multi-source mode, clears the hit pattern word; clears only the last event being processed or already processed; clear time <500 nsec.

F(10)•A(0-3): Clears LAM and data register

F(16)•A(0-3): Writes offset register, 24 bits

F(17)•A(0-3): Selects multi-source mode and writes router command word

Data format:

L	ROUTER INCREMENT	NB OF CYCLES
W24	W9	W1

*NOTE: The tests here defined are mainly for calibration purposes and not for normal customer use.

Bit 1 to 8: Number of router cycles, = 0 for multi-source mode.
 Bit 9 to 23: Number of router increment steps (step size 256 channels).
 Bit 24: Multi-source mode: if = 1, generates overflow condition if number of hits at multi-source input >1.
 Normal Mode: if = 1, external router will not loop.

Writes command word in the following format:

	TIME OVERFLOW	RANGE
W24	W5	W1

Bit 1 to 4: Time Resolution Range (see below).
 Bit 5 to 24: Time Overflow Setting (see below).

F(24)•A(0-3): Disables module (in this state, the offset plus router value can be read with F(0) or F(2)).

F(25)•A(0-3): Increments router counter by one. Must not be used in multi-source mode.

F(26)•A(0-3): Enables module

GENERAL

Time Range: ± 167 msec maximum. Defined by 32-bit coding; any subset may be read out by appropriate CAMAC command to redefine the maximum time range. Circuit symmetry relative to START and STOP times permits negative time measurements.

Time Resolution: 156.2 psec minimum; 15 resolution ranges controlled via CAMAC, LSB ranging from 156.2 psec to 2560 nsec.

Precision: $\delta < 0.8$ counts for 156.2 psec resolution. 10^{-8} long-term stability.

Average Conversion Time: Typically, 0.5 μ sec for zero time measurement

Offset Register: A 24-bit CAMAC loaded offset value may be added to any measured time.

Router Increment Register: CAMAC programmable 15-bit value register whose purpose is described below ("Router Register").

Router Counter: CAMAC presettable 8-bit register counting the number of increment commands to be accepted. Set to zero for multi-source mode.

Router Register: 15-bit dynamic offset value that is added to the 16 MSB of the data; the content of this register is equal to the content of the "Router Increment Register" (CAMAC settable) times the content of the "Router Counter" (CAMAC resettable) for single source mode, or times the number of the first input channel hit for multi-source mode.

Time Overflow Setting: Time overflow value, CAMAC controlled over a range from 160 nsec to 167 msec in steps of 160 nsec; produces a pulse on the front panel overflow connector. May either abort, or substitute the overflow time when overflow occurs (side panel switchable).

Buffer Memory: One level of memory for both time data and the multi-source pattern; permits a second event to be acquired before the first event is read out.

LAM Generation: A Data Ready condition generates a LAM signal if no front panel bus is connected.

Operation Modes: Side panel switches and front panel interconnections permit other modes of operation beside the normal separated start/stop time interval measurement. Pulse width determination and even start/stop pulses traveling on the same cable are possible.

Multiple Start (Stop) Capability: Many modules may be externally interconnected so that they share a common stop (start) pulse, but respond individually to different start (stop) pulses.

Acquisition Rate Speed-Up: Several modules may be interconnected by external cables, permitting the basic acquisition rate (>1 MHz) to be multiplied by a factor proportional to the number of modules.

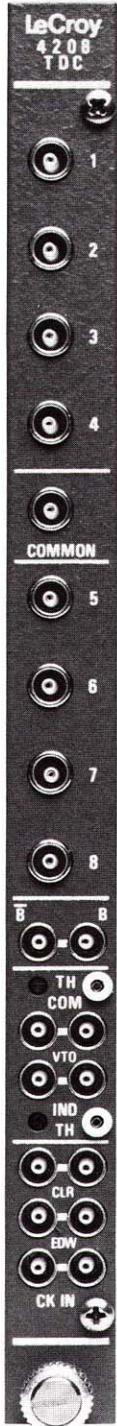
Data Acquisition: CAMAC, LeCroy histogramming memory bus and LeCroy 3500 System compatible.

Range Option: While normally the time range goes from a negative to a positive value, position of side panel switches permit selection of only positive or only negative time intervals.

Packaging: RF-shielded, #2 width CAMAC module.

Power Requirements:

30 mA at + 24 V
3.1 A at + 6 V
2.7 A at - 6 V
60 mA at - 24 V



CAMAC Model 4208

8 Channel Wide Range Real-Time TDC

- 8 channels in a single width CAMAC module
- 24-bit dynamic range
- High resolution: LSB = 1 nsec
- Mixed common START/STOP operations
- Common fast clear input
- Minimum dead time due to the real-time technique

The LeCroy Model 4208 Time-to-Digital Converter (TDC) is designed to cover applications where time measurements must be performed in real time, and require wide dynamic ranges with high resolution.

The Model 4208 has eight independent channels, each of which measures the time from the leading edge of a common input pulse to the leading edge of its individual input pulse.

Due to the particular design, common start input mode as well as common stop input mode can be used. The TDC will encode input pulses preceding the common input as negative times and input pulses arriving after the common input as positive times.

The 4208 TDC may also operate as a single channel multi-hit (8) TDC. In this strap selectable mode, all eight channels are cascaded, each channel hit enables the next one. The unit may also be configured as a dual channel TDC with multi-hit (4), a quad TDC with double hit, or almost any combination of multi-hit.

The 4208 converts the measured time intervals into a 23-bit digital word plus a 24th sign bit which indicates whether or not the common input has preceded the individual input. This corresponds to a dynamic range of ± 8.3 msec (which is expandable with an external clock and appropriate logic circuits).

The module is equipped with a high stability crystal controlled 125 MHz clock. The 1 nsec resolution is realized by digital interpolation between two clock pulses. Dead time after an event has occurred is negligible and data readout can occur immediately after the event.

SPECIFICATIONS

CAMAC Model 4208

8 CHANNEL WIDE RANGE REAL-TIME TDC

INPUTS

8 Individual Inputs:

One Lemo-type connector per channel, impedance $50\ \Omega$; protected to $\pm 3\ A$ for $0.5\ \mu\text{sec}$, clamping at $+ 6$ and $- 6\ V$; each input is followed by a fast discriminator, minimum input pulse width is $4\ \text{nsec}$; threshold is common to the 8 channels and is adjustable by a front panel potentiometer (IND TH) from $- 1.5\ V$ to $+ 1.5\ V$; threshold precision $\pm 20\ \text{mV}$; $10\times$ threshold monitor on the front panel. Multi-hit selectable by internal straps.

Common Input (COMMON):

One Lemo-type connector, high impedance $50\ \Omega$; protected to $\pm 3\ A$ for $0.5\ \mu\text{sec}$, clamping at $+ 6$ and $- 6\ V$; the input is followed by a fast discriminator, minimum input pulse width is $4\ \text{nsec}$; threshold adjustable by a front panel potentiometer (TH) from $- 1.5\ V$ to $+ 1.5\ V$; $10\times$ threshold monitor on the front panel.

Individual Veto Inputs (IND):

Two bridged Lemo-type connectors, high input impedance; accepts NIM levels; the eight individual inputs are inhibited for the duration of the veto; active for the first hit only in multi-hit mode.

Common Veto Inputs (VTO):

Two bridged Lemo-type connectors, high input impedance; accepts NIM levels; the common input is inhibited for the duration of the veto.

End of Time Window (EDW):

Two bridged Lemo-type connectors; high input impedance; accepts NIM level pulses; LAM is generated in response to the leading edge allowing readout of the unit. Internal monostable provided, range adjustable from 0.2 to $8\ \text{msec}$ (set at factory to $8\ \text{msec}$); OR'd with the external EDW input; can be disabled via internal strap.

Fast Clear Input (CLR):

Two bridged Lemo-type connectors; high input impedance; accepts NIM levels; the unit is ready to operate approximately $50\ \text{nsec}$ after the trailing edge of the Fast Clear Input. Clear input width: $> 50\ \text{nsec}$. Does not clear the LAM.

External Clock Input (CK IN):

Two bridged Lemo-type connectors; high impedance NIM input active in external clock mode only. Permits: absolute time accuracy improvement, and time range expansion (clock suppression during "no event dead time"). Note: If the duty cycle of external clock is not $50\% \pm 5\%$, time linearity can be affected.

OUTPUTS

Busy Output (B and \bar{B}):

Two Lemo-type connectors; two NIM levels are started by a nine-input OR of the eight individual inputs and the common input, and are stopped by the clear; allow various input veto logic combinations; complementary outputs are provided.

CAMAC COMMANDS

Z, C:

Initialize module; clears all channels and clears the LAM.

I:

Inhibits all channel inputs during CAMAC inhibit command.

Q:

Conditional response for F(0), F(2), F(8), F(10).

X:

X = 1 response is generated for each valid function.

L:

When enabled (jumper option), LAM is generated by the unit in response to either the "End of Time Window" input or the internal monostable pulse, whichever comes first.

F(0)•A(0) to A(7):

Addressed readout; read data on 24-bit read lines (2's complement convention); Q = 0 if an empty channel is read; Q = 1 otherwise.

F(2)•A(0) to A(7):

Addressed readout as for F(0); F(2)•A(7) clears the unit at S2; does not clear the LAM.

F(8)•A(0):

Test Look-at-Me; Q = 1 if LAM is present.

F(9)•A(0):

Clears unit; resets LAM and all channels.

F(10)•A(0):

Test and clear Look-at-Me; Q = 1 if LAM is present.

GENERAL

Resolution:

$\pm 1\ \text{nsec}$

Dynamic Range:

23 bits + 1 bit for sign.
Expandable via external clock mode.

Integral Non-Linearity:

± 1 count

Encoding Time:

None, the time is encoded in real time.

Multi-hit Dead Time:

Inherent dead time (time reference at front panel Lemo-type connector): $3\ \text{nsec}$ typical.

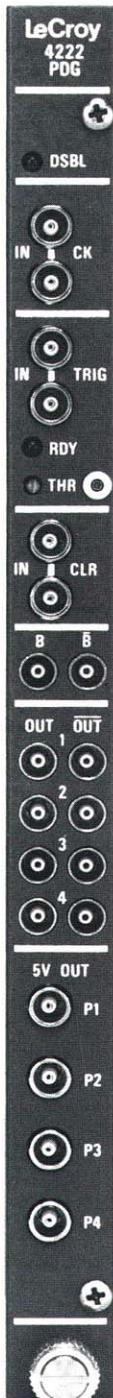
Packaging:

Single width CAMAC standard module.

Power Requirements:

$1.5\ A$ at $6\ V$; $3.3\ A$ at $- 6\ V$; $17\ mA$ at $+ 24\ V$; $17\ mA$ at $- 24\ V$.

SPECIFICATIONS SUBJECT TO CHANGE



CAMAC Model 4222

Quad, Wide Range, Gate and Delay Generator

- 4 channels in a single width CAMAC module.
- 170 nsec - 16.7 msec dynamic range (24-bit).
- High resolution: 1 nsec steps.
- Common Trigger input, edge selection and threshold level adjustment.
- Common Clear input.
- Minimum Deadtime with Real-time Technique.
- CAMAC programmable.

The LeCroy Model 4222, Quad, Wide Range, Gate and Delay Generator, produces long, precise time delays and time intervals synchronously with a random Trigger input. The 4-channel module features wide dynamic range with high resolution and minimum dead-time. All 4 channels of the Model 4222 are started by a common Trigger input. Each channel provides a programmable time delay of up to 16.7 msec in 1 nsec increments.

Three outputs are provided for each channel:

- a level output providing a NIM signal which goes "true" after the programmed time delay and is reset by the Clear;
- a level output providing a NIM signal which goes "false" after the programmed time delay and is reset by the Clear;
- a pulse output providing a 5 V fast risetime signal into 50Ω after the programmed time delay.

Outputs 1 and 2, or outputs 3 and 4, can be internally coupled to generate two independent programmable time windows synchronized to the Trigger input.

The Model 4222 may be set to Retrigger Mode (side switch selectable) permitting the unit to retrigger without being reloaded. In Retrigger Mode, a second side switch permits two options: the unit may be retriggered anytime 100 nsec after the last trigger, or anytime after the longest delay has elapsed.

An external clock may be used to feed several Model 4222 modules with an identical time base.

SPECIFICATIONS

CAMAC Model 4222 QUAD, WIDE RANGE, GATE AND DELAY GENERATOR

INPUT CHARACTERISTICS

Trigger Input (TRIG):	Two bridged front panel Lemo-type connectors; high input impedance; positive/negative edge selection via switch through side cover; threshold level adjustable between -1.5 and +1.5 V with a front panel potentiometer; 10X threshold monitor on front panel; minimum input width: 5 nsec; the unused input must be terminated in 50 Ω.
Clear Input (CLR):	Two bridged front panel Lemo-type connectors; high input impedance accepts NIM level pulses; minimum input width: 50 nsec; the unused input must be terminated in 50 Ω. If a Clear pulse is received when a delay is being generated all outputs are reset to quiescent state and the Trigger input is enabled.
Clock Input (CK):	Two bridged front panel Lemo-type connectors: high input impedance; selected via an internal strap; NIM level inputs; the unused input must be terminated in 50 Ω. Clock input frequency must be 31.25 MHz ± 0.1%. Stability determines the long-term accuracy of the time delays.

OUTPUT CHARACTERISTICS

BUSY and $\overline{\text{BUSY}}$ Outputs (B & \overline{B}):	Two front panel Lemo-type connectors; NIM level outputs. BUSY output state goes true in response to a valid Trigger and remains true until either the end of the shortest delay or the end of the longest delay as selected by an internal switch.
Delayed Level Outputs (OUT & $\overline{\text{OUT}}$):	Two front panel Lemo-type connectors per channel: NIM level outputs; both direct (OUT) and complementary ($\overline{\text{OUT}}$) outputs are provided. A set of side panel switches permits the selection of either independent outputs or coupled window outputs for channels 1 and 2, or 3 and 4, separately: <ul style="list-style-type: none">- Channels 1 and 2 (or 3 and 4) INDEPENDENT: Each channel output (OUT) goes "true" when the corresponding programmed time delay has elapsed; output is reset by the Clear or by the next Trigger if the Retrigger Mode has been selected.- Channels 1 and 2 (or 3 and 4) COUPLED: Channel 1 (3) output (OUT) goes "true" when time delay 1 (3) has elapsed and goes "false" when time delay 2 (4) has elapsed; delay 1 (3) < delay 2 (4). Channel 2 (4) output (OUT) goes "true" when delay 2 (4) has elapsed and is reset by Clear or by the next Trigger if the Retrigger Mode has been selected.
Delayed Pulse Output (P1-P4):	One front panel Lemo-type connector per channel. Each Channel PULSE OUT delivers a 1 nsec risetime 5 V pulse (into 50 Ω) when the corresponding time delay has elapsed; pulse width 100 nsec ± 10%.

CAMAC COMMANDS AND FUNCTIONS

Z:	Initializes module resets all channels, disables trigger input and enables CAMAC access (does not reset data registers).
C:	Resets all channels (does not reset data registers), equivalent to front panel Clear input.
I:	Disables trigger input when present.
X:	X response is generated for each valid function.
Q:	Q response is generated for each valid function unless otherwise specified.
F(0)•A(0-3):	Reads selected programmed delay for channels 1-4 in 24 bits; Q=1 always; 24-bit unsigned integer convention.
F(1)•A(0):	Reads status via Read Lines 1 to 4: R1 = 1 if shortest delay elapsed; R2 = 1 if longest delay elapsed; R3 = 1 if Model 4222 is ready for trigger; R4 = 1 if CAMAC access enabled. All states are strobed by the leading edge of the CAMAC N signal.
F(9)•A(0):	Resets all channels (does not reset data registers) equivalent to external Clear input.
F(16)•A(0-3):	If CAMAC access enabled, writes delay to selected channel 1-4 in 24 bits. Q=1 if CAMAC access enabled; Q=0 otherwise. 24-bit unsigned integer convention.
F(24)•A(0):	Disables unit; enables CAMAC access.
F(25)•A(0):	Triggers the unit (equivalent to external front panel Trigger input): Q=1 if unit was ready for Trigger; Q=0 otherwise.
F(26)•A(0):	Enables unit; disables CAMAC access.

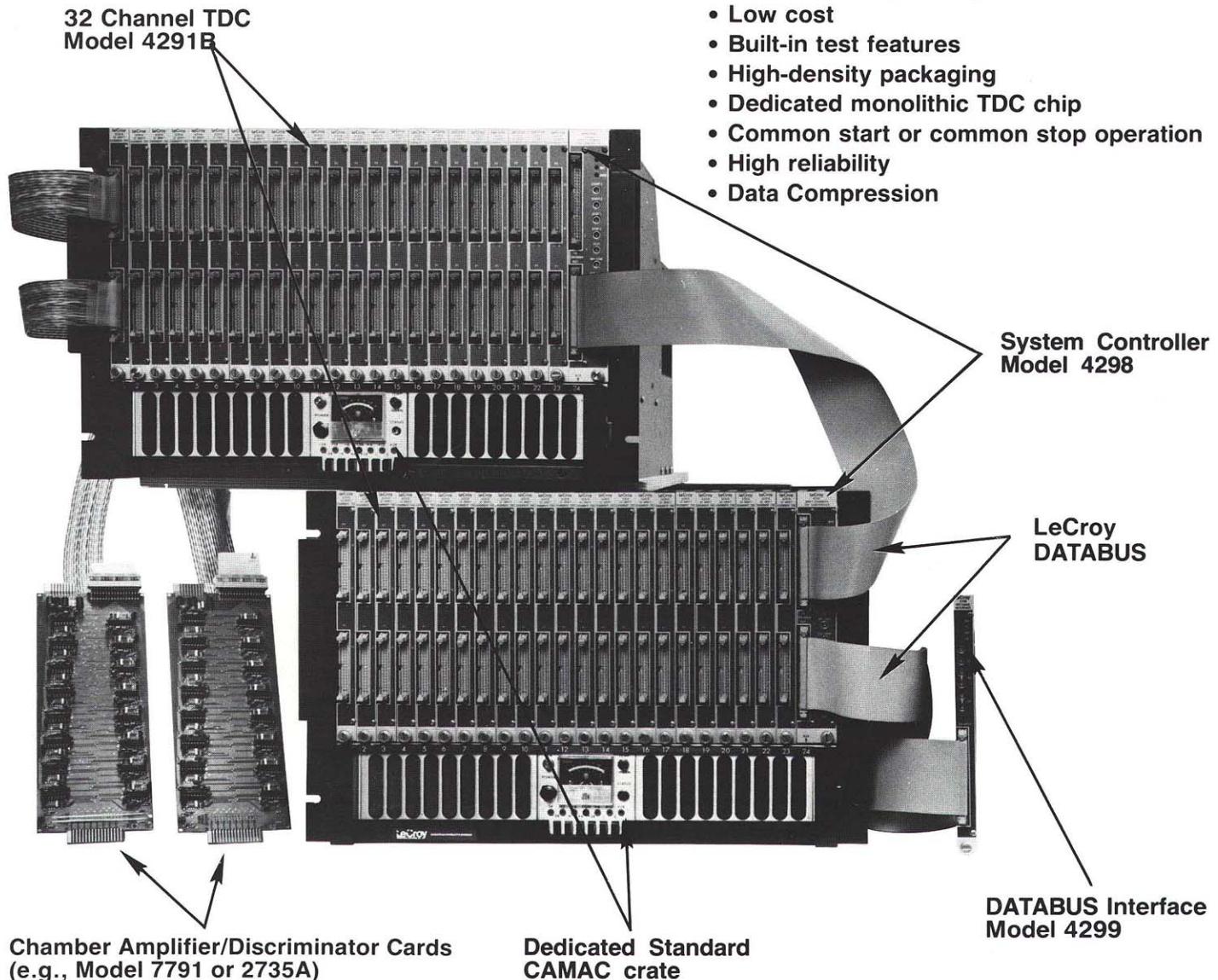
GENERAL

Delay Range:	170 nsec + 0 to 16.777215 msec in 1 nsec increments.
Accuracy:	$\pm 200 \text{ psec} \pm \text{time base error}$.
Jitter:	150 psec RMS maximum; up to 1 msec delay (see manual for additional information).
Insertion Delay:	170 nsec.
Crosstalk:	< 500 psec when delays differ by less than 8 nsec, 0 otherwise.
Internal Time Base:	High stability quartz oscillator: $\Delta f/f_0 : \pm 5 \cdot 10^{-6}$ initial frequency tolerance; $T_c : < 0.5 \text{ ppm}/^\circ\text{C}$; Aging : $< 3 \cdot 10^{-9}/\text{day}$.
Packaging:	Single width standard CAMAC module.
Power Requirements:	40 mA at +24 V 1.3 A at +6 V 2.5 A at -6 V 130 mA at -24 V

SPECIFICATIONS SUBJECT TO CHANGE

System 4290

Drift Chamber Time Digitizing System



GENERAL DESCRIPTION

The 4290 is a complete operating system for multiwire drift chamber data-handling. The System, organized as a sub-system of CAMAC (or FASTBUS in the future), accepts differential ECL signals from chamber preamplifiers-discriminators such as the LeCroy Model MVL100 Monolithic IC's or Model 7791, 2735 or 4292 Cards.

Up to 23 Model 4291 32 Channel Time Digitizer modules (736 wires) can be housed in a dedicated, standard CAMAC crate with a Drift Chamber TDC Controller, Model 4298, occupying the controller position (station 24 and 25) of the crate. The Crate Controller acts as a fast data readout preprocessor, rejecting unwanted zero or full scale values during data-taking. Valid data are dumped via a fast DATABUS into a parallel access, bi-directional $4K \times 16$ -bit memory housed in a DATABUS Interface module, Model 4299. The Interface obeys conventional CAMAC protocol and is therefore to be located in a crate on the data acquisition branch. Its large capacity allows buffering of more than one event on long-spill machines, and it also offers the advantage of concentrating a large amount of valid data in a single CAMAC crate for later microprocessor pre-analysis.

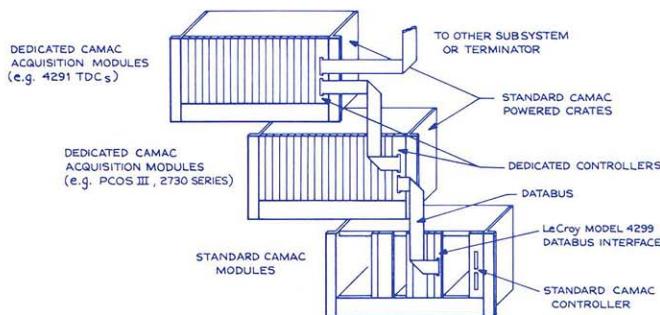
Each digitizer channel has the ability to be automatically trimmed so that all pedestals and slopes are set to identical values, thus eliminating the need to do computer corrections. To provide this and other test features, the 4298 Crate Controller acts as a programmable time mark generator for the test and calibration sequences. Alternating zero and full scale time signals are generated by the Controller, allowing each channel to "learn" the values of both trims. Initialized by an AUTOTRIM command at the 4299 Interface, the System can correct for all pedestal differences up to $\pm 5\%$ of the full scale time (e.g., ± 50 nsec for 1 μ sec full scale) caused by cabling and preamplifiers.

The full scale range can be continuously adjusted in each 4291 module from 500 nsec to 2 μ sec. Options for other ranges can be provided. The conversion time is 35 μ sec for 9-bit accuracy. Transfer time is 12.5 μ sec per "hit" 4291 module plus 0.5 μ sec per valid word (for 5-meter DATABUS).

Data may be recorded employing either a COMMON START or a COMMON STOP scheme. The former is uniquely suited to most synchronous accelerator configurations (PEP, PETRA, etc.) and the latter is suited to long-spill machines (SPS, FNAL, etc.).

A typical system configuration is illustrated on the cover. Its main components are the Model 4291B 32 Channel Time Digitizer, Model 4298 Dedicated Crate Controller, Model 4299 DATABUS Interface/Buffer, and Model 7791 or 2735 card (both Chamber Mounted Systems) or Model 4292 (OFF Chamber System) Chamber Amplifier/Discriminator.

SYSTEM CONFIGURATION



Dedicated CAMAC Model 4291B 32 Channel Drift Chamber Time Digitizer

The LeCroy Model 4291B is a single-width CAMAC module containing 32 time digitizers. Two 34-pin front-panel connectors (P1, P2), each accommodating 16 complementary inputs at ECL levels, allow use of twisted-pair ribbon cables from the discriminator outputs to the TDC's. The input impedance of the digitizers is 110Ω .

Each digitizer consists of one LSI Custom Monolithic Model MTD110. This monolithic circuit has been expressly designed to provide excellent time resolution in applications where a large number of digitizers are required. It is a 9-bit plus overflow time-to-digital converter utilizing an analog time stretcher followed by a digital counter. The outstanding feature of this analog device is its self-calibration mode AUTOTRIM. This feature employs two sets of internal registers, DAC's, and digital comparators used to adjust both the offset and the slope of the analog ramp. In AUTOTRIM mode, a precision pulse source (in the 4298 Controller) generates a series of pulses that alternate between a pedestal count of two and a full scale count of 514 (overflow plus 2). The initial MTD110 registers are then appropriately updated causing perfect calibration to be achieved. The adjustment range corrects for unit-to-unit variations in manufacturing, as well as, slow temperature and/or voltage changes. The range of the offset adjusts is more than adequate for internal variations, and allows for the option of correcting for external cable and preamplifier variations. All of the active circuits are incorporated in a single, low-power, 18-pin DIP package, making it possible to achieve high accuracy and high density at low per-channel cost.

The 4291 offers either a COMMON START or COMMON STOP operating mode, user selected via the Model 4298 Crate Controller.

In the COMMON STOP mode, the Wire input to the differential receiver becomes the Start input. This begins the timing cycle, which is completed by receipt of an EXperiment COMmon trigger (derived from the event trigger) which generates a Stop. Subsequent Wire inputs before the trigger are each processed as another Start, just as if the System were quiescent. After the trigger pulse is received, the inputs are inhibited and the arrival time of the last Wire input pulse before the trigger (but within the full scale time range) is digitized and transferred to the 4298 Controller. The mode is ideal when a quality pretrigger is not available since the entire full scale time can be used as the trigger decision time.

In the COMMON START mode, the EXperiment COMmon trigger generates a Start used to initiate the timing cycle. Then the first Wire input received (during the full scale time) causes a Stop, and the timing cycle is completed. At the end of the full scale time, the conversion and transfer cycle is initiated.

In either mode, if a wire pulse is received during the full scale time, a HIT register will be set to provide a prompt indication of valid data. This HIT data is used internally to reduce readout time (only HIT modules are read out) and is available to the user via a rear panel connector for use in the higher level trigger logic.

TRIGGER DECISION LOGIC MODEL 4291B

In the Model 4291B, the hit registers are buffered and available in parallel on connector P3 located at the top rear end of the unit. The tristate TTL buffers, which are of negative-type logic, can be strobed via the ENABLE input of P3. A positive logic option is available upon request.

INPUT/OUTPUT SPECIFICATIONS

Hit Register Outputs: 32-bit parallel output provides low-power Schottky, low-true tristate output.

Output Enabled, No Hit: > 2.4 V at + 15 mA max.

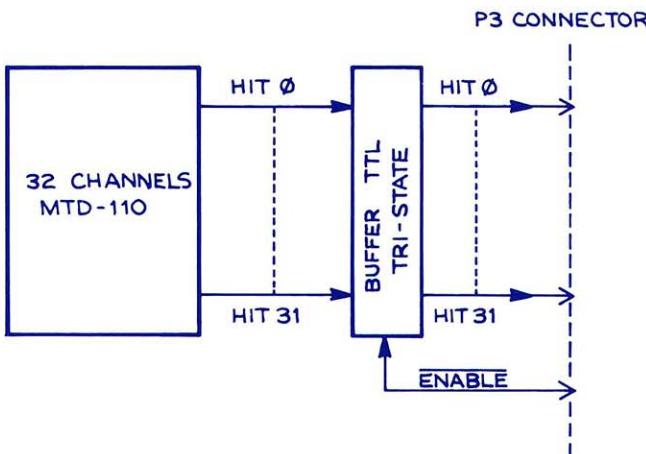
Output Enabled, Hit Present: < 0.5 V at - 24 mA max.

Output Not Enabled: High impedance; $\pm 20 \mu\text{A}$.

Enable Input: High level disables (> 2 V, 0.1 mA max.). Low level enables (< 0.8 V, 0.4 mA max.). Enable time < 40 nsec. Data are available after the full scale time until reset.

P3 Connector: Rear panel 32-pin connector mates with same connectors as used on front panel. Detailed pin allocation is defined in the 4291B User Manual.

SPECIFICATIONS SUBJECT TO CHANGE



SPECIFICATIONS



Inputs:	32 ECL differential line receivers; 110 Ω input impedance; double-pulse resolution < 200 nsec in COMMON STOP mode (not applicable in COMMON START mode); 15 nsec minimum width.
Full Scale:	Continuously adjustable from 512 to 2048 nsec (1 nsec/count to 4 nsec/count). Other options available on request.
Accuracy:	Gain accuracy within 0.1% with absolute accuracy within 1 count.
TDC Range:	9 bits plus overflow.
Common Trigger:	Distributed by 4298 module via the CAMAC Dataway. In the COMMON START mode, the trigger must be supplied 200 nsec before the first expected wire pulse. In the COMMON STOP mode, the trigger must be supplied 200 nsec after the last expected wire pulse.
Pedestal Compensation:	External channel-to-channel variations in Wire input timing of up to $\pm 5\%$ of full scale time may be automatically compensated by the AUTOTRIM feature. (Requires that 4298 test pulses be supplied at the detector.)
Conversion and Transfer Time:	Approximately 35 μsec plus 12 μsec per "HIT" module plus 0.5 μsec per valid word (for 5-meter DATABUS).
Reset (Fast Clear):	Distributed by 4298 module via the CAMAC Dataway. Resets TDC's and HIT registers in less than 300 nsec.
Readout Control:	Requires one Model 4298 module and one 4299 DATABUS Interface. All clocks, controls, test pulses, and data are bused via the CAMAC Dataway.
Trigger Decision Logic Outputs:	HIT pattern is available on upper rear connector P3 of CAMAC module. NOTE: A HIT is registered by any wire input occurring within the digitized time window plus a 10 to 20 percent extension on either end of this window.
Input Connectors:	Two lock and eject dual 17-pin headers. Mates with 3M 3414-6034, AMP 86987-1, or LeCroy CK/34. Pin assignments are listed in the User Manual. Cable should be 34 conductor twisted pair ribbon, Spectrastrip 455-248-34 or LeCroy DC2/34-xx (cable with connectors).
Current Requirements:	+ 24 V at 30 mA - 6 V at 900 mA + 6 V at 700 mA

SPECIFICATIONS SUBJECT TO CHANGE

Dedicated CAMAC Model 4298

Drift Chamber TDC Controller

The 4298 Drift Chamber Digitizer Controller is located in station numbers 24 and 25 of a standard dedicated CAMAC crate containing up to 23 Model 4291 Drift Chamber Digitizer modules. The Controller, designed to read out, calibrate, and test a complete crate of time digitizers, is connected to any CAMAC System via the Model 4299 DATABUS Interface Buffer. A maximum of 16 Model 4298s (or DATABUS compatible controllers) can be daisy chained on the same DATABUS.

The different operating modes of the system are selectable via a set of side-panel accessible switches and four 16-bit internal registers. The ORDER register, the TIME register, and two ADDRESS registers (NL and NH) are CAMAC programmable via the Model 4299 DATABUS Interface. COMMON START or COMMON STOP operation is selected via a side-panel switch.

The block diagram on opposite page provides detailed information on the operation of the Model 4298. In general, the time digitizer's conversion sequence is initiated upon receipt of a trigger signal from the experiment via its EXPeriment COMMON input, which then self inhibits until the end of the clear cycle. At the end of the conversion, compacted data $1 < \text{DATA} < 512$ (data compacting is implemented or suppressed by proper programming of the ORDER register) is automatically transferred to the 4299 DATABUS Interface which acts as a memory buffer for up to 4K words. The data is organized in the 4299 Memory as is shown in the chart below.

At the end of the data transfer, an automatic clear to the digitizers is generated and the 4299 LAM circuit is set On.

The Test or AUTOTRIM features of the Model 4298 are centered around the internally programmable, crystal controlled, time mark generator and the related control logic which provide accurate timing signals on the four START and STOP front panel outputs. To perform an Internal Test or AUTOTRIM of a crate of 4291s, connect equal length cables from the START 2 and STOP 2 outputs to the appropriate INTernal COMMON and TEST inputs (order depends on whether in COMMON START or STOP mode) and generate the Test or AUTOTRIM commands via the 4299. The Wire

WORD #		CONTENTS	
0	OPTIONAL	WORD COUNT	
BIT	16/15	11 / 10	7 / 6
1	N _P MODULE ADDR	0	OPTIONAL
2	A _P CHAN. ADDR	TDC DATA 1	
3	A _P CHAN. ADDR	TDC DATA 2	
4	A _P CHAN. ADDR	TDC DATA 3	
5	A _P CHAN. ADDR	TDC DATA 4	
6	N _P MODULE ADDR	0	OPTIONAL
7	A _P CHAN. ADDR	TDC DATA 5	
8	A _P CHAN. ADDR	TDC DATA 6	
9	DELINING WORD		

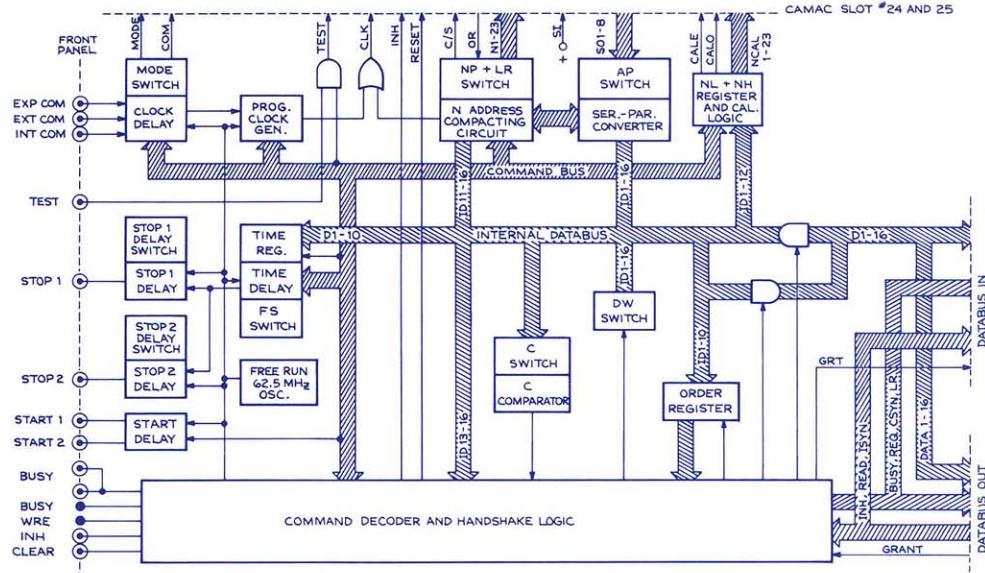
N_P, A_P, DELINING WORD AND OPTIONAL
ARE SIDE PANEL SETTABLE.

inputs will be disabled, and timing pulses will be injected at the TDC inputs. INT COM input simulates the EXPeriment COMMON trigger. The system can also be Tested or AUTOTRIMmed via the front panel Wire input connectors by using START 1 and STOP 1 outputs and the EXTERNAL COMMON along with the external test pulse distribution system for the inputs (including as much of the chamber cabling and preamps as is possible). The added propagation delay of the external wiring can be compensated for by using the side-panel switch-settable digital delay incorporated in the 4298. Proper cabling diagrams are included in the User Manual.

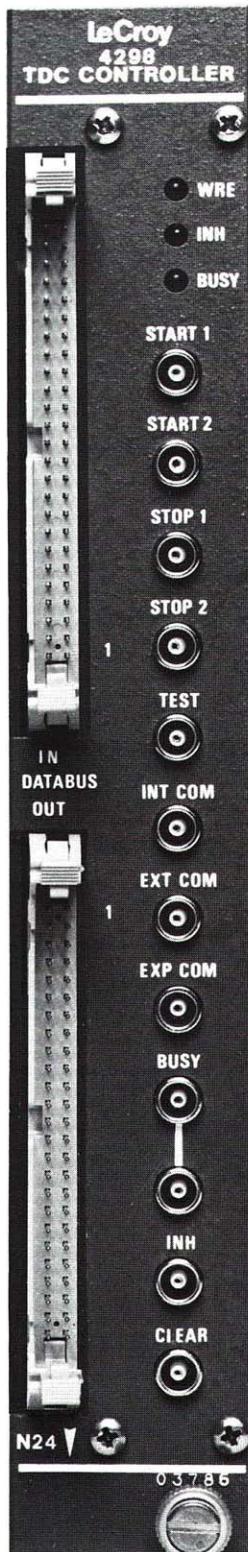
In either internal or external test mode, the TIME register in the 4298 determines the time interval between the START and the STOP pulses allowing precision computer controlled testing of the entire system.

When an AUTOTRIM mode is initiated, the TIME register is alternately set to $t = 0$ for the pedestal trimming and $t = \text{full scale}$ for the gain trimming, with the entire AUTOTRIM cycle performed automatically by the 4298 Controller. If the Chamber System is included in the external mode, any variations or drifts in external preamps, cabling, etc. will be calibrated out.

BLOCK DIAGRAM—MODULE 4298



SPECIFICATIONS



INPUTS

General:

Lemo-type front panel connectors. Require NIM-level inputs. Impedance, 50 ohms $\pm 5\%$. Direct coupled. Reflections $<10\%$ for risetime >2 nsec.

CLEAR:

Resets 4298 and all 4291s in crate. Minimum width 20 nsec.

INHibit:

Inhibit all Wire inputs when activated.

EXperiment COMmon:

Used as the Common Start or Common Stop input. Derived from the experiment trigger. Starts system digitization. Inhibited by INH and/or system BUSY signal.

COMMON START Mode: The 4291 Time Digitizers cannot be stopped during the first 200 nsec following the EXP COM input.

COMMON STOP Mode: The START to the 4291s must precede the EXP COM input by at least 200 nsec.

EXTernal COMmon:

Used as Common Start or Common Stop input when simulated wire pulses are routed to the chamber electronics to include them in test or for AUTOTRIM. Starts system digitization. Disabled by Internal Test mode.

COMMON START Mode: EXT COM input is connected to START 1 output. STOP 1 output signal must be routed to the chamber test pulse system which then generates stop pulses to the time digitizers.

COMMON STOP Mode: EXT COM input is connected to STOP 1 output. START 1 output signal must be routed to the chamber test pulse system which then generates start pulses to the time digitizers.

Used as Common Start or Common Stop input when simulated wire pulses are routed internally via the test line on the CAMAC Dataway to test or AUTOTRIM. Starts system digitization. Disabled by External Test mode.

COMMON START Mode: INT COM input is corrected to START 2 output. STOP 2 output signal must be connected to the TEST input which routes the stop signal to the time digitizers via the test line on the CAMAC Dataway.

COMMON STOP Mode: INT COM input is connected to STOP 2 output. START 2 output signal must be connected to the TEST input which routes the stop signal to the time digitizers via the test line on the CAMAC Dataway.

TEST:

Activates the test line on the CAMAC Dataway for an internal test or AUTOTRIM sequence. This input is disabled in the external mode.

OUTPUTS

General:

Lemo-type front panel connectors.

High impedance (current source) supplies NIM-levels into 50 ohms: (0 levels = $0 \text{ mA} \pm 2 \text{ mA}$; 1 level = $16 \text{ mA} \pm 2 \text{ mA}$). Risetime and falltime <3 nsec. Overshoot 10%.

START 1, 2: Internally generated when a Test or Autotrim cycle is initiated.

STOP 1, 2: Internally generated when a Test or Autotrim cycle is initiated. Delayed from START by precision time mark generator set from TIME register. Both have independent switch-settable delays, where STOP 1 is side-panel accessible to allow for compensation of delay when using the external mode.

BUSY: Double-amplitude NIM pulse generated for duration of conversion and readout.

DATABUS I/O

Allows cascading of multiple LeCroy dedicated Controllers or Processors to one 4299 for data or control word transfer. Cable to 4299 Interface should be LeCroy DAT-DO/50-LL and to other 4298 Controllers should be DAT-DI/50-LL (or use 3M 3302/50 Flat Ribbon Cable with 3M 3425-6050 Connector or LeCroy 403 211 050 Connector). The last processor on the DATABUS requires a Terminator, DAT-TR/50.

SIDE-PANEL SWITCHES

Allows user selection of operating modes and flag bits. See User Manual for detailed setup information.

GENERAL

Packaging:

No. 2 RF-CAMAC module conforming to ESONE Report EUR4100E and IEEE Standard 583.

Current Requirements:

+ 6 V at 2.4 A
- 6 V at 2.4 A

SPECIFICATIONS SUBJECT TO CHANGE

CAMAC Model 4299

DATABUS Interface

The LeCroy 4299 is a single-width CAMAC Interface and Data Buffer designed for use with LeCroy's expanding family of dedicated CAMAC Crate Data Acquisition Systems using DATABUS for efficient control and fast data transfer. These include System 4290, PCOS-III and others. The Model 4299 allows connecting of up to 16 dedicated crates to a single CAMAC station.

The LeCroy Model 4299 DATABUS Interface allows bi-directional 16-bit parallel word transfers between the CAMAC Dataway and dedicated data processing System Controllers (LeCroy Models 4298, 2738, etc.) via standard, economical, easy-to-assemble ribbon cable.

The Interface includes a 4K x 16-bit memory to allow fast block transfer of data between it and the CAMAC interfaced computer. The block diagram and description below provide more detail on use and operation of the Interface.

Transferring data from CAMAC to DATABUS is accomplished one of two ways. The simplest uses a CAMAC Write function and subaddress A(0) to transfer one word at a time to the DATABUS under CAMAC control. (Q-response must be tested each time to be sure of data transfer.) If large amounts of data are to be transferred, the CAMAC Write function with subaddress A(1) is used to allow a block transfer of data to the 4K memory, followed by a F(25)•A(0) to initiate transfer from memory to DATABUS. In either mode, the 4299 Interface writes data to the DATABUS with a synchronization signal, ISYN, which stays true until the addressed Controller acknowledges with a CSYN. (In the case where CSYN is not returned, an automatic 25 μ sec time out will reset ISYN and the function is considered executed.)

Transferring data from a dedicated Controller to CAMAC is always via the memory. Any Controller can initiate a REQuest, which is acknowledged by the 4299 Interface (if its memory is not full or being accessed) with a GRANT signal and READ command (Interface is quiescently in WRITE mode) as long as REQuest is maintained. The Controller sends data with a CSYN which the Interface acknowl-

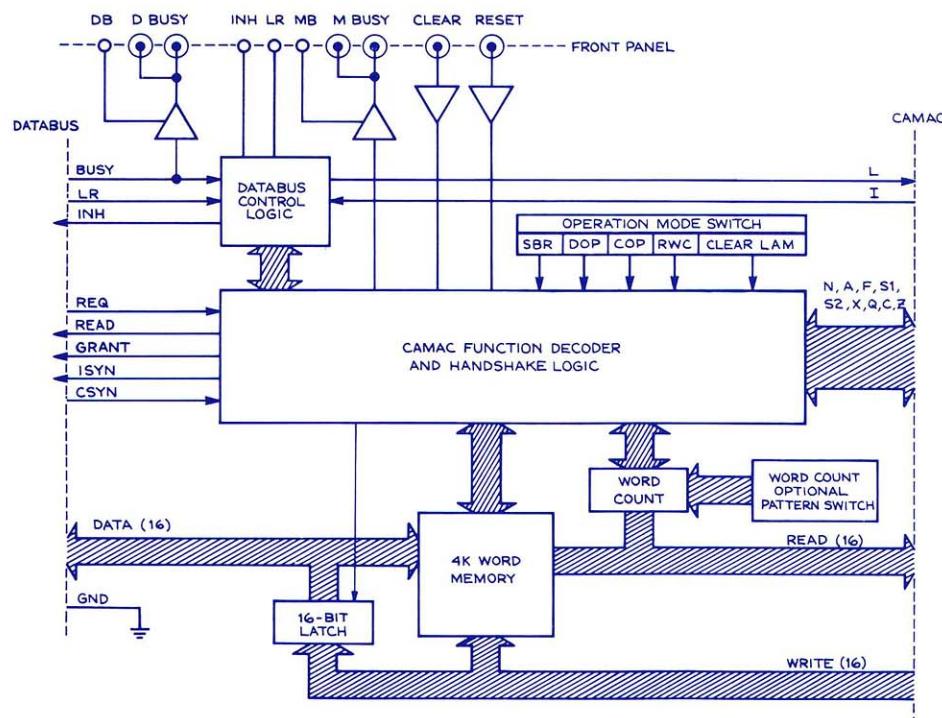
edges with an ISYN as it stores data sequentially in memory. CAMAC LAM is set and memory can now be read out by a CAMAC READ function and subaddress A(0) or A(1). The first word out will always indicate the number of words in memory (located in the 12 LSB's, the 4 MSB's are side-panel switch-settable user option flags). The identification and data words (from the Controller) will sequentially follow every subsequent READ command.

Q-response is maintained until the last word in the data block is read out. While optimized for Block Transfer Reads, data can be read out word by word under CAMAC control. Read out is destructive with subaddress A(0), nondestructive with A(1). If A(1) is used, a new read cycle can be initiated by F(11)•A(1), then cleared at any time by an F(11)•A(0) or other valid memory clear function.

Memory can be protected in various ways using side-panel switch options. SBR (Single Block Read) prevents memory access from DATABUS if the previous memory has not been read or cleared by CAMAC, DOP (DATABUS Overwrite Protect) prevents memory access if data written from CAMAC into memory has not yet been transferred to the DATABUS, and COP (CAMAC Overwrite Protect) prevents memory access from the CAMAC dataway if data written from DATABUS into memory has not yet been transferred to CAMAC. In all cases, the GRANT response to a DATABUS REQuest and the Q-response to a CAMAC command will be suppressed when memory data is to be protected.

An internal LAM (Look At Me) register in the Model 4299 can be set by any dedicated Controller via the DATABUS. It can be tested or cleared by standard CAMAC function commands. It also can be cleared by front panel inputs RT or CL and by options determined by the side-panel settable Clear LAM switches to clear at end of First Word Readout (FWR), at end of Last Word Readout (LWR) or do not clear at read out (DRC), all of which allow use of any of the other valid clear functions, plus a clear via dedicated Controller only (LMD).

BLOCK DIAGRAM—MODULE 4299



SPECIFICATIONS



INPUTS

General:

Lemo-type front panel connectors. Require NIM-level inputs. Impedance, $50 \Omega \pm 5\%$. Direct-coupled. Reflections, $< 10\%$ for risetime > 2 nsec.

Reset (RT):

Resets registers and clears memory. An initialize cycle is generated on the DATABUS. Minimum width: 20 nsec.

Clear (CL):

Clears the memory only. Minimum width: 50 nsec.

OUTPUTS

General:

Lemo-type front panel connectors.

High impedance (current source) bridged outputs supply NIM levels into 25 ohms (0 level = $0 \text{ mA} \pm 4 \text{ mA}$; 1 level = $32 \text{ mA} \pm 4 \text{ mA}$). Risetime and falltimes: < 5 nsec. Overshoot: 10%.

Memory Busy (MB):

Memory Busy Signal indicates that the memory contains data or is being accessed. Front panel MB LED also indicates status.

Databus Busy (DB):

DATABUS Busy Signal indicates that the DATABUS BUSY is activated. Front panel DB LED also indicates status.

DATABUS I/O

Allows cascading of up to 16 LeCroy dedicated Controllers or Processors to one 4299 for data or control word transfer. Cable to first processor or controller should be DAT-DO/50-LL (or use 3M 3302/50 Flat Ribbon Cable with 3M 3425-6050 Connector or LeCroy 403 211 050 Connector). Maximum total cable lengths should not exceed 100 meters. Transfer rate is two megawords per second for total cable length of 5 meters or less, slower for longer runs. (See previous pages for additional information.)

CAMAC COMMANDS

C•S2:

Memory clear (jumper option).

Z•S2:

Clears memory, initializes logic status of the unit and generates initialize cycle on the DATABUS.

I:

Activates DATABUS Inhibit line. Front panel INH LED indicates status.

L:

LAM signal is activated by DATABUS LR request. A front panel LR LED indicates status. (See LOOK AT ME on previous page.)

X:

An X-response is generated when any valid N•F•A command below is recognized even though it may not be executed.

Q:

A Q-response is generated only if the requested function can be executed.

N•F(R)•A(0):

Memory destructive READ function. Can be chosen among CAMAC functions F(0), F(1), F(2) or F(3). Q-response generated if function is executed.*

N•F(R)•A(1):

Memory non-destructive READ function. Can be chosen among CAMAC functions F(0), F(1), F(2) or F(3). Q-response generated if function is executed.*

N•F(8)•[A(0) + A(1)]:

Tests LAM. Q-response generated only if LAM is present.

N•F(9)•[A(0) + A(1)]:

Clears memory, initializes logic status of the unit, and generates initialize cycle on the DATABUS. Q-response generated.

N•F(10)•A(0 + 1):

Tests LAM. A Q-response is generated only if LAM is present. Clears the LAM memory at S2 if the CLEAR LAM switch is not in LMD position.

N•F(11)•A(0):

Clears memory. Q-response generated if memory not activated by the DATABUS.

N•F(11)•A(1):

Initialize memory address counter for a new readout cycle. Q-response generated if memory not activated by the DATABUS.

N•F(W)•A(0):

DATABUS WRITE function. Can be chosen among CAMAC functions F(16), F(17), F(18) or F(19) to write one word at a time on the DATABUS. Q-response generated if function is executed.

N•F(W)•A(1):

Memory WRITE function. Can be chosen among CAMAC functions F(16), F(17), F(18) or F(19). Q-response generated if function is executed.

N•F(24)•[A(0) + A(1)]:

Sets DATABUS INHIBIT. Q-response generated.

N•F(25)•[A(0) + A(1)]:

Triggers the transfer of memory data onto the DATABUS. Q-response generated if data transfer is executed.

N•F(26)•[A(0) + A(1)]:

Resets DATABUS INHIBIT. Q-response generated.

N•F(27)•[A(0) + A(1)]:

Tests DATABUS BUSY signal. Q-response generated if DATABUS BUSY signal is present.

R1 to R16:

Data READ lines.

W1 to W16:

Data WRITE lines.

GENERAL

Packaging:

No. 1 RF-shielded CAMAC module.

Current Requirements:

+ 6 V at 2 A; - 6 V at 200 mA.

*R = 0, 1, 2, 3 is jumper selected on the PC board.

SPECIFICATIONS SUBJECT TO CHANGE

4290 SYSTEM TEST & MAINTENANCE

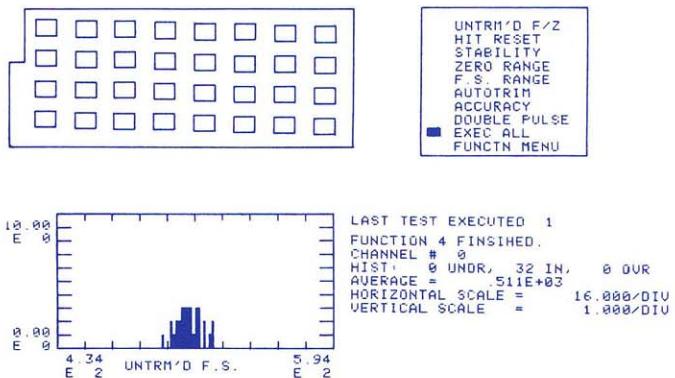
LeCroy's 4291 Series 32 channel TDC's go through extensive testing before delivery to the customer. The TDC Test System is based upon LeCroy's Model 3500 Acquisition & Control System. LeCroy Model 4298 Controller and 4299 DATABUS Interface are the only modules required to perform an Internal Test or AUTOTRIM of a crate of 4291s. A LeCroy Model 4416 16 Channel Discriminator, used to simulate an externally pulsed "chamber system," is required for the external test mode. An extensive software package has been developed to rapidly detect and diagnose malfunctioning TDC channels. This 4290 Test System is used by LeCroy Repair Facilities throughout the world. Researchers with large numbers of 4291 Series TDC's in their data acquisition system find the TDC Test System a highly desirable tool for monitoring and maintaining the performance of experiments.

Tests are performed in sequence on a pass-fail basis. A selection table of tests is displayed on the CRT along with a "monolithic map" of the 4291 module (See Figure 1). The test table permits test selection via light pen; the module map offers visual identification of TDC channels under test. Passing a test is indicated on the 4291 monolithic map by all channels being "illuminated." Channels performing outside of specifications are indicated by a "darkened" block symbol. Light-pen selection of a TDC channel after test gives pertinent data regarding the performance of the channel. Following are summaries of the tests and options available in the TDC test package.

Untrimmed Full Scale. Using the test input (common to all MTD110s), two data points, one at X% and one at Y% (usually 25% and 75%) of the intended full scale are taken. From these data points the *untrimmed full scale* and *untrimmed offset* output are extrapolated. The untrimmed full scale value is checked against the tolerances prescribed by the data sheet. Selection of the DISPLAY option following this test causes a distribution of the untrimmed full scale values for the entire 4291 to be displayed.

Untrimmed Zero. The extrapolated value calculated in the previous test for zero-scale is checked against the tolerances prescribed by the data sheet. Selection of the DISPLAY option following this test produces a display of the untrimmed zero-scale responses for all channels of the 4291 under test.

Stability. A series of conversions are executed at some fraction of full scale input time, and the resulting data are stored in histogramming memory fashion. The *short-term stability* of each channel is checked against the tolerance allowed for



CRT Display during 4291 TDC stability testing. Note test selection table, module map of MTD110 monolithics, and stability test data display format.

in the specifications. Both an *absolute variation* in counts, and an *R.M.S. variation* are specified. Note that this test must precede AUTOTRIM related testing, since stability to within one count is imperative to the convergence of the AUTOTRIM algorithm.

Zero Range. A non-converging AUTOTRIM sequence is performed with readout for "zero-scale" (exactly 256 cycles in order to leave the 8-bit threshold DAC unchanged) allowing the threshold DAC's in each MTD110 to wrap around. From this data set, the *monotonicity*, *step size* and *full range* (in counts) of the offset adjustment is determined. The output must behave monotonically (except for the change at the MSB of the DAC). The maximum step size allowed is one count. Minimum and maximum range (variation) specifications are determined from the data sheet.

Full Scale Range. A non-converging AUTOTRIM sequence is performed for "full scale" (exactly 128 cycles in order to leave the 7-bit slow-current DAC unchanged) allowing the DAC to wrap around. From this data set the *monotonicity*, *step size* and *range* are checked in exactly the same fashion as in the previous test. Range specifications are prescribed in the data sheet.

AUTOTRIM. Without data transfer, full AUTOTRIM sequence is performed. Then for a specified number of tries, full scale and zero-scale conversions are executed. For each "try" every channel is checked for a zero-scale response and a full scale response within the specified AUTOTRIM trim error. If for any one of the tries, a channel is within tolerance, it passes.

Accuracy. A sequence of 33 evenly spaced (from zero to full scale) input times (using the test input) are applied to cause conversions in the mode specified. Since this test follows the AUTOTRIM testing, all channels should be calibrated. From this data, the absolute *accuracy* (thereby incorporating a linearity measurement) in counts is checked against the specification prescribed in the data sheet.

Monolithic is used for computer testing of individual MTD110s. Upon selection of this test, the operator is prompted to select a channel from the module "map" for individual testing. Following a full test on the MTD110, pertinent specifications and performance parameters are displayed (e.g., graphic displays of the raw TDC response, the difference from expected response, zero-range and full scale range AUTOTRIM response, etc.).

Cycle Conversions is used for probing (diagnostic work) the 4291 board to verify waveforms. The System simulates the sequence used to take ACCURACY data.

The Model 3500-based Module Test System is easily expandable to test and maintain other LeCroy Systems, such as the LeCroy 2280 ADC System. For further information, contact your local LeCroy Representative.



LeCroy Model 3500-based Module Test System.



CAMAC Model 4299

Databus Interface

The LeCroy 4299 is a single-width CAMAC interface and data buffer designed for use with LeCroy's expanding family of dedicated CAMAC crate data acquisition systems. These include System 4290, PCOS III, and others. The Model 4299 allows connecting of up to 16 dedicated crates to a single CAMAC station.

The LeCroy DATABUS connects the 4299 with System Controllers (4298, 2738, etc.). This is a bi-directional 16-bit ribbon cable bus. It allows data to be read from LeCroy dedicated crate systems and test or control information to be downloaded to the crates.

The system includes a 4k X 16-bit memory. This allows blocks of data to be transferred to the 4299. Block transfer is ideal for applications which require rapid readout. It may also be operated in the Word Step mode. Data words may be transferred one at a time under CAMAC control.

The Model 4299 has been designed with maximum flexibility for readout of data acquisition systems. The Model 4299 offers destructive or non-destructive readout. It also offers a word count register to facilitate block transfer readout. Side panel accessed switches enable memory overwrite protection from either the Dataway or the DATABUS. Thus, the 4299 may be used as a multiple-event buffer or as a single-event buffer. Front panel Lemo-type connectors allow the user to reset or clear the 4299 with NIM pulses.

A register internal to the Model 4299 can be set by any dedicated controller in the DATABUS chain. This sets the LAM of the Model 4299 and lights a front panel LED labeled LR. The LAM status of the 4299 can be tested or cleared by standard CAMAC commands. It can also be cleared via the front panel Reset or Clear Lemo inputs provided that none of the System Controllers are asserting the LAM.

The operating mode of the LAM circuit can be selected via a side-panel switch, CLEAR LAM. The CLEAR LAM switch has the following four positions:

- LMD: The LAM memory circuit is disabled. Reset is possible via dedicated crate controller only.
- FWR: LAM is reset at the end of the first readout cycle, FR, or by any of the valid clear functions.
- LWR: LAM is reset at the end of the last readout cycle, FR, or by any one of the valid clear functions.
- DRC: LAM is not automatically reset by the readout function, FR. All other clear functions remain valid.

SPECIFICATIONS

CAMAC Model 4299

DATABUS INTERFACE BUFFER

INPUTS

- General: Lemo-type front panel connectors. Require NIM-level inputs. Impedance, $50 \Omega \pm 5\%$. Direct-coupled. Reflections, $< 10\%$ for risetime > 2 nsec.
- Reset (RT): Resets registers and clears memory. An initialize cycle is generated on the DATABUS. Minimum width: 20 nsec.
- Clear (CL): Clears the memory only. Minimum width: 50 nsec.

OUTPUTS

- General: Lemo-type front panel connectors. High impedance (current source) bridged outputs supply NIM levels into 25 ohms (0 level = $0 \text{ mA} \pm 4 \text{ mA}$; 1 level = $32 \text{ mA} \pm 4 \text{ mA}$). Risetime and falltimes: < 5 nsec. Overshoot: 10%.
- Memory Busy (MB): Memory Busy Signal indicates that the memory contains data or is being accessed. Front panel MB LED also indicates status.
- Databus Busy (DB): DATABUS Busy Signal indicates that the DATABUS BUSY is activated. Front panel DB LED also indicates status.

DATABUS I/O

Allows cascading of up to 16 LeCroy dedicated Controllers or Processors to one 4299 for data or control word transfer. Cable to first processor or controller should be DAT-DO/50-LL (or use 3M 3302/50 Flat Ribbon Cable with 3M 3425-6050 Connector or LeCroy 403 211 050 Connector). Maximum total cable lengths should not exceed 100 meters. Transfer rate is two megawords per second for total cable length of 5 meters or less, slower for longer runs. (See previous pages for additional information.)

CAMAC COMMANDS

- C•S2: Memory clear (jumper option).
- Z•S2: Clears memory, initializes logic status of the unit and generates initialize cycle on the DATABUS.
- I: Activates DATABUS Inhibit line. Front panel INH LED indicates status.
- L: LAM signal is activated by DATABUS LR request. A front panel LR LED indicates status. (See LOOK AT ME on previous page.)
- X: An X-response is generated when any valid N•F•A command below is recognized even though it may not be executed.
- Q: A Q-response is generated only if the requested function can be executed.
- N•F(R)•A(0): Memory destructive READ function. Can be chosen among CAMAC functions F(0), F(1), F(2) or F(3). Q-response generated if function is executed.*
- N•F(R)•A(1): Memory non-destructive READ function. Can be chosen among CAMAC functions F(0), F(1), F(2) or F(3). Q-response generated if function is executed.*
- N•F(8)•[A(0) + A(1)]: Tests LAM. Q-response generated only if LAM is present.
- N•F(9)•[A(0) + A(1)]: Clears memory, initializes logic status of the unit, and generates initialize cycle on the DATABUS. Q-response generated.
- N•F(10)•A(0 + 1): Tests LAM. A Q-response is generated only if LAM is present. Clears the LAM memory at S2 if the CLEAR LAM switch is not in LMD position.
- N•F(11)•A(0): Clears memory. Q-response generated if memory not activated by the DATABUS.
- N•F(11)•A(1): Initialize memory address counter for a new readout cycle. Q-response generated if memory not activated by the DATABUS.
- N•F(W)•A(0): DATABUS WRITE function. Can be chosen among CAMAC functions F(16), F(17), F(18) or F(19) to write one word at a time on the DATABUS. Q-response generated if function is executed.
- N•F(W)•A(1): Memory WRITE function. Can be chosen among CAMAC functions F(16), F(17), F(18) or F(19). Q-response generated if function is executed.
- N•F(24)•[A(0) + A(1)]: Sets DATABUS INHIBIT. Q-response generated.
- N•F(25)•[A(0) + A(1)]: Triggers the transfer of memory data onto the DATABUS. Q-response generated if data transfer is executed.
- N•F(26)•[A(0) + A(1)]: Resets DATABUS INHIBIT. Q-response generated.
- N•F(27)•[A(0) + A(1)]: Tests DATABUS BUSY signal. Q-response generated if DATABUS BUSY signal is present.
- R1 to R16: Data READ lines.
- W1 to W16: Data WRITE lines.

GENERAL

- Packaging: No. 1 RF-shielded CAMAC module.
- Current Requirements: + 6 V at 2 A; - 6 V at 200 mA.

*R = 0, 1, 2, 3 is jumper selected on the PC board.



CAMAC Model 4300

16 Channel, Fast Encoding and Readout ADC (FERA)

- **High density:** 16 channels in a single width standard CAMAC module.
- **Fast conversion:** 11 bits in 8.5 μ sec or 10 bits in 4.8 μ sec, 9 bits in 2.8 μ sec.
- **High sensitivity:** 11 bits, 480 pC full scale; 9 or 10 bits, 256 pC full scale.
- **Floating common signal ground:** to eliminate sensitivity to common mode noise (hum) and DC offset.
- **50 or 100 Ω input impedance:** compatible with flat twisted pair cables or 50 Ω multi-coaxial flat cables.
- **Pedestal compensation:** minimizes the gate width effect on the pedestal.
- **Internal pedestal memory:** programmable pedestal subtraction during readout.
- **Programmable zero suppression:** compresses data and accelerates readout.
- **Programmable high speed readout:** 100 nsec/word via front panel ECL port.
- **Sequential or random access CAMAC readout.**
- **Common test feature.**
- **System compatibility:** designed for operation with fast buffer memories, bit slice processors, look up memories, data stacks and other ECL trigger processing units.

The LeCroy Model 4300 Fast Encoding and Readout ADC (FERA) is designed to cover applications where charge measurements and readout must be performed rapidly and with high resolution. The FERA may be used as a single standard CAMAC module, or as part of a large system.

The FERA is a high speed charge integrating analog-to-digital converter. Each module contains 16 independent ADCs that are enabled by a common gate of 50 nsec to 500 nsec duration. Larger gate widths are possible after pedestal adjustment. The inputs, designed to accomodate 17-pair flat cables, offer a common mode rejection of ± 200 mV.

After conversion, the digitized data may be automatically corrected for pedestal with values contained in the internal programmable pedestal memory. Digitized data is available first on the front panel ECL port and, subsequently on the CAMAC dataway. The ECL port readout is optional. All zero data words may be suppressed separately for the ECL port or CAMAC readout to provide data compression. The compression procedure requires 1.6 μ sec (both after the conversion and ECL port readout).

The front panel bus system includes the protocol necessary to permit high speed sequential readout to ECLline compatible modules including the LeCroy Models 2375 Data Stack Module, 2372 Memory Lookup Unit, and 4302 Triple Port Fast Memory. The Model 4302 is the memory extension of the LeCroy 4800 series of Fast Bit Slice CAMAC Processors which permits the distribution of programmable intelligence within the CAMAC system.

The readout modes, pedestals and remote testing of the Model 4300 FERA are controlled via CAMAC. The gate, fast clear, test signals and ECL port timing for up to a crate of FERAs, may be controlled from a Model 4301 FERA Driver.

SPECIFICATIONS CAMAC Model 4300

16 Channel, Fast Encoding and Readout ADC (FERA)

ANALOG INPUTS (16)

Connector:	17 × 2-pin front panel connector (BERG 75789-101-34). The upper 16 pins of the left row are negative signal inputs. The upper 16 pins of the right row are connected to the common virtual ground (AC coupled to ground). The lowest 2 pins are connected to ground.
Input Sensing:	Charge (current integrating).
Full Scale:	256 pC (9 or 10 bits), 480 pC (11 bits).
ADC Resolution:	Two factory options: 9 bits or 10/11 bits; the 10/11-bit selection is made via 4 internal jumpers and adjustment by an internal potentiometer.
Conversion Time:	Typically 9 bits in 2.8 μsec, 10 bits in 4.8 μsec, 11 bits in 8.5 μsec.
Range:	9 or 10 bits typically 256 pC minus ADC pedestal. 11 bits typically 480 pC minus ADC pedestal.
Sensitivity:	10 or 11 bits 0.25 pC/count ± 3%, 9 bits 0.5 pC/count ± 3%.
Input Impedance:	Two factory options: 100 Ω ± 3%, within the range of 0 to -30 mA DC; or 50 Ω ± 3%, within the range of 0 to -60 mA DC. Above these limits, diode protection clamping will affect input impedance.
Input Protection:	± 25 V for 1 μsec transients (clamping diodes to ground and -3 V).
Input Limitations:	Maximum current for linear response -30 mA. With 50 Ω input impedance, the linearity is degraded to typically ± (1% of reading + 0.25 pC) for -60 mA.
Common Mode Properties:	Common mode rejection ratio > 50 dB for ± 200 mV (DC to 1 kHz).
ADC Isolation:	> 50 dB.
Integral Linearity:	Typically ± 0.5 pC. Worst case ± (0.25% of reading + 0.5 pC) for signals of slew rate < 2 mA/nsec. For signals of slew rate 4 mA/nsec, linearity is degraded to typically ± (1% of reading + 0.25 pC).
Differential Linearity:	Typically ± 10%, worst case ± 20%.
Residual Pedestal:	Minimum 1 pC and maximum 13 pC for a gate width from 50 to 500 nsec and all inputs open. Adjustable with an internal potentiometer for gate width > 500 nsec. Subtracted from data by CAMAC command.

Pedestal/Gate Width Coefficient:	$< \pm 8 \text{ pC}/\mu\text{sec}$, typically $\pm 3 \text{ pC}/\mu\text{sec}$.
Operating Temperature:	0° to 40° C.
Temperature Coefficient:	Typically $(-0.05\% \text{ of reading} \pm 0.1 \text{ count})/\text{°C}$ for a gate width of 500 nsec. Coefficient may vary slightly for other gate widths.
Long Term Stability:	$\pm (0.25\% \text{ of reading} + 0.5 \text{ pC})/\text{week}$ at constant temperature and voltage.

COMMAND BUS

Connector:	8 x 2-pin front panel connector. The input matching resistors and output pull down resistors may be removed for high impedance inputs and outputs. When these resistors are in place, a front panel LED (PD ON) is lit.
Input Levels:	Differential ECL levels, 100 Ω impedance differential.
Output Levels:	Differential ECL levels (into 100 Ω differential).
Gate Input (GATE):	One, common for all ADCs. Non-retriggerable. Gate width 50 to 500 nsec ($> 500 \text{ nsec}$ is possible after pedestal adjustment). Gate must precede input signals by at least 20 nsec.
Clear Input (CLR):	One, common for all ADC front ends and digital logic. May be executed at any time. Minimum clear width: 5 nsec. CLEAR settles to within 1 count in less than 2 μsec during conversion, the action is immediate after conversion.
Request Output (REQ):	One, ECL port readout request indicates that this module is ready to take control of ECL port data transfer. After conversion time, REQ is set only if the ECL port readout is programmed and the module contains valid data.
Write Strobe Output (WST):	One, indicates when the data is valid on the ECL port output. WST is set in a minimum of 10 nsec after the data is presented to the ECL port (settling time) and released when the write acknowledge is received. The ECL port data is stable during entire WST pulse. Minimum write strobe width 40 nsec.
Write Acknowledge Input (WAK):	One, acknowledge signal from the ECL port receiver indicating data has been loaded and the next data word may be sent. The next WST is set 50 nsec after the release of WAK. Minimum write acknowledge width 30 nsec.
Test Reference Voltage Input (TRV):	Two paralleled front panel 2-pin connectors, high input impedance (200 kΩ), accept the Test Reference Voltage; second connector usable for monitoring or daisy chaining. The gate and charge pulses are generated at the input of all ADCs by the CAMAC function F(25)•A(0). The test charge pulse is proportional to the DC level at the TRV input. Channel-to-channel matching of the proportionality constant is $\pm 1\%$. TRV input range: 0 to + 10.24 V, equivalent to 0 to 512 pC $\pm 0.1\%$ on each ADC. The common virtual ground offset is automatically compensated.

ECL PORT ENABLE/PASS

Readout Enable Input (REN):	1 × 2-pin front panel connector. Accepts differential ECL levels. Input impedance 100 Ω differential. Indicates to this module that it can take control of the ECL Port Bus. The REN signal must be maintained during entire readout time. REN enables the ECL port outputs, WST output and WAK input if the module is ready for data transfer (REQ output ON).
Pass Output (PASS):	1 × 2-pin front panel connector, generates differential ECL levels (into 100 Ω differential). Indicates that this module has finished using the ECL port or is not ready. PASS output is activated by the REN input signal and closed by the REQ output internal command. Transit time between REN input and PASS output typically 3 nsec if module empty.

ECL PORT OUTPUT

Connector:	17 × 2-pin front panel connector; (BERG 75789-101-34). The last 2 pins are not connected.
Output Levels:	Differential ECL levels (into 100 Ω differential). The pull down resistors may be removed for high impedance outputs. When these resistors are in place, a front panel LED (PD ON) is lit.
Specifications:	Data word size: 16 bits. Sequential data readout with maximum output frequency 10 MHz (see Readout Block Format).

CAMAC COMMANDS

Note: after a GATE, the module is BUSY (=1), and only the data readout functions are enabled. The BUSY status is released (=0) only after a clear CAMAC function or front panel CLR signal.

Z:	Initializes module; clears the module and sets the seven command bits of the status register to 1.
C:	Clears the module.
I:	Inhibits the front panel GATE during CAMAC inhibit command.
X:	X response is generated for all valid functions.
Q:	Q response is generated only if a function can be executed.
L:	Look-At-Me (LAM) set, if enabled, after the end of conversion (or ECL port readout) and if there is valid data to be read. LAM is cleared by Z, C, F(9), F(10), front panel CLR or, if sequential read is selected, by F(2) after the last data has been read.
F(0)•A(0)	Read status word register. R1 to R15; R16 = 0; Q = 1 if BUSY = 0.
R1 to R8:	VSN; Virtual Station Number: index source for sequential readout with zero suppression.
R9:	EPS; ECL port Pedestal Subtraction: when EPS = 1, pedestals are subtracted for ECL port readout.
R10:	ECE; ECL port data Compression Enable; when ECE = 1, data zeros are suppressed for ECL port readout.
R11:	EEN; ECL port ENable: when EEN = 1, ECL port readout is permitted.

R12: CPS; CAMAC Pedestal Subtraction: when CPS = 1, pedestals are subtracted for CAMAC readout.

R13: CCE; CAMAC data Compression Enable: when CCE = 1, data zeros are suppressed for CAMAC sequential readout.

R14: CSR; CAMAC Sequential Readout: when CSR = 0, CAMAC random access readout is enabled; when CSR = 1, CAMAC sequential readout is enabled.

R15: CLE; CAMAC LAM Enable: when CLE = 1, LAM is enabled.

Note: The seven bits, EPS to CLE, are set to 1 by the CAMAC Z function.

F(1)•A(0-15):

Reads pedestal memory on R1 to R8; R9 to R16 = 0.

Random access to the 16 pedestal words.

Channels 0 to 15 are addressed by subaddresses 0-15.

Q = 1 if BUSY = 0.

F(2)•A(0-15):

CSR = 0; random access to the 16 ADC values. Reads ADC value on R1 to R11; R12 to R16 = 0. Channels 0 to 15 are addressed by subaddresses 0-15. Q = 1 if BUSY = 1 and data are ready.

CSR = 1; sequential readout of ADC values. Reads ADC value on R1 to R16 (see Readout Block Format). The increment to the next word is triggered by S2. Q = 1 if BUSY = 1 and as long as valid data to be read are present. The subaddress A is not decoded.

F(8)•A(0):

Tests Look-At-Me. Q = 1 if LAM is present.

F(9)•A(0):

Clears the module. Q = 1.

F(10)•A(0):

Tests and clears LAM. Q = 1 if LAM is present; LAM reset at S2 if set.

F(16)•A(0):

Writes status word register. W1 to W15; W16 not used; see F(0) for assignment. Q = 1 if BUSY = 0. The status word register is loaded at S1.

F(17)•A(0-15):

Random access for writing of the 16 pedestals. Writes pedestal memory on W1 to W8; W9 to W16 not used. Channels 0 to 15 are addressed by subaddress 0-15. Q = 1 if BUSY = 0. The 8-bit pedestal word is loaded at S1.

F(25)•A(0):

Enables test. Q = 1 if BUSY = 0.

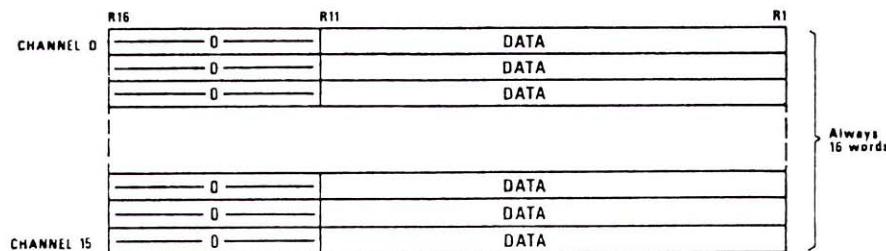
The gate is opened for 550 nsec at S2. The TRV input generates a charge proportional to the TRV for each ADC. Maximum rate 10 kHz; recovery time 100 μ sec.

READOUT BLOCK FORMAT

Without Zero Suppression:

ECL port readout;
CAMAC readout;

EEN = 1, ECE = 0.
CSR = 1, CCE = 0.

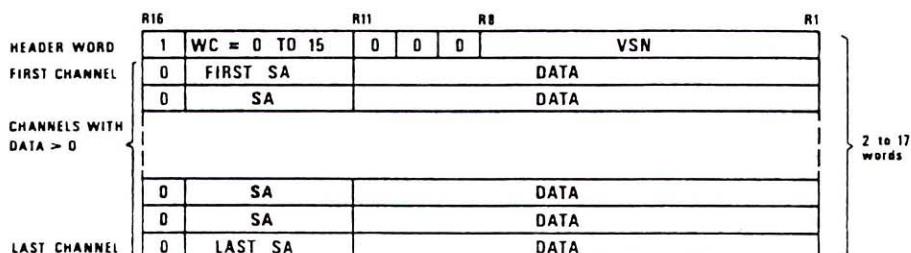


DATA: 9-bit resolution; 0 to 511;
overflow = 2047.
10-bit resolution; 0 to 1023;
overflow = 2047.
11-bit resolution; 0 to 1919;
overflow = 2047.

With Zero Suppression:

ECL port readout;
CAMAC readout;

EEN = 1, ECE = 1.
CSR = 1, CCE = 1.



VSN: Virtual Station Number loaded in the Status Register.
WC: Number of data words following the header word, 0 indicates 16 data words.
DATA: 9-bit resolution; 1 to 511;
overflow = 2047.
10-bit resolution; 1 to 1023;
overflow = 2047.
11-bit resolution; 1 to 1919;
overflow = 2047;
SA: Channel SubAddress.

GENERAL

Packaging:

RF-shielded, # 1 width CAMAC module.

Power Requirements:

2.1 A at +6 V; 2.7 A at -6 V

0.1 A at +24 V (65 mA plus 1.5 times average input current).

Note: when all output pull down and input matching resistors are removed, the current at -6 V is reduced to 2.4 A.



CAMAC Model 4301

Fast Encoding and Readout ADC (FERA) System Driver

- Provides all utility functions for a full crate of LeCroy Model 4300 FERAs including:
 - Gate and Clear signals distributed to all FERAs.
 - Write Acknowledge used in ECL Bus transfers distributed to all FERAs.
 - Bus Request for the ECL Bus received from all FERAs, available on the front panel.
 - Write Strobe for the ECL Bus transfers received from all FERAs, available on the front panel.
 - Variable Test Reference Voltage distributed to all FERAs for testing and calibration. Generated from CAMAC controlled 12-bit DAC.
- ECL and NIM Inputs and Outputs.
- 16-Channel Single-Ended ECL to Differential ECL Converter.

The Model 4301 Fast Encoding and Readout ADC System Driver provides a simple mechanism for the distribution and collection of common signals for up to an entire crate of Model 4300 FERAs. The functions include all ADC control functions such as Gate and Clear as well as all timing and control functions for the ECL Port.

An internal CAMAC controlled Digital-to-Analog Converter (DAC) permits precise generation of reference voltage levels for test and calibration of the Model 4300 FERAs.

The Model 4300 FERAs use an ECL Port for 10 MHz readout of the 16-bit data words. When bussed together, these standard differential ECL signals become single-ended ECL. The signals must be converted back to differential ECL before being sent to a standard ECLLine logic module or memory unit. This translation is conveniently handled by the Model 4301. To permit simple interconnections, connectors are located at the same position as those of the Model 4300 ECL Port and the Model 4302 Triple Port Fast Memory Module.

The Model 4301 FERA Driver uses two separate ECL Busses. The Command ECL Bus is used to receive and distribute signals used by a set of FERAs via an 8 × 2-pin connector. The Data ECL Bus is connected to the ECL Ports of the Model 4300 FERAs and carries the data during fast readout. The Data ECL Bus uses a standard ECLLine 17 × 2-pin connector for both input and output interconnections. LeCroy recommends one Model 4301 be used with up to 22 Model 4300 FERAs, a full CAMAC crate.

SPECIFICATIONS

CAMAC Model 4301

FERA DRIVER

INPUT/OUTPUT CHARACTERISTICS

Gate (GAI & GATE):

Two inputs (GAI); Lemo-type connector accepts NIM signal levels (50 Ω input impedance), and 1 x 2-pin connector accepts differential ECL signals (100 Ω input impedance). Inputs are OR'd and available on the Command ECL Bus (GATE) for distribution to the Model 4300 FERAs.

Clear (CLI & CLR):

Two inputs (CLI); Lemo-type connector accepts NIM signal levels (50 Ω input impedance), and 1 x 2-pin connector accepts differential ECL signals (100 Ω input impedance). Inputs are OR'd and available on the Command ECL Bus (CLR) for distribution to the Model 4300 FERAs.

Write Acknowledge
(WAI & WAK):

Two inputs (WAI); Lemo-type connector accepts NIM signal levels (50 Ω input impedance), and 1 x 2-pin connector accepts differential ECL signals (100 Ω input impedance). Inputs are OR'd and available on the Command ECL Bus (WAK) for distribution to the Model 4300 FERAs. The WAK may also echo the WST signal after a fixed time delay as described below.

Write Strobe
(WST & WSO):

Input via Command ECL Bus (WST) from the Model 4300 FERAs. Two Outputs (WSO); Lemo-type connector generates NIM signal levels into 50 Ω impedance, and 1 x 2-pin connector generates differential ECL signals into 100 Ω. For synchronous operation, the WSO signal may be connected directly to the WAI via a fixed delay cable or active delay.

Inhibit Readout
(IRI):

Two inputs (IRI); Lemo-type connector accepts NIM signal levels (50 Ω input impedance), and 1 x 2-pin connector accepts differential ECL signals (100 Ω input impedance). Inputs are OR'd and act as a veto for the REO signal described below. Since the REO is usually connected to the first Model 4300 FERA to be read out, the IRI inhibits the readout and may be used to block the readout process until the receiver module is ready.

Readout Request
(REQ, RQO & REO):

Input via Command ECL Bus (REQ) from the Model 4300 FERAs. Following a fixed delay, three outputs are generated (factory setting for delay, 200 nsec; may be adjusted by internal potentiometer RQ DEL). The first two outputs (RQO) may be used to signal a request to readout; Lemo-type connector generates NIM signal levels into 50 Ω impedance, and 1 x 2-pin connector generates differential ECL signals into 100 Ω. The third output (REO) can be vetoed by the IRI signal and is normally connected to the REN or Readout Enabled input of the first Model 4300 FERA to be read out; 1 x 2-pin connector generates differential ECL signals into 100 Ω.

Test Reference
Voltage (TRV):

Internal CAMAC controlled 12-bit DAC generates a precision reference voltage on the Command ECL Bus (TRV), for testing and calibrating the Model 4300 FERAs (see complete description below).

ECL Data Bus
(IN & OUT):

16 inputs via 17 x 2-pin connector (IN). Accepts single ended ECL signals from the ECL Ports of the Model 4300 FERAs. Generates differential ECL outputs on the 17 x 2-pin connector (OUT) for all 16 signals.

TEST REFERENCE VOLTAGE SPECIFICATIONS

The TRV output on the Command ECL Bus is driven by an internal CAMAC controlled Digital-to-Analog Converter (DAC). The DAC uses a control register which may be set and read via CAMAC commands (see below).

WARNING: the register content is randomly set at power on.

Range:

0 to 10.2375 V corresponding to inputs for the Model 4300 FERA of 0 to 511.875 pC.

LSB:

2.5 mV corresponding to inputs for the Model 4300 FERA of 0.125 pC.

Integral Linearity:

± 0.5 LSB.

Full Scale Error:

± 1 LSB.

Settling Time:

5 μsec.

Current Limit:

3 mA.

CAMAC COMMANDS

X, Q:

X and Q responses are generated for each valid function.

F(0)*A(0):

Reads the contents of the 12-bit DAC control register on CAMAC lines R1 to R12. X and Q responses are generated.

F(9)*A(0):

Generates a CLR signal on the Command ECL Bus at time S1. Same action as front panel CLI input. X and Q responses are generated.

F(16)*A(0):

Sets the contents of the 12-bit DAC control register from CAMAC lines W1 to W12. X and Q responses are generated.

GENERAL

Packaging:

RF-shielded # 1 width CAMAC module.

Current Requirements:

100 mA at +6 V; 1.2 A at -6 V.
20 mA at +24 V; 30 mA at -24 V.

SPECIFICATIONS SUBJECT TO CHANGE

TECHNICAL DATA

LeCroy



CAMAC ECL_{line} Model 4302 Triple Port Fast Memory Unit

- **Fast Access Time: 100 nsec.**
- **Large Size: 16K by 16-bits.**
- **Two Read/Write Ports and One Write Port.**
- **Compatible with FERA, the LeCroy Fast Encoding and Readout ADC System.**
- **Compatible with PCOS III, the LeCroy multiwire Proportional Chamber System.**
- **May be used to Expand the Memory of the LeCroy Series 4800 CAB Programmable CAMAC Processors.**

The LeCroy Model 4302 Triple Port Fast Memory Unit has been designed for a variety of applications requiring large fast buffer memories. A large fast access time buffer memory may be used to liberate front-end electronics in high data rate applications. Several events may be accumulated in the buffer for subsequent readout and processing.

With a 100 nsec access time to the 16K by 16-bit memory, the Model 4302 is fast enough to be a complement to ECL_{line}, the fast pulse CAMAC programmable logic system from LeCroy. The flexibility of the module is further enhanced by the Model 4302's three ports. The memory unit has a read/ write port to CAMAC, a read/write port to the LeCroy 4800 series of fast intelligent CAMAC processors (CAB), and, finally, a fast ECL write port on the front panel for rapid data loading. Several 4302 modules may be cascaded to extend the memory capacity to multiples of 16K.

Data loaded into the Model 4302 Memory Unit may be accessed either by CAMAC or directly by a LeCroy Series 4800 CAB Programmable CAMAC Processor. The Model 4302 can be directly connected to the CAB via the CAB internal bus and data is available within the indirect address space of the processor. Up to four Memory Units can be directly coupled to the CAB for a total of 64K 16-bit words.

A typical application of the Model 4302 is with one or more LeCroy Model 4300 Fast Encoding and Readout ADCs (FERA) accessing the Model 4302 Memory Units via their front panel ECL Ports.

SPECIFICATIONS

CAMAC ECLine Model 4302

TRIPLE PORT FAST MEMORY UNIT

INPUT CHARACTERISTICS

Data Inputs:	Front panel, 34-pin connector accepts complementary ECL signals; 100 Ω input impedance; up to 16 parallel bits can be accepted and stored in the memory word addressed at the strobe pulse arrival time; memory address is automatically incremented by one at the end of the strobe pulse.
Strobe Veto (VETO):	Front panel, 2-pin connector accepts complementary ECL pulses. 100 Ω input impedance; an input signal acts as a veto on the Write Strobe Input (WSI). Connecting the <u>FULL</u> output on the VETO input in adjacent Model 4302s permits simple cascading of memory units. WSI and Data Inputs must also be connected.
Write Strobe (WSI):	NIM: two bridged Lemo-type connectors, high input impedance, accepts NIM level pulses; unused input must be terminated. ECL: front panel, 2-pin connector accepts complementary ECL pulses; 100 Ω input impedance. The leading edge of the strobe pulse must fall inside the data pulse and must arrive at least 10 nsec after the data are valid; minimum width 20 nsec; maximum frequency 10 MHz for both NIM and ECL.
Clear Address Counter (CLR):	NIM: Lemo-type connector, input impedance 50 Ω, minimum pulse width 20 nsec, accepts NIM level pulses; an input pulse resets the memory address and clears the LAM.

OUTPUT CHARACTERISTICS

Overflow (OVF):	NIM: Lemo-type connector; generates NIM level pulses when terminated in 50 Ω. ECL: front panel, 2-pin connector generates complementary ECL levels. When the ECL port is enabled, a signal is generated as long as the memory address is equal to or exceeds the value that has been preset by switches on the side of the module; the output is active until the memory address is changed (either by the CAB or by CAMAC). The two side panel switches permit the selection of 12288, 14336, 15360, or 15872 as the overflow address.
Acknowledge (ACK):	ECL: front panel 2-pin connector, generates a complementary ECL signal; echoes WSI with 35 nsec delay time; inhibited if the address counter has reached full memory capacity.
Memory Full (<u>FULL</u>):	ECL: front panel 2-pin connector, generates a complementary ECL level; active as long as the address counter has not reached the full memory capacity.

CAB COMMANDS AND FUNCTIONS

G I ₂ -I ₅ :	Sets operation mode in the addressed memory. I ₅ ,I ₄ = 2-bit memory address. I ₃ ,I ₂ = mode: 00 = no action; 01 = enable CAMAC, disable CAB and ECL port; 10 = enable CAB, disable CAMAC and ECL port; 11 = enable ECL port, disable CAMAC and CAB; This general function may be executed at any time.
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TxW0: Writes address pointer.
 TxW1: Writes a 16-bit data word into the actual address and increments address by one.
 TW0x i: Reads address pointer, where $i = 0, 1, 2, 3$ is the address of the memory unit.
 TW1x: Reads a 16-bit data word out of the actual address and increments address by one.
 Note: The transfer instructions yield valid results only when in CAB operation mode.
 x = any source of destination register on the CAB data bus.

CAMAC COMMANDS AND FUNCTIONS

L: A LAM is generated on overflow (OVF).
 Z: Resets memory address to zero and clears the LAM.
 X: X = 1 response is generated for each valid CAMAC function.
 Q: Q = 1 response is generated for any executable function unless otherwise specified.
 F(0)•A(0): Reads 16-bit data at the current memory address; increments the address by one at S2. No Q response is generated when the address pointer exceeds the memory capacity.
 F(1)•A(0): Reads memory address on 16 bits (R1 to R16). The presence of the two most significant bits indicates memory address overflow.
 F(1)•A(1): Reads mode register (CAMAC Read Lines R1 and R2).

R2	R1	
0	1	CAMAC Enabled
1	0	CAB Enabled
1	1	ECL Enabled

F(2)•A(0): Reads 16-bit data at the current memory address and decrements the address pointer by one at S2. The first F(2)•A(0) reads the address pointer. The Q response is suppressed on further F(2)•A(0) reads after the data word at address 0 has been read.
 F(8)•A(0): Tests LAM.
 F(10)•A(0): Tests and clears LAM.
 F(16)•A(0): Writes 16-bit data at the current memory address; increments the address by one at the end of S1. No Q response when the pointer exceeds the memory capacity.
 F(17)•A(0): Writes memory address on 14 bits (W1 to W14).
 F(17)•A(1): Writes mode register (CAMAC Write Lines W1 and W2).

W2	W1	
0	0	Disables all modes
0	1	Enables CAMAC
1	0	Enables CAB
1	1	Enables ECL

F(24)•A(0): Disables LAM.
 F(26)•A(0): Enables LAM. LAM is generated on overflow.

F(0)•A(0), F(1)•A(0), F(2)•A(0), F(16)•A(0), and F(17)•A(0) cannot be executed and no Q response is generated unless the unit is in CAMAC operation mode.

GENERAL

Packaging: RF-shielded, # 1 width CAMAC module.
 Power requirements: 2.2 A at +6 V; 200 mA at -6 V.

TECHNICAL DATA

LeCroy



CAMAC ECLine™ Model 4415 16 Channel Programmable Non-Updating Discriminator

- **High Density:** 16 channels in a single width CAMAC module
- **Medium Counting Rate:** 50 MHz
- **Threshold Range:** 30 mV to 600 mV differential
- **Complementary or Single Ended Inputs:** suitable for flat, inexpensive, twisted pair cables
- **Complementary Differential ECL Outputs:** drive flat twisted pair cable
- **Output Masking:** simulates desired trigger configuration
- **Built-in Test Feature:** permits testing of all enabled channels
- **Common Veto:** permits simultaneous fast inhibiting of all channels

The new generation of high energy physics experiments, involving extremely high counting rates and/or large detector arrays, requires a "total system" approach to instrumentation. LeCroy's new CAMAC 4000 Series of ultra-fast, high-density programmable instrumentation modules provides the solution to this requirement by allowing the experimenter to achieve full computer control of the data acquisition system within a single instrumentation standard.

The Model 4415 is a medium speed multichannel discriminator designed to meet the existing demands of modern high, medium, and low energy physics. It offers very low cost, high reliability using custom built monolithic circuits, low complexity, local or remote programmability features, and testing capability. Moreover, the option for grounding one of the two input pins permits using the 4415 as positive, negative, or differential input discriminators.

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Low Cost/High Density

The 4415 offers substantial savings over conventional shapers or discriminators. Packaged 16 channels to a single width CAMAC module, it not only costs less per channel, but also cuts down on rack space by at least a factor of four and decreases the cost of associated cabling and power supply hardware.

The high density of the 4415 is made possible through extensive use of dedicated monolithics (MVL100) and the selection of CAMAC packaging. Use of the CAMAC standard permits high density by providing increased power with adequate cooling to maintain reliable operation.

Low Complexity/High Reliability

The complementary inputs and outputs are designed for use with inexpensive flat or individual cables, allowing fast and accurate system interconnections. The low parts count resulting from the elimination of the usual ECL-to-NIM conversion stage and from the inclusion of the timing stage in the MVL100 yields low cost and high reliability. ECL outputs provide the convenience of compatibility with most large-scale in house-designed trigger decision circuits, as well as, with LeCroy's other Series 4000 programmable units. The output widths are adjustable from 10 to 300 nsec. A test input, on a front panel Lemo type connector accepting NIM level negative pulses, allows a fast simultaneous test of all channels, and a veto front panel input allows simultaneous fast inhibiting of all channels.

SPECIFICATIONS CAMAC Model 4415

16 CHANNEL PROGRAMMABLE NON-UPDATING DISCRIMINATOR

INPUT CHARACTERISTICS

Signal Inputs:	16, BERG 75789-101-34, front panel 34 pins connectors. Differential, DC-coupled (AC coupled on request, common mode ± 30 V). Impedance, $110 \Omega \pm 5\%$ differential; $55 \Omega \pm 5\%$ from each pin to ground.
Threshold:	Adjustable via front panel screwdriver control or via an external voltage applied to the threshold control connector, common to all channels.
Threshold Control:	AMP 87230-1, front panel 2 pin connector; impedance, $5.6 \text{ k}\Omega$. Used as output, indicates the internal threshold control voltage. Used as input, commands the threshold control voltage.
Threshold Range:	30 mV to 600 mV differential ± 10 mV or $\pm 10\%$ whichever is greater.
Threshold Control Ratio:	Threshold monitor point on front panel has 10:1 ratio of monitor voltage to actual voltage. Range, -0.3 V to -6 V.
Hysteresis:	$150 \mu\text{V}$, typical.
Input-Output Delay:	(10 ± 2) nsec, typical.
Test Input:	One Lemo type front panel connector, $50 \Omega \pm 2\%$, triggers all channels; requires NIM level signal (> -600 mV); minimum width, 10 nsec; maximum rate, 50 MHz. Test is enabled when the remote/local switch is in remote mode only. Front panel LED indicator.
Veto Input:	One Lemo type front panel connector, $50 \Omega \pm 2\%$, permits simultaneous fast overlap inhibiting of all channels; requires NIM level signals (> -600 mV); direct coupled.

OUTPUT CHARACTERISTICS

Signal Outputs:	2 × 16, two outputs per channel in two BERG 75789-101-34, front panel 34-pin connectors; ECL differential level (−0.8, −1.7 V) into 100 Ω twisted pair; duration, 10 nsec to 300 nsec ± 3 nsec or ± 5% whichever is greater. Continuously variable via front panel screwdriver control, common to all channels; risetimes and falltimes typically 2.2 nsec; width stability < 0.2%/°C.
	Individual channels are CAMAC maskable by overlap with a 16-bit masking register.

CAMAC COMMANDS

X:	An X-response is generated when a valid N, A, F command is recognized.
Q:	A Q-response is generated only if the requested function can be executed.
Z:	Disables mask register and clears test mode at S2 time.
I:	Disables all outputs in remote mode (internal jumper option disables I).
N.F (16)•A(0):	Writes mask register pattern (W1-W16) at S1 time. A Q-response is always generated.
N.F (17)•A(0):	W1 = 1 enables test mode at S1 time. W1 = 0 resets test mode at S1 time. A Q-response is always generated.
N.F (25)•A(0):	Test function, triggers all channels at S1 time. A Q-response is given in test mode when the remote/local switch is in remote mode only.
N.F (27)•A(0):	Remote/local switch test. A Q-response is given in remote mode only.

REMOTE/LOCAL SWITCH

Front-panel switch.
In local mode, disables mask register, test mode, N.F (25) •A(0) and I.

GENERAL

Maximum Frequency:	50 MHz
Double Pulse Resolution:	Typical 110% of width output (between leading edges) or plus width plus 12 nsec whichever greater.
Time Slewing:	< 2 nsec for input amplitudes from 2 to 20 times over threshold.
Test Output Delay:	Typical 27 nsec
Veto Output Delay:	Typical 10 nsec
Multiple-Pulsing:	None; one and only one output pulse is produced for each input pulse regardless of input pulse amplitude and duration.
Power Requirements:	900 mA at + 6 V 1950 mA at − 6 V 20 mA at − 24 V

SPECIFICATIONS SUBJECT TO CHANGE



CAMAC ECL_{line} Model 4416B

16 Channel Programmable Updating Discriminator

- **High density:** 16 channels in a single width CAMAC module.
- **High counting rate:** 150 MHz operation; typical 5 nsec double pulse resolution.
- **Low threshold:** 15 mV to > -1 V.
- **Standard input connectors:** Lemo type, special design.
- **Complementary ECL outputs:** differentially drive flat twisted pair cable.
- **Burst Guard mode and veto input:** permit predictable operation under difficult conditions.
- **Programmable threshold:** local or remote.
- **Threshold monitor:** both analog and digital.
- **Input masking:** simulates desired trigger configuration.
- **Built-in test feature:** permits testing all system components.

The new generation of high energy physics experiments, involving extremely high counting rates and/or large detector arrays, requires a "total system" approach to instrumentation. LeCroy's new CAMAC 4000 Series of ultra-fast, high-density programmable instrumentation modules provides the solution to this requirement by allowing the experimenter to achieve full computer control of the data acquisition system within a single instrumentation standard.

The new Model 4416B is a unique, high speed multichannel discriminator designed to meet the exacting demands of modern high energy physics. It offers low cost and high density, very high speed with low complexity, local or remote programmability features, and self-testing capability.

Low Cost/High Density

The Model 4416B, offers substantial savings over conventional quad or octal discriminators. Packaged 16 channels to a single width CAMAC module, it not only costs less per channel, but also cuts down on rack space by at least a factor of four. It decreases the cost of associated cabling and power supply hardware.

The unprecedented density of the Model 4416B is made possible through extensive hybridization, the use of a specially designed Lemo type input connector assembly, and the selection of CAMAC packaging. Use of the CAMAC standard permits high density by providing increased power with adequate cooling to maintain reliable operation.

High Speed/Low Complexity

The Model 4416B has been designed with 150 MHz counting rate capability. This significant advance, made possible by LeCroy's new LD401 hybrid, results in low system dead time and subsequent higher trigger efficiency.

Two complementary ECL outputs per channel are designed for use with inexpensive flat or individual cables, allowing fast and accurate system interconnections. Elimination of the usual

ECL-to-NIM conversion stage and the inclusion of the timing stage in the LD401 hybrid, yields low cost and high reliability. ECL outputs provide the convenience of compatibility with most large scale trigger decision circuits, and with LeCroy's other Series 4000 programmable units. The output widths are adjustable from 3 to 40 nsec. Output widths up to 100 nsec are possible with the restriction that minor output width modulation effects may occur if the input width and output width are equal.

Local or Remote Programmability

Use of the CAMAC standard provides the option of either local or remote programming and monitoring of the common threshold level. The threshold is adjustable via front panel potentiometer or via CAMAC instructions to an internal 10-bit DAC, from -15 mV to greater than -1 volt. Accurate threshold monitoring is accomplished locally via a front panel monitor point or remotely via CAMAC command and an internal ADC. The remote setting and reading capability provides the convenience of computer controlled plateau measurements.

For additional system flexibility, input masking is made possible by simultaneously inhibiting any combination of the 16 inputs via CAMAC command. This feature allows the user to generate or simulate any desired trigger configuration and perform complete point-to-point checks of the system electronics.

A built-in test feature simulates an input signal for each channel upon receipt of either an F(25) command or a NIM level signal applied to a Lemo type rear panel test input connector. This permits rapid, simultaneous testing of all enabled discriminator channels.

SPECIFICATIONS CAMAC Model 4416B 16 CHANNEL PROGRAMMABLE UPDATING DISCRIMINATOR

INPUT CHARACTERISTICS

Signal Inputs:

16, Lemo type front panel connectors, $50 \Omega \pm 2\%$.
Protected to $\pm 5 A$ for $0.5 \mu\text{sec}$ clamping at +1 and -6 volts.
Reflections < 4% for input pulses of 2 nsec risetime.
Stability better than $0.2\%/\text{ }^{\circ}\text{C}$ over $20\text{ }^{\circ}\text{C}$ to $60\text{ }^{\circ}\text{C}$ operating range offset $\pm 1 \text{ mV}$.
Threshold, -15 mV to -1023 mV $\pm 5\%$ or $\pm 1.5 \text{ mV}$, whichever is greater, (common to all channels); front panel screwdriver adjust in local or through 10-bit DAC in remote mode. (See note)
Threshold monitor point on front panel has 10:1 ratio of monitor voltage to actual voltage $\pm 5\%$.
Hysteresis, typical 6 mV.

Test Input:

1, Lemo type connector on rear panel, $50 \Omega \pm 2\%$, triggers all enabled channels.
Requires NIM level signal ($> -600 \text{ mV}$).
Minimum width: 3 nsec.
Maximum rate: 150 MHz.

Veto Input:

1, Lemo type front panel connector, $50 \Omega \pm 2\%$.
Permits simultaneous fast inhibiting of all channels.
Requires NIM level signal ($> -600 \text{ mV}$).
Direct coupled.
Must precede input signal by approximately 3.5 nsec and overlap its leading edge in update mode or overlap complete input signal in Burst Guard mode.
Minimum duration: 5 nsec.

OUTPUT CHARACTERISTICS

Two bridged outputs per channel.
ECL level (-0.8, -1.7 volt) into 100Ω twisted pair.
Duration, 3 nsec to 40 nsec. (Up to 100 nsec with restrictions (see text above).
Continuously variable via screwdriver control, common to all channels.
Risetimes and falltimes typically 1.5 nsec.
Width stability better than $0.25\%/\text{ }^{\circ}\text{C}$ maximum.

CAMAC COMMANDS

X:	An X-response is generated when a valid N, A, F command is recognized.
Q:	A Q-response is generated only if the requested function can be executed.
Z:	Clears mask register at S2 time.
N•F(1)•A(0):	Reads threshold setting when in local or remote mode.
N•F(16)•A(0):	Writes mask register pattern (W1-W16).
N•F(17)•A(0):	Writes threshold setting register; 11 bits, 10 bits of data providing 1 mV resolution are used to program common threshold received on W1-W10 and 1 bit to set the manual threshold value (front panel screwdriver control) to the threshold register received on W11. In this case, the data presented on W1-W10 are ignored. Requires S1 and remote mode switch position.
N•F(25)•A(0):	Test function. Only channels not masked off by F(16) are triggered by internally generated 3 nsec wide pulse.
N•F(27)•A(0):	Remote/local switch test. A Q-response is given when the front panel switch is in remote mode only.

GENERAL

Double-Pulse Resolution:	Typical, 5 nsec.
Time Slewing:	0.5 nsec for input amplitudes from 2 to 20 times over threshold.
Input-Output Delay:	< 14 nsec.
Test Output Delay:	< 16 nsec.
Multiple Pulsing:	None; one and only one output pulse is produced for each input pulse regardless of input pulse amplitude and duration.
Burst Guard:	A rear panel switch enables the burst guard operation for all channels. The selection of this mode is indicated by a front panel LED.
Power Requirements:	60 mA at + 24 V 400 mA at + 6 V 3.4 A at - 6 V 30 mA at - 24 V

Note: For frequencies higher than 120 MHz or input pulse widths smaller than 4 nsec, the minimum input charge needed above threshold becomes critical. This has the effect of increasing the effective threshold and hysteresis (for further details, see instruction manual).

SPECIFICATIONS SUBJECT TO CHANGE



CAMAC ECLline Model 4418 16-Channel Programmable Logic Delay/Fan-Out

- **High density:** 16 independent delay lines in a single-width CAMAC module.
- **Programmable:** full CAMAC control features permit computerized timing adjustment.
- **Low cost:** per-channel cost significantly lower than for conventional non-programmable delay units.
- **Solid-state reliability:** no switches, no relays, no faulty contacts.
- **Deadtimeless:** specially designed passive delay lines operate at frequencies above 100 MHz.
- **Power-off memory:** internal supply maintains delay settings for several hours when CAMAC crate power goes down.
- **Fan-out capability:** triple outputs provide fan-out of 3 per channel.

For the first time in a single-width CAMAC module, the new LeCroy ECLline Model 4418 Logic Delay/Fan-Out combines the advantages of unprecedented 16-channel density, computer programmability, and deadtimeless solid-state reliability—all at a lower per-channel cost than conventional “delay boxes”!

The 16 independent delay lines, each with a fan-out of three, are individually programmable via CAMAC in steps of one or two nanoseconds (other options available for large quantities). Power supply backup ensures that delay settings are retained even when CAMAC crate power goes down. The use of ECL gates instead of mechanical switches and relays eliminates the reliability problems associated with conventional delay boxes. Because all delay components are passive, deadtimeless operation up to 100 MHz and above is ensured.

CAMAC control of delay lines permits computerization of such routine tasks as coincidence curve-taking, one of the main uses of delay units. The Model 4418 is compatible with all other LeCroy ECLline CAMAC modules.

The new generation of high energy physics experiments, involving extremely high counting rates and/or large detector arrays, requires a “total system” approach to instrumentation. LeCroy’s new CAMAC 4000 Series of ultra-fast, high-density programmable instrumentation modules provides the solution to this requirement by allowing the experimenter to achieve full computer control of the data acquisition system within a single instrumentation standard.

SPECIFICATIONS

CAMAC Model 4418

16-CHANNEL PROGRAMMABLE LOGIC DELAY/FAN-OUT

INPUT CHARACTERISTICS

Number of Inputs: 16; all identical.
100 Ω direct-coupled; high impedance by simple user option.
Reflections <10% for complementary ECL signals of 2 nsec risetime.
Minimum width: 5 nsec.

Input Sensitivity: ± 200 mV differential.

OUTPUT CHARACTERISTICS

Complementary Outputs: Three per channel.
ECL levels (-0.8 and -1.7 V).
Capable of driving 100 Ω twisted pair cable.
Duration equal to input pulse duration ± 1 nsec (4418/16) or ± 1.2 nsec (4418/32).
Risetimes and falltimes, 2.5 nsec into 100 Ω termination.

CAMAC COMMANDS

X, Q: An X and Q-response are generated when a valid N, A, F command is recognized.

F16•(A0 to A15): Load delay time setting on write lines W1 to W4.
One subaddress for each channel.

GENERAL

Double-Pulse Resolution: <10 nsec.

Maximum Rate: >100 MHz.

Input-Output Delay: (15 ± 1) nsec $+(0-15)$ nsec in steps of 1 nsec, option 4418/16.
 $+(0-30)$ nsec in steps of 2 nsec, option 4418/32.

Precision on total delay increment: ± 1 nsec, option 4418/16.
 ± 2 nsec, option 4418/32.

Precision of Step Increment: Total delay/15 ± 300 psec, option 4418/16.
Total delay/15 ± 500 psec, option 4418/32.

Power Requirements: $+6$ V at 50 mA.
 -6 V at 2.5 A.

Power Off Memory: 2 hours min. (typical 10 hours).

Crosstalk: If adjacent channels get synchronous pulses, then the measured channel can be affected by ± 1 nsec; typical.

LONG RANGE OPTION

Double-Pulse Resolution: <30 nsec.

Maximum Rate: >35 MHz.

Input-Output Delay: (15 ± 1) nsec $+(0-120)$ nsec, option 4418/128.

Precision on total delay increment: ± 8 nsec.

Precision of step increment: Total delay/15 ± 2.5 nsec.

Minimum Input Width: >25 nsec.

Output Width: Equal to input width ± 4 nsec.

SPECIFICATIONS SUBJECT TO CHANGE



CAMAC ECL_{ine} Model 4431

8 Channel, 4-Bit Programmable Prescaler

- **High Density:** 8 channels in a single-width CAMAC module
- **High Counting Rate:** 140 MHz
- **Input/Output Levels:** complementary ECL, suitable for flat twisted-pair cable
- **Prescaling Factors:** individually programmable via CAMAC or by front-panel commands
- **Output Masking:** disables undesired outputs
- **Common Inhibit:** inhibits all inputs
- **Common Test:** permits testing of all enabled channels
- **Common Reset:** resets all channels
- **OR Output:** logical OR of all 8 outputs

The LeCroy Model 4431 is a programmable prescaler designed especially to extend the maximum working frequency of either the Models 4432 and 4434 thirty-two channel, 24-bit Latching Scalers or the Model 4433 thirty-two channel, 16-bit Latching Scaler.

The prescaling factors are individually programmable under either CAMAC or front-panel control and may be monitored via dataway read commands. The input to output transit time is independent of the prescaling factor, making the 4431 very useful in altering trigger logic rates without timing readjustment. Individual output widths are continuously adjustable in the range 4-20 nsec via front-panel potentiometers. A mask register may be used to disable individual channel outputs and is programmable by either CAMAC commands or front-panel switches. In the CAMAC mode, the status of the mask is displayed by panel mounted LED's. In addition to the individual outputs, the 4431 also generates an OR output whose output duration is equal to the time overlap of the channel outputs.

Front-panel inputs allow for external test, reset, and inhibit of the unit. Eight line twisted-pair connectors are used for signal input/output and employ complementary ECL levels which are fully compatible with all ECL_{ine} modules.

The new generation of high energy physics experiments, involving extremely high counting rates and/or large detector arrays, requires a "total system" approach to instrumentation. LeCroy's new CAMAC 4000 Series of ultrafast, high-density programmable instrumentation modules provides the solution to this requirement by allowing the experimenter to achieve full computer control of the data acquisition system within a single instrumentation standard.

SPECIFICATIONS CAMAC Model 4431

8 CHANNEL, 4-BIT PROGRAMMABLE PRESCALER

INPUT CHARACTERISTICS

Signal Inputs:	8, in a 2x8-pin front-panel connector; accepts differential ECL input levels; 110 Ω input impedance pin to pin; direct coupled. Minimum input pulse width: 4 nsec; maximum input frequency: 140 MHz.
Test Inputs:	1, in a 2x1-pin front-panel connector; accepts differential ECL input levels; 110 Ω input impedance pin to pin; direct coupled; triggers all 8 channels at once. Minimum input pulse width: 4 nsec; maximum input frequency: 140 MHz.
Reset Inputs:	1, in a 2x1-pin front-panel connector; accepts differential ECL input levels; 110 Ω input impedance pin to pin; direct coupled; resets all 8 prescalers (loads PRESC FACTOR). Minimum input pulse width: 6 nsec.
Inhibit Inputs:	1, in a 2x1-pin front-panel connector; accepts differential ECL input levels; 110 Ω input impedance pin to pin; direct coupled; inhibits all 8 channel outputs for the duration of the signal.

OUTPUT CHARACTERISTICS

Signal Output:	8, in a 2x8-pin front-panel connector; complementary ECL levels. Width: front-panel adjustable from <4 to >20 nsec for each channel; updating outputs. Output width stability: ±(0.5 nsec + 0.5% width).
OR Output:	1, in a 2x1-pin front-panel connector; complementary ECL levels. OR output equals the logical OR of all 8 channel outputs.

CAMAC COMMANDS AND FUNCTIONS (remote mode)

C:	Resets all 8 prescalers (Loads PRESC FACTOR) at S2 (equivalent to front-panel RESET input).
Z:	Initialize the unit, i.e., clears mask register and resets all prescaling factors to 16 at S2.
X:	X=1 response is generated for any of the following functions.
Q:	Q=1 response is generated for any of the following functions only if the unit is set to remote mode.
N•F(0)•A(0) to A(8):	Read the mask register onto R1-R8.
N•F(1)•A(0) to A(8):	Read the prescaling factor of the addressed channel A(0) to A(8) onto R1-R4.
N•F(9)•A(0) to A(8):	Reset all prescalers (loads PRESC FACTOR) at S2 (equivalent to front-panel reset input).
N•F(16)•A(0) to A(8):	Write the mask register, data on W1-W8. A "1" on a write line inhibits the corresponding channel.
N•F(17)•A(0) to A(8):	Write the prescaling factor of the addressed channel A(0) to A(8); data on W1-W4. Prescaling factor = data + 1.

FRONT PANEL SWITCHES AND LED'S

Local Switch (1):	Select the 4431 operating mode. When set in local mode, all CAMAC functions are disabled and the front-panel switches are enabled.
Local Led (1):	When ON, it indicates LOCAL operation.
Mask Switch (1):	Selects MASK or PRESC FACTOR control (only in local mode).
Data Switches (8):	a. <i>MASK mode</i> : 8 data switches (1, 2, 3, 4, 5, 6, 7, 8) select mask pattern (only in local mode). A "1" inhibits the corresponding channel. b. <i>PRES Factor mode</i> : 4 data switches (1, 2, 4, 8) select prescaling factor (1-16). 3 data switches (1, 2, 4,) select channel address (1-8) (only in local mode).
Data LED's (8):	a. <i>MASK mode</i> : 8 LED's display the current mask register state (always in remote mode !). b. <i>PRES Factor mode</i> : 4 LED's display the current prescaling factor of the channel selected by the 3 data switches (1, 2, 4) (only in local mode).
Store Push Button (1):	a. <i>MASK mode</i> : Writes the selected (8 data switches) mask pattern into the mask register. b. <i>PRES Factor mode</i> : Writes the desired prescaling factor (4 data switches) into the selected channel (3 data switches). Each of the 8 prescaling factors must be loaded individually.

GENERAL

Double Pulse Resolution	< 7 nsec
Input to Output Transit Time:	14±2 nsec; independent from the prescaling factor.
Packaging:	RF-shielded single-width CAMAC module.
Power Consumption:	< 300 mA at +6 V < 2.2 A at -6 V < 70 mA at -24 V

SPECIFICATIONS SUBJECT TO CHANGE



CAMAC ECLine Model 4434

32 Channel 24-Bit Latching Scaler

- **High Density:** 32 Scalers, 24 bit each, in a single width CAMAC Module
- **Auxiliary Bus Output:** for interconnection with external raster scan display
- **Medium Counting Rate:** 20 MHz
- **Input Levels:** complementary ECL or single ended TTL
- **Common Load, Common Clear, Common Veto:** on the Front Panel or via CAMAC Command
- **LAM Generation**
- **Sequential or addressed readout**

The LeCroy Model 4434 contains 32 channels of 24-bit scalers. Through the extensive use of LeCroy custom built hybrid circuits, the Model 4434 achieves a dramatic increase in channel density with a very low overall cost per channel.

Each channel is identical and is followed by an internal buffer which may be used to store and readout accumulated data independent of data acquisition.

Inputs to the 4434 are complementary ECL levels compatible with all ECLline modules. Single ended TTL levels are available as a factory option. Each scaler counts signals which have a duration > 10 nsec and a maximum frequency of 20 MHz, assuming the module is not disabled by either the front panel veto or CAMAC Inhibit. However, a local double pulse resolution of 30 nsec is permitted. Receipt of a CAMAC or front panel Load command temporarily halts the scalers and transfers the contents to the internal buffer memory. The scalers may then be optionally cleared before counting is resumed.

Memory readout may take place at any time, independent of data acquisition, under standard CAMAC or Auxiliary Data Bus control. In either case, readout can be performed both sequentially or randomly.

The Auxiliary Bus organization is designed to permit connection of up to 16 modules to the same bus.

The new generation of high energy physics experiments, involving extremely high counting rates and/or large detector arrays, requires a "total system" approach to instrumentation. LeCroy's new CAMAC 4000 Series of ultra-fast, high-density programmable instrumentation modules provides the solution to this requirement by allowing the experimenter to achieve full computer control of the data acquisition system within a single instrumentation standard.

SPECIFICATIONS

CAMAC ECLine Model 4434

32 CHANNEL 24-BIT LATCHING SCALER

INPUT CHARACTERISTICS

Signal Inputs:	32, in two 2×17 -pin front panel connectors, BERG 7578D-101-34.
Input Levels:	Differential ECL (Factory option is available to accept TTL single-ended inputs with the scaler incrementing on the negative going transition).
Input Impedance:	110Ω pin-to-pin with differential ECL, 560Ω to $+5$ V for TTL single-ended inputs.
Input Pulse Width:	10 nsec minimum.
Double Pulse Resolution:	Less than 30 nsec.
Maximum Frequency:	> 20 MHz.
Maximum Instantaneous Rate:	> 30 MHz.

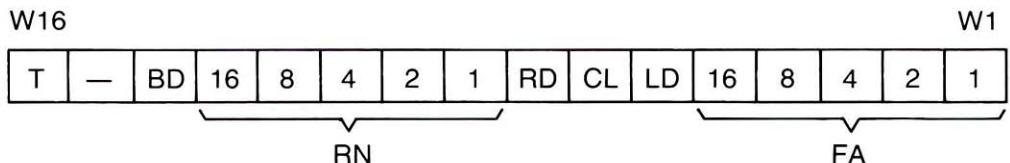
COMMAND INPUTS

General:	The LOAD, CLEAR and VETO inputs each have a single front panel Lemo-type connector; a common side-switch selects either negative going NIM or TTL levels, input impedance 50Ω for NIM pulses; 50Ω AC and 100Ω DC to $+5$ V for TTL pulses.
Load Input:	A LOAD pulse with > 10 nsec width will disable inputs for 220 nsec and shift the scaler contents into a 32-word \times 24-bit buffer; the LOAD command can optionally generate a LAM on the CAMAC dataway and also prepare the memory for readout by loading the starting subaddress (FA) and readout number (RN) previously defined by a CAMAC F(16) or Z; a front panel LED (RDE, Readout Enabled) is lit in recognition of a Load command.
Clear Input:	A CLEAR pulse with > 20 nsec width will disable inputs for a duration of approximately 100 nsec and clear the 32 scalers.
Veto Input:	Disables inputs for the duration of the VETO (action identical to CAMAC INHIBIT).

CAMAC COMMANDS AND FUNCTIONS

Note:	The following notation is used in this section: CR: Command Register; loaded by F(16) FA: First Address to be read RN: Readout Number; defines how many channels (minus one) have to be read in the module
Z:	Initialize the unit at S2, i.e. all scalers, buffer and LAM are cleared as well as register CR.
C:	Clear all scalers at S2.
I:	All scaler inputs are inhibited during CAMAC INHIBIT command; the action is identical to that of the front panel VETO input.
X:	A X = 1 response is generated in recognition of any valid function.
Q:	A Q = 1 response is generated in recognition of any executable function.
L:	A Look-At-Me signal can be generated according to several possible options described in the "Option Switches" section below.
N•F(0)•A(0):	Generates readout of the selected channel; F(0) can be executed and a Q = 1 response will be provided under the following conditions: a) Side switch LAD (Latching Disable) = ON: always if the LED RDE (Readout Enabled) is ON. b) Side switch LAD = OFF: only after a LOAD has been performed and as long as the readout of the given number of channels had not been completed.
N•F(2)•A(0):	Sequential data readout with auto-increment of the address; F(2) can be executed and a Q = 1 response will be provided independent of the Latching Disable switch position, if a LOAD has been previously performed, and as long as the readout of the given number of channels has not yet been completed. Note: if the number of scalers to be read is RN + 1 > 32-FA then the readout, after address 31, will continue with addresses 0, 1, 2, etc. until RN + 1 channels have been read.

- N•F(8)•(0): Test LAM: Q = 1 response is generated when LAM is ON.
- N•F(10)•A(0): Test and clear LAM; a Q = 1 response is generated when LAM is ON. LAM is cleared at S2.
Note: LAM goes on again after F(10) in the following cases:
 a) Switch LOF (LAM at Overflow)=ON and scaler not cleared.
 b) Switch LDR (LAM Data Ready)=ON and data readout not finished.
- N•F(16)•A(0): Load register CR (Command Register); F(16) can always be executed and a Q = 1 response is generated.
The Command Register is a 16 bit word with the following format and explanation:



- FA: First Address to be read.
- RN: Readout Number; defines how many channels (minus one) have to be read starting from the address FA; after a Z command, RN is set to 31 and FA to 0.
- T: Test; when T = 1 permanently inhibits signal inputs; increments at S2 all scalers by one count; after a Z command T = 0.
- LD: Load; LD = 1 performs a load if switch LAD (Latching Disable) = OFF; after 0.8 μ sec the module will be ready for readout; enables functions F(0) and F(2).
- CL: Clear; CL = 1 clears all the 32 scalers.
- RD: Readout enable; RD = 1 prepares the module for readout, does not require a LOAD; readout can be started after 0.8 μ sec.
- BD: Bus Disable; BD = 1 disables the Auxiliary Bus readout; after a Z command BD = 0.

OPTION SWITCHES

- A set of side accessible switches allows the user to select different options as follows:
- LAD: Latching Disable; when ON the module works as a normal non-latching scaler.
- OVF: Overflow decides whether an overflow condition occurs when bit 16 of any scaler is ON or when bit 24 is ON.
- LCO: Load and Clear at Overflow when ON.
- LOF: LAM at Overflow; a LAM is generated when at least one channel reaches the overflow set value.
- LRE: LAM at Readout Enable; a LAM is generated after a readout request.
- LDR: LAM Data Ready; a LAM is generated after a readout request and as long as there are data to be read.
- BAD: 4-bit Bus Address; defines module address in the auxiliary bus.
- VBR: Veto by Bus Readout; enables a veto of all scaler inputs during the loading of the auxiliary bus output registers (< 200 nsec).
- NIM/TTL: Decides pulse standard accepted by inputs LOAD, CLEAR and VETO:
 NIM: 0 = 0 mA 1 = - 12 mA
 TTL: 0 = + 2.5 V 1 = + 0.5 V

AUXILIARY BUS

A total of 16 LeCroy Model 4434 Modules may be interfaced to an auxiliary bus via a front panel 34-pin connector. The auxiliary bus must end in an independent dedicated controller. Use of the auxiliary bus permits addressed readout of the scaler contents independent of CAMAC operations for applications such as raster scan display.

GENERAL

- Packaging: Single width CAMAC standard module.
- Power Consumption: TTL-Version ECL-Version
- | | | |
|-------|-------|--------|
| + 6 V | 2.8 A | 3.1 A |
| - 6 V | 40 mA | 400 mA |



CAMAC ECLine Model 4448 48-Bit Coincidence Register

- **High density:** 48 bits in a single-width CAMAC module.
- **Low cost:** with three times conventional density, per-bit cost decreases drastically.
- **ECL inputs:** 100 Ω complementary inputs simplify total system.
- **MWPC application:** ideal in high-rate applications using cable delays.
- **Analog sum output:** three analog outputs (groups of 16 bits) permit fast majority decisions.
- **Fast common gate:** provides coincidence resolving time under 3 nsec.
- **Fast clear:** rejected events can be cleared in less than 5 nsec.

The LeCroy Model 4448 Coincidence Register ("pattern unit") offers fast storage capability at an unprecedented high density and low cost. Its complementary ECL line receiver input stage, compatible with inexpensive twisted-pair flat cable, makes it perfectly suitable for both small and large multiwire proportional chamber and hodoscope systems. The three fast analog outputs providing majority information are extremely useful in fast trigger decision applications.

The logic channels, which seek a coincidence between each input and a common fast gate input, provide coincidence resolving times under 3 nsec. Logical "1" data levels, representing the time coincidence between the common gate and the 48 inputs, are stored in a 48-bit fast buffer register for later readout under CAMAC commands. The facility of performing majority logic is provided by three front-panel summing outputs which are each driven by 16 logic channels. The output current of the summing circuit is proportional, in increments of 100 mV into 50 Ω per register bit, to the number of coincidences stored in the register. Other operating features include a front-panel clear input, which responds to negative logic levels, and a built-in test mode.

High Density/Low Cost

The modern design and a new concept of input interconnection have resulted in a dramatic density increase over present designs. With 48 bits per slot, up to 1104 bits of fast coincidence registers can be housed in one CAMAC crate.

Besides the advantage of reducing the physical size of an experimental setup, high density cuts down CAMAC overhead and per-bit cost. This new system concept also permits substantial savings on interconnection costs.

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The new generation of high energy physics experiments, involving extremely high counting rates and/or large detector arrays, requires a "total system" approach to instrumentation. LeCroy's new CAMAC 4000 Series of ultra-fast, high-density programmable instrumentation modules provides the solution to this requirement by allowing the experimenter to achieve full computer control of the data acquisition system within a single instrumentation standard.

MWPC Applications

Its high density and low cost per bit make the Model 4448 Coincidence Register well suited for multiwire proportional chamber work. Its complementary line receiver input stage is fully compatible with the LeCroy Model 7790 16-channel chamber card, as well as with most in-house designed MWPC amplifier-discriminators.

The simplicity of system setup obtained using the Models 7790 and 4448 is very attractive for small systems. It is also feasible for large systems in high-rate conditions where cable delays must be used to minimize deadtime.

High-speed readout of large systems can be performed through a dedicated controller using the LAM structure to skip empty modules. Encoded data is then transferred to the LeCroy Model 4299 memory module.

Hodoscope Applications

In hodoscope applications, the Model 4448 Coincidence Register is used in conjunction with the Model 4416, a 16-channel 200 MHz updating discriminator with complementary ECL outputs.

In cases where cost is a primary consideration, the Model 4448 can be directly connected with the LeCroy Model 4415, a 16-channel, 80 MHz non-updating discriminator.

SPECIFICATIONS CAMAC Model 4448 48-BIT COINCIDENCE REGISTER/PATTERN UNIT

INPUT CHARACTERISTICS

Number of Inputs:	48; all identical. 100 Ω direct-coupled; high impedance by simple user option. Reflections <10% for complementary ECL signal of 2 nsec risetime. Minimum width < 4 nsec.
Input Sensitivity:	± 200 mV differential.
Double-Pulse Resolution:	8 nsec max.; 6 nsec typical.
Gate Input:	One; Lemo-type connector; 50 Ω impedance; -600 mV or greater; minimum duration at full logic level (-750 mV), 3.0 nsec.
Clear Input:	One; Lemo-type connector; -600 mV or greater, 50 Ω impedance; minimum duration 5 nsec; 2 nsec settling time after clear.

OUTPUT CHARACTERISTICS

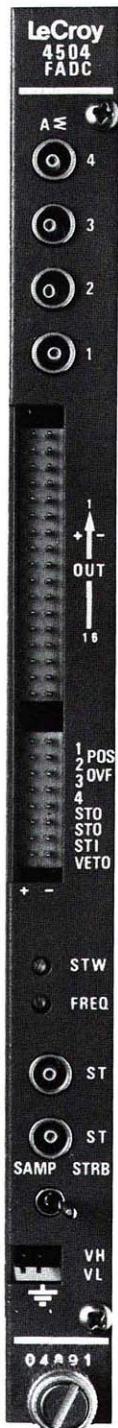
Summing Outputs:	3 identical: one for each of the three groups A, B, C of 16 bits each. -100 mV $\pm 5\%$ into 50 Ω is presented for each register latched in the corresponding group of 16. Maximum output into 50 Ω , -0.7 volt corresponds to 7 set registers; risetime 3 nsec, delay of leading edge of summing output from leading edge of coincident input; 9 nsec.
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CAMAC COMMANDS

Z or C:	Clears registers during S2. (Used for special test feature option.)
I:	Inhibit gate input.
F0·A0:	Reads register A.
F0·A1:	Reads register B.
F0·A2:	Reads register C.
F2·A0:	Reads and clears register A.
F2·A1:	Reads and clears register B.
F2·A2:	Reads and clears register C.
F9·A0:	Clears register A.
F9·A1:	Clears register B.
F9·A2:	Clears register C.
F8·(A ₀ + A ₁ + A ₂):	Tests LAM.
F11A·(A ₀ + A ₁ + A ₂):	Clears all registers.
L:	LAM: logic OR of all registers (switchable on or off for each register A, B or C).

GENERAL

Gate-Input Delay:	2.5 nsec typical.
Coincidence Width:	2.5 nsec up, determined by input and gate pulse durations.
Packaging:	CAMAC single-width module.
Power Requirements:	+6 V: 400 mA -6 V: 1.9A



CAMAC ECLine Model 4504

4 Channel 4-Bit Flash ADC

- 4 Independent flash ADC's, 4 bits plus overflow
- 100 MHz with sampling times down to 4 nsec
- Variable voltage range
- Front panel fast data output
- External strobe or internal free running sampling strobe

The Model 4504 has been designed for applications where digital representations of analog signals are required.

The unit contains four identical channels each of which accepts an analog voltage of up to 5 V. Upon receipt of a strobe pulse, each input signal is converted to a 4-bit digital word. The inputs may be sampled at a frequency of up to 100 MHz with sampling times as short as 4 nsec.

The accepted voltage range of the 4504 may be tailored to the characteristics of the input signals by adjusting two voltage levels, common for the four channels, via two 8-bit CAMAC programmable DAC's. Each voltage level may be set between -2.5 V and +2.5 V. The voltage difference between these two levels gives the analog voltage range which will be quantized into 15 equally spaced intervals and finally coded into a 4-bit binary digital word.

A digital overflow output is provided for each channel to indicate that the input pulse has exceeded the positive full scale limit. In case of an overflow, that channel's overflow bit is set to one. The four bits of the corresponding digital output word can be forced to one or zero depending on the position of a side switch.

A strobe output timed with the flash ADC outputs is also provided for use in subsequent logic operations.

Typical applications for this unit include situations where the analog majority level provided by several ECLine units (4417, 4448, 4532) has to be converted into a digital information for use with the ECLine Model 4508 Fast Lookup Memory.

When used with pulses from photomultipliers, wire chambers or other detectors, the 4504 acts as a multithreshold discriminator encoding the pulse amplitude into the four output bits. The 4504 measures voltage. To digitize charge, the input should be preceded by an integrator.

The new generation of high energy physics experiments, involving extremely high counting rates and/or large detector arrays, requires a "total system" approach to instrumentation. LeCroy's new CAMAC 4000 Series of ultra-fast, high-density programmable instrumentation modules provides the solution to this requirement by allowing the experimenter to achieve full computer control of the data acquisition system within a single instrumentation standard.

SPECIFICATIONS

CAMAC ECLine Model 4504

4 CHANNEL 4-BIT FLASH ADC

INPUT CHARACTERISTICS

- Analog Inputs (A_{\leq}): 4, one per channel; Lemo-type connectors; 50Ω input impedance; direct coupled; minimum input pulse width 10 nsec.
- Strobe Input (STI): 1, common to the four channels; front panel two pin connector; 110Ω input impedance; accepts complementary ECL pulses; minimum input width 4 nsec; maximum frequency 100 MHz; the trailing edge of the strobe pulse will hold the digital output until the next strobe pulse arrives.
- Veto Input (VETO): 1, in a two pin front panel connector; 110Ω input impedance; accepts complementary ECL pulses; vetoes the strobe input during its width.

OUTPUT CHARACTERISTICS

- Digital Outputs (OUT): 16, four per channel, in a 2×17 pin front panel connector; provides complementary ECL pulses; the four outputs represent a four-bit binary word giving the digital translation of the analog value at the input; the digital outputs change state in coincidence with the trailing edge of the strobe pulse and hold until the next strobe pulse is applied.
- Overflow Outputs (POS OVF): 4, one per channel, in a 2×4 pin front panel connector; provide complementary ECL pulses behaving as the Digital Outputs above and indicate that the input signals have exceeded the positive full scale limit.
- Strobe Outputs (STO & ST): 4 in total; two in a 2×2 pin front panel connector (STO) providing complementary ECL pulses; two in front panel Lemo-type connectors (ST); high output impedance (current source); generate NIM level pulses when terminated in 50Ω ; produce a pulse, suitable as a strobe for subsequent logic operations, which is triggered by the strobe input and timed with the digital outputs; the width is adjustable by a front panel potentiometer (STW) in the range 5 to 25 nsec.

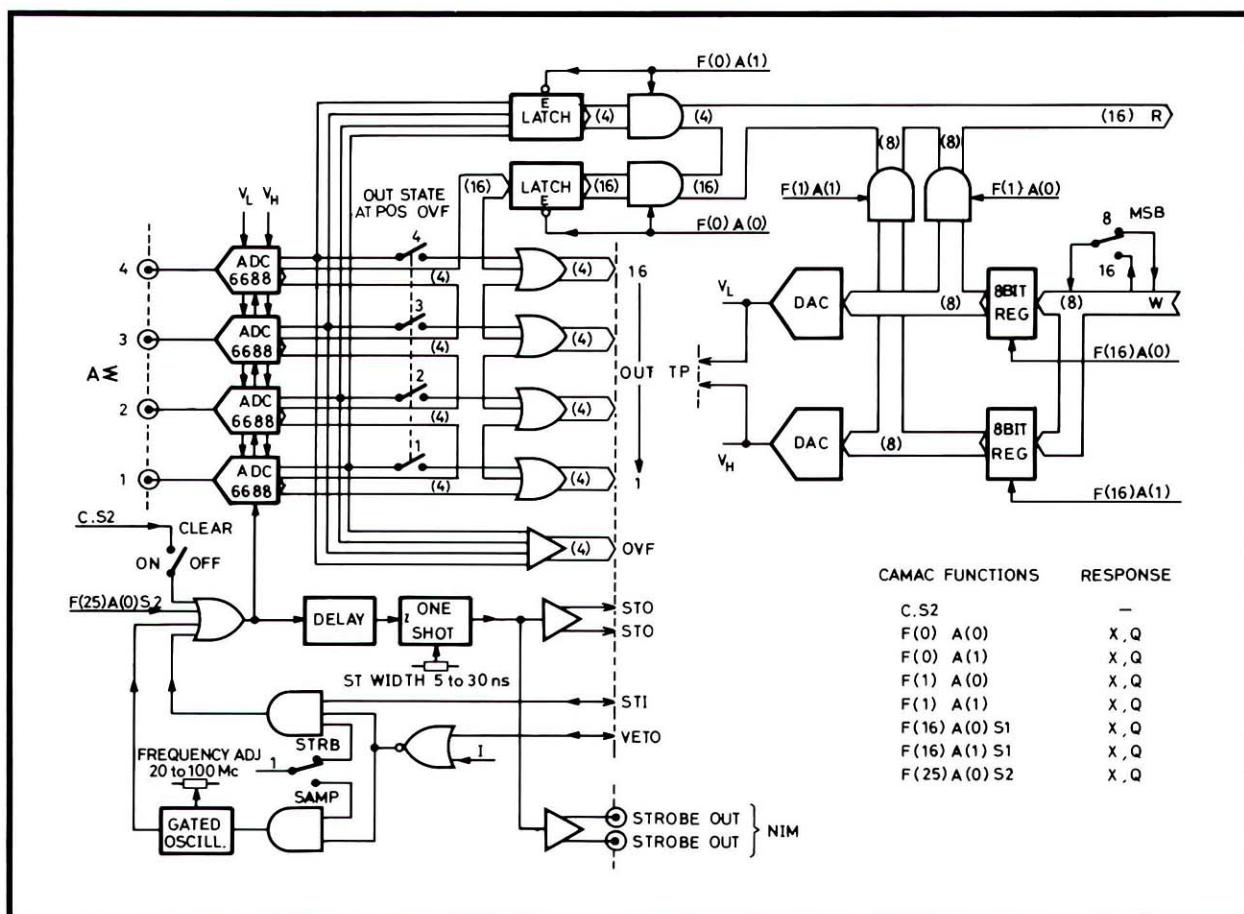
CAMAC FUNCTIONS AND COMMANDS

- C: Generates a strobe during S2 time. This function is not affected by I or VETO input and may be disabled by a side panel switch. The digital outputs will be set depending on the analog value of the inputs; in particular, if the inputs are disconnected all the digital outputs will correspond to 0 V at the inputs. The output logic state will be determined by the VL and VH reference voltages.
- I: Inhibit strobe.
- X, Q: $X = 1$ and $Q = 1$ responses are generated for any of the following functions:
- $F(0) \bullet A(0)$: Read digital outputs; R1 to R16, four bits per channel.
- $F(0) \bullet A(1)$: Read digital overflow, R1 to R4, one bit per channel.
- $F(16) \bullet A(0)$: Write Low Reference Voltage (VL) on 8 bits; range from -2550 mV to +2250 mV in steps of 20 mV.
- $F(16) \bullet A(1)$: Same as above but for the High Reference Voltage (VH).
- $F(25) \bullet A(0,1)$: Equivalent to C.

GENERAL

Test Points:	Two front panel test points allow measurements of VL and VH in a ratio 1:1; output impedance 7.5 K Ω .
Strobe Switch:	A front panel switch allows the strobe be generated either by the front panel strobe input (STRB), or by an internal free running oscillator (SAMP) whose frequency is adjustable by a front panel potentiometer (FREQ) from 20 to 100 MHz. The veto input is active in both cases.
Overflow Switch:	A side switch (OUT STATE AT OVERFLOW) allows the setting of all digital outputs to one or zero when an overflow occurs.
Clear Switch:	A side switch (CLEAR) allows the CAMAC clear function to be disabled.
Most Significant Bit:	A side switch (MSB) selects W8/R8 or W16/R16 as the MSB for data written/read from VL and VH.
Minimum ADC Resolution:	40 mV/step.
Transit Time:	Strobe (trailing edge) to digital outputs typically 15 nsec.
Current Requirements:	1.1 A at + 6 V 1.5 A at - 6 V 6 mA at + 24 V
Packaging:	Single-width CAMAC standard module.

SPECIFICATIONS SUBJECT TO CHANGE



BLOCK DIAGRAM
MODEL 4504 FLASH ADC



CAMAC ECLine Model 4508

Dual 8-Input/8-Output Fully Programmable Logic Unit

- **High density:** Two eight-input logic units in a single-width CAMAC module.
- **High input rate:** >65 MHz capability.
- **Complementary ECL inputs and outputs.**
- **Programmability of any desired logical function:** AND, OR, Inhibit, Majority, Sum, or any combinations of these functions.
- **Three different output operation modes.**
- **Constant delay:** In "shaped" and "continuous operation" mode, delay between input and output is independent from the chosen logical operation.
- **Input pattern:** Stored and available as part of the data.

The new generation of high energy physics experiments, involving extremely high counting rates and/or large detector arrays, requires a "total system" approach to instrumentation. LeCroy's new CAMAC 4000 Series of ultra-fast, high-density programmable instrumentation modules provides the solution to this requirement by allowing the experimenter to achieve full computer control of the data acquisition system within a single instrumentation standard.

LeCroy's new ECLine Model 4508, a standard CAMAC module, consists of two independent 8-input logic units, each able to perform any kind of logical operation on the eight inputs. Each section provides eight outputs. The circuit is programmable so that each output can correspond to a different logical combination of the inputs. There is no limitation on the complexity of the logical function which can be accomplished on the eight inputs. The logical configuration can be either an AND and OR, an exclusive OR, an Inhibit, a multiplicity function, or any combination of these functions as well. But the usefulness of this circuit goes much further. It finds application anywhere a logical problem exists. Other examples of useful applications are eight-bit output register (word generator), adder, colinearity, etc.

As soon as a strobe pulse arrives, the input pattern is stored on registers. These can be read and reset through normal CAMAC operations, or they can be reset by an external fast reset.

The front-panel 17-pair flat cable connectors are conveniently compatible for interconnection with LeCroy ECLine discriminators, scalers, and other logic units.

SPECIFICATIONS

CAMAC Model 4508

DUAL 8-INPUT/8-OUTPUT

FULLY PROGRAMMABLE LOGIC UNIT

INPUT CHARACTERISTICS

Number of Channels:	2, identical.
Inputs:	Eight, in a single 2 x 17 pin connector; 110 Ω input impedance (optionally high impedance available); accept differential ECL levels.
Input Width:	Minimum input pulse width or overlap to produce outputs, 10 nsec; maximum width D.C.
Maximum Rate:	>65 MHz;
Strobe Input:	One per section; Lemo-type connector; 50 Ω input impedance; a negative NIM logic pulse enables; minimum width to enable, 5 nsec; maximum frequency, >65 MHz; the strobe pulse must precede the input pulses by 2 nsec to achieve exact time coincidence; in the "shaped" or "continuous" modes (see later), a strobe pulse must always be followed by a clear pulse or by a CAMAC reset function or command.
Clear Input:	One per section; Lemo-type connector; 50 Ω input impedance; a negative NIM logic pulse clears pattern registers and resets output levels when operating in "overlap," "shaped," or "continuous" mode; minimum width to clear, 5 nsec.

OUTPUT CHARACTERISTICS

Outputs:	Eight per channel (single 2 x 17 pin connector); complementary ECL levels.
Output Width:	Depends on the output operation mode. In the "shaped" mode, the output width can be adjusted between <5 nsec and >100 nsec via a front-panel potentiometer common to each eight outputs. In the "overlap" mode, the output width is equal to the input width or coincidence overlap. In the "continuous" mode, the outputs, enabled by the strobe pulse, are frozen in their dynamic state until the next external fast clear or CAMAC reset function or command.
Syncro Output:	One per section; Lemo-type connector; high output impedance (current source). When terminated into 50 Ω , NIM levels are generated. The syncro output reproduces the strobe pulse after a constant delay of (17 \pm 1) nsec. Pulse width equals the width of the normal outputs. This output can be used, for instance, as a strobe for subsequent units or as a clear for the unit itself.

GENERAL

Strobe-Clear LED:	A front-panel LED fires in conjunction with any strobe pulse and until the next clear.
Propagation Delay:	(17 \pm 3) nsec in "overlap" mode; in "shaped" or "continuous" mode, the delay is fixed by the strobe timing; delay between strobe and output, (21 \pm 1) nsec independent of the chosen logical operation.

Operation Modes:	A front-panel switch, one per section, allows choice of one of the following three output operation modes, common to all outputs of a section: Overlap (OVL)—The output pulse width is determined by the input pulse widths (OR function) or by the input pulse overlap (for other functions). Shaped (SHP)—The output pulse, which includes an AND with the strobe pulse, is reshaped. The output pulse width is adjustable in the range 5-100 nsec through a potentiometer (one per section) on the front panel. Continuous (CNT)—The outputs, which include an AND with the strobe pulse, are frozen in their dynamic state until an external fast clear or a CAMAC C, Z, F9, or F2 occurs. This output mode is particularly convenient to avoid timing problems.
Input Pattern:	As soon as a strobe pulse is applied, the input pulse configuration is stored on registers which can be read afterwards by CAMAC. This is true for any of the output modes. This very useful facility allows an off-line reconstruction of the trigger. In order to clear the pattern registers, the strobe pulse has to be followed by a clear pulse or by a CAMAC C, Z, F9, or F2.
Logical Functions Accomplished:	Each section of the module, after suitable programming, is able to perform any kind of logical operation on the eight inputs. The eight outputs are separately programmable so that each output can correspond to a different logical operation on the inputs. Or, at the other extreme, all outputs can have the same meaning if higher fan-out is required.
Programming:	Each 4508 section contains a 256-word x 8-bit memory, which must be programmed with 256 consecutive steps to indicate which of these 256 possible configurations of the 8 inputs will give or not give an output.

CAMAC COMMANDS AND FUNCTIONS

Z or C:	The address register for the memories of both sections is set to 0; pattern registers are cleared.
X:	An X=1 response is generated for any valid CAMAC function (F) shown below.
Q:	A Q=1 response is generated for any valid CAMAC function, except when the memory addresses overflow. (This latter feature permits one to recognize when the reading or the loading of a memory has been completed.)
F0:	F0·A0, read first section 8-bit input pattern; F0·A1, read second section 8-bit input pattern; F0·A2, read first section memory content at the given address; the memory content is displayed on read lines R1-R8, the given address on read lines R9-R16. F0·A3, as before but for the second section.
F2:	F2·A0, read first section 8-bit pattern and reset at S2; reset output levels when operating in continuous mode; F2·A1, same as F2·A0, but for the second section. F2·A2, read first section memory content at the given address (as for F0·A2) and increment address by one at S2; F2·A3, same as F2·A2, but for the second section.

F9: F9·A0, clear first section pattern; reset first section output levels when operating in continuous mode; F9·A1, as above, but for the second section; F9·A2 or F9·A3, reset memory address in both sections.

F16: F16·A0, load first section memory content at the given address; data have to be sent on write lines W1-W8; F16·A1, as above, but for the second section. F16·A2, random access to the first section memory at S1 (the selected address has to be sent on write lines W9-W16); load memory content with data present on W1-W8, at the selected address, at S1. F16·A3, same as above, but for the second section.

F18: F18·A0, load first section memory content, at the given address, with data present on W1-W8, at S1; increment address by 1 at S2. F18·A1, as above, but for the second section. F18·A2 or F18·A3, load the memory's address register at S1 (this address has to be sent on write lines W9-W16).

Packaging: Single-width CAMAC standard module.

Power Requirements: = +6 V at 0.5 A; -6 V at 2.6 A.

SPECIFICATIONS SUBJECT TO CHANGE



CAMAC ECL_{line} Model 4516 16-Channel, 3-Fold Programmable Logic Unit

- **High density:** 16 channels in a single-width CAMAC module.
- **High input rate:** > 150 MHz capability.
- **100 Ω or high-impedance complementary ECL inputs:** (user-option) permit reuse of inputs in subsequent logic.
- **Complementary ECL outputs:** differentially drive flat, twisted-pair cable.
- **Programmable "AND/OR" functions:** permit all combinations of 3-fold logic.
- **Common Veto facility:** minimum width 3.5 nsec for low system deadtime.
- **Common "OR" output:** useful for fast, unrefined triggers.
- **CAMAC packaging:** higher density, better cooling, ease of remote control.

The LeCroy Model 4516 is a high-speed, multichannel 3-fold coincidence unit designed to provide the flexibility of full CAMAC system control and general-purpose logic functions to meet a wide range of coincidence requirements in modern particle physics experiments. Oriented toward large trigger logic use, the 4516 offers low cost and high density, exceptionally high speed with low complexity, and local or remote programmability of logic functions. It is designed to be directly compatible with its companion module, the LeCroy Model 4416 16-channel discriminator.

Low-Cost/High Density

The 4516 offers significant savings over conventional NIM logic units. Packaged 16 channels to a single-width CAMAC module, it not only costs less per channel, but also occupies substantially less rack space and decreases the cost of associated cabling and power supply hardware.

The high density of the 4516 is made possible by the extensive use of ECL, by the use of cable headers designed to mate with 16-channel twisted pair flat cable, and by the implementation of the CAMAC standard. Lemo connectors for the common Veto and the OR outputs are located on the rear panel to conserve front panel space. Use of the CAMAC standard permits high density by providing increased power with adequate cooling to maintain reliable operation.

High Speed/Low Complexity

With a minimum coincidence width of only 3.5 nsec, the Model 4516 is perfectly compatible with the Model 4416 discriminator and all other LeCroy ECL_{line} CAMAC modules. This permits high trigger efficiency through low system deadtime. Use of ECL logic elements permits coincidence decisions in excess of 150 MHz.

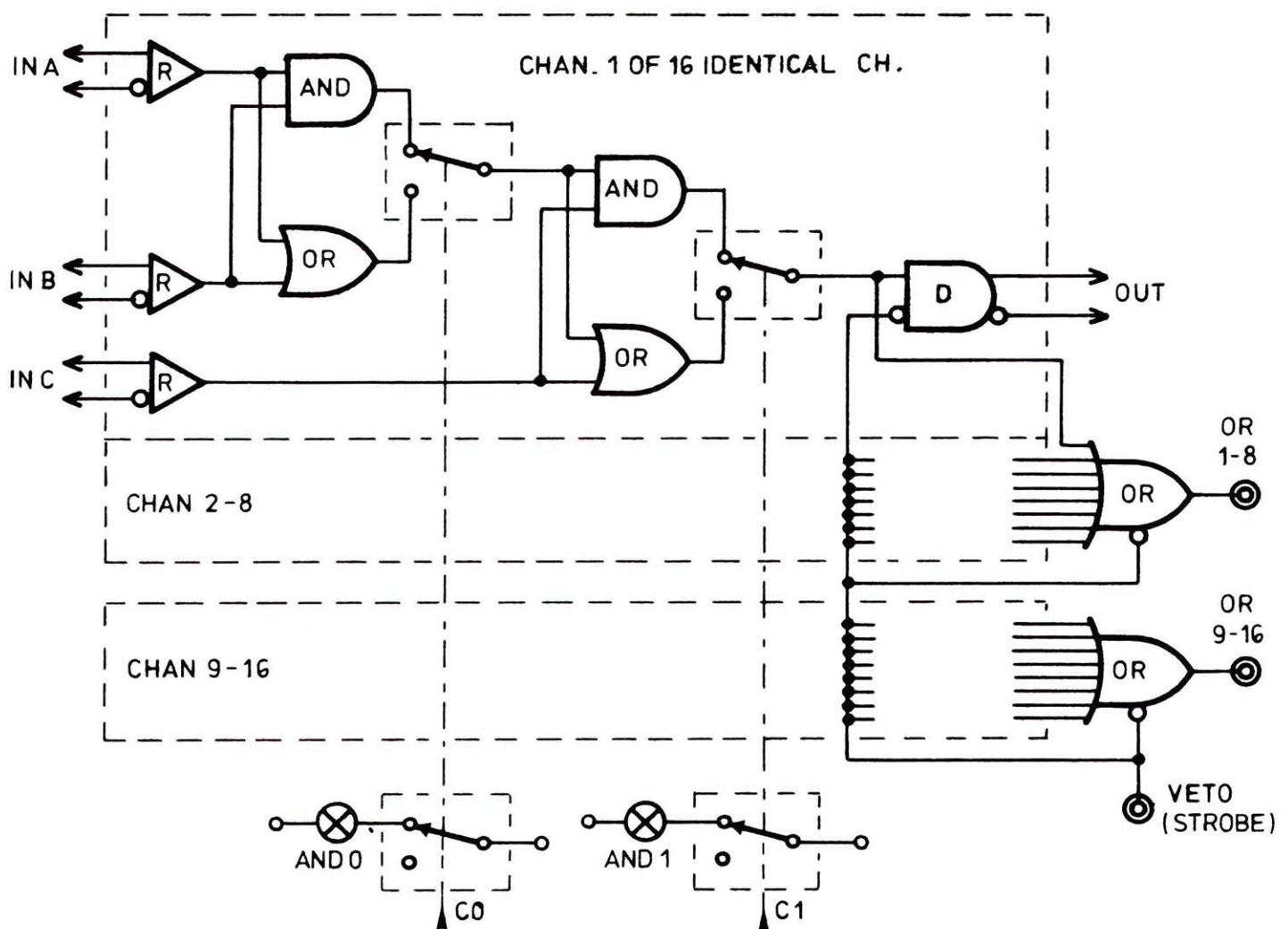
The new generation of high energy physics experiments, involving extremely high counting rates and/or large detector arrays, requires a "total system" approach to instrumentation. LeCroy's new CAMAC 4000 Series of ultra-fast, high-density programmable instrumentation modules provides the solution to this requirement by allowing the experimenter to achieve full computer control of his data acquisition system within a single instrumentation standard.

The complementary ECL outputs of each 4516 channel are designed for use with inexpensive, flat twisted-pair cables, allowing fast and accurate system interconnection. The low parts count resulting from the elimination of the usual ECL-to-NIM conversion stage yields low cost and high reliability. Output durations are equal to the coincidence overlap. Convenience of use is also made possible by ECL-level inputs, which can either receive and terminate incoming signals in $100\ \Omega$, or receive and pass on incoming signals off a high impedance for further logic or scaler use.

Local Or Remote Programmability of Logic Functions

Two rear-panel switches determine whether the 4516 is in Local or Remote Mode. In the Local Mode, manual and/or selection of logic gates 0 and 1 is made via these 2 rear-panel switches. In the Remote Mode, this selection is made via CAMAC command if the rear panel control switches are in center position (AND/REMOTE/OR). Front-panel LED's indicate the logical AND status, of C0 and C1 which are common to all channels.

The Model 4516 can be programmed to perform the functions of single 48-fold or triple 16-fold fan-in, and any combination of AND or OR logic. This ability to achieve a variety of logic functions and to redistribute the input signals via high impedance to subsequent units for other logic purposes makes the Model 4516 a convenient and generally useful component of today's demanding trigger systems.



SPECIFICATIONS

CAMAC Model 4516

16-CHANNEL, 3-FOLD PROGRAMMABLE LOGIC UNIT

INPUT CHARACTERISTICS

Number of Channels: 16, all identical.

Logic Inputs: 3, 100 Ω direct-coupled; high impedance by simple user option.
Reflections < 10% for complementary ECL signal of 2 nsec risetime.

Veto: Rear-panel connector. Permits simultaneous gating of all channels. 50 Ω;
requires NIM-level signal (> -600 mV) direct-coupled. Must overlap coincidence
of the 3 front panel inputs by a minimum of 5 nsec.

OUTPUT CHARACTERISTICS

Complementary Output: One per channel. ECL level (-0.8 and -1.6 V).
Capable of driving 100 Ω twisted-pair cable.
Duration equal to input overlap. Risetimes and falltimes 2.5 nsec into 100 Ω
termination.

OR Output: Two rear-panel connectors. Negative-going voltage output at NIM level.
Width is identical to the coincidence overlap.

CAMAC COMMANDS

X: An X-response is generated when a valid N,A,F command is recognized.

Z: Sets all channels to OR Mode.

F26·A0: Sets all C0's to AND Mode.

F24·A0: Sets all C0's to OR Mode.

F26·A1: Sets all C1's to AND Mode.

F24·A1: Sets all C1's to OR Mode.

F27·A0: Gives a Q-response if C0 switch is in AND Mode.

F27·A1: Gives a Q-response if C1 switch is in AND Mode.

GENERAL

Logic Functions: Fan-in (3 X 16-fold and 1 X 48-fold), and any combination of AND and OR
coincidence.

Maximum Rate: 150 MHz input and output.

Coincidence Width: 3.5 nsec up, determined by input pulse duration.

Double-Pulse Resolution: Less than 5 nsec at minimum input width.

Input-Output Delay:

A or B to OUT	11 nsec typical
A or B to OR	12 nsec typical
C to OUT	8 nsec typical
C to OR	9 nsec typical
Veto to OUT	8 nsec typical
Veto to OR	6 nsec typical

Power Requirements: +6 V at 50 mA
-6 V at 1.25 A

Note: As a factory option, it is possible to replace the two 1-8 and 9-16 OR outputs by two 1-16 OR outputs.

SPECIFICATIONS SUBJECT TO CHANGE



CAMAC ECLine Model 4532

32 Input Majority Logic Unit

- High channel density: 32 parallel inputs
- Majority information up to 16 hits
- Single bit or cluster mode
- 2 by 2 fast OR logic outputs
- Hit pattern CAMAC readable
- Self triggered or externally gated operation
- Provisions for multiple module cascading

The new generation of high energy physics experiments, involving extremely high counting rates and/or large detector arrays, requires a "total system" approach to instrumentation. LeCroy's new CAMAC 4000 Series of ultra-fast, high-density programmable instrumentation modules provides the solution to this requirement by allowing the experimenter to achieve full computer control of the data acquisition system within a single instrumentation standard.

The ECLine Model 4532 answers most of the majority logic problems encountered in modern High Energy Physics Experiments.

The Model 4532 calculates the multiplicity value from 32 logic channels and presents the result as a current proportional to the number of inputs up to a maximum of 16. These may be either individual inputs or clusters (i.e. adjacent inputs are counted as one input) as determined by a side switch. The multiplicity calculation can either be performed on the overlap of input pulses during a time determined by an externally applied gate (e.g. with photomultipliers), or on latched levels which are set by inputs occurring within a predetermined time window (e.g. for use with proportional chambers). In the latter mode, the analog output will increase as each pulse arrives at the inputs. The time window can be either internally generated or externally provided. The internal time window is self-triggered by the first input pulse arriving after a previous reset. A front panel potentiometer permits adjustment of the time window.

In addition to the front panel outputs, the Model 4532 also stores the input information which arrived during the time window in a CAMAC addressable 32-bit register. In both the overlap Memory Disable and latching Memory Enable modes, a front panel output provides a two by two OR of the gated inputs. The OR is performed on channels 1 and 2, 3 and 4, etc. In Overlap mode, the outputs will be pulses having a width determined by the input pulse widths, while in Latching mode the outputs will be levels set by the leading edge of the input pulses and reset by the CAMAC or front panel fast reset functions.

The Model 4532 analog output is provided on two paralleled connectors to permit the cascading of several majority units and extending the multiplicity calculation beyond 32 inputs.

The analog output is designed to be used as input to a variable threshold discriminator, or to the Model 4504 Flash ADC for conversion into a four-bit binary word.

SPECIFICATIONS

CAMAC ECLINE Model 4532

32 INPUT MAJORITY LOGIC UNIT

INPUT CHARACTERISTICS

All inputs accept differential ECL level (-0.8 V, -1.7 V) into 110 ohm input impedance (high input impedance is possible by removing socket mounted terminators).

Data Input (IN):	32 in two 34 pin front panel connectors; minimum input pulse width 6 nsec, maximum width DC.
Reset Input (RTI):	Fast reset of the input registers; generates a reset of the analog majority output and of the comparator outputs (MDO, DMO). When the analog output is cascaded with other units, the RTI only resets the contribution from the modules that received the RTI. Minimum input pulse width 6 nsec, maximum width DC. In Memory Disable mode, the RTI is inhibited.
Gate Input (GAI):	Normally open when unconnected. Normally closed when connected to a cable providing standard ECL levels. In Memory Disable mode, data pulses having an overlap with the GAI will contribute to the outputs. In Memory Enable mode, data pulses having their leading edge inside the GAI time will be accepted and stored. By deriving the GAI from the DMO, an internally generated time window is possible. Minimum overlap time width with input pulses for majority decisions, 10 nsec. Minimum overlap time width with input pulses for logical OR's, 3 nsec; maximum width DC.
Cluster Carry (CCI):	When Cluster Selection is Enabled, receives the carry information on the cluster from the Cluster Carry Output (CCO) of any adjacent majority logic unit.
Analog Majority Input/Output (AMIO):	Two bridged front panel Lemo type connectors; high impedance current source; generates a current proportional to the input multiplicity at the rate of 3.2 mA per hit (or 80 mV per hit into 25 ohms). The AMIO connectors can be used for daisy chaining of analog majority information within a group of similar units. Transit time between AMIO connectors 2 nsec. Unused output must be terminated with 50 ohms.

OUTPUT CHARACTERISTICS

All logic outputs provide complementary ECL levels (-0.8 V, -1.7 V) and are capable of driving differential 110 ohm loads.

Data Outputs (OUT):	16 in a 34 pin front panel connector. Each output corresponds to the logical OR of two channels (respectively, 1 and 2, 3 and 4, ..., 31 and 32). In Memory Disable mode, provides pulses corresponding to an overlap coincidence between the gate pulse and the data inputs. In Memory Enable mode, provides levels started by the coincidence between the gate pulse and the leading edge of the data pulses.
OR Output (ORO):	Provides the logical OR of the 32 channels, otherwise, behaves as data outputs.
Strobe Output (STO):	Provides a pulse, suitable for strobing of subsequent logic units, at the end of the gate input and delayed by the internal transit time (6 nsec). Width adjustable from 10 to 25 nsec by a trimmer (STROBE WIDTH) accessible from the side of the module.
Majority Discriminated Output (MDO):	The AMIO input/output is internally used as input to an adjustable threshold comparator providing the MDO output. Threshold adjustable from 1 to 16 hits by a front panel potentiometer (MA THR). The output will be a pulse or a level depending on the selected operating mode.
Delayed Majority Output (DMO):	Reproduces the output MDO above, after an adjustable delay. A switch on the side of the module (DM RANGE) selects one of two delay ranges; 10-100 nsec or 50-1000 nsec. A front panel potentiometer (DMO DELAY RANGE) permits continuous adjustment. The DMO is cleared as soon as the MDO is cleared.
Cluster Carry (CCO):	When Cluster Selection is Enabled, indicates that Output channel 32 was hit for use in conjunction with channel 1 of a logically adjacent cluster logic in another 4532 module (CCI input).

CAMAC COMMANDS

Z, C

Clears data memory and LAM at S2 time.

L	A Look-At-Me signal is generated (in Memory Enable mode only) at the end of the gate input if the OR output is set. The LAM may be enabled or disabled by the LAM enable switch accessible on the side of the module.
X	An X = 1 response is generated for any executable function.
Q	A Q = 1 response is generated for any executable function in Memory Enable mode only.
F(0)•A(0), A(1)	Read input pattern. A(0): channels 1 to 16, A(1): channels 17 to 32. A Q response is generated in Memory Enable mode only.
F(1)•A(0)	Read status register: R1 = 1 if LAM is ON R2 = 1 if LAM Enable switch is ON R3 = 1 if MEMORY Enable switch is ON R4 = 1 if CLUSTER Enable switch is ON Q response is always generated.
F(2)•A(0)	Read input pattern, channels 1 to 16. Q response is generated in Memory Enable mode only.
F(2)•A(1)	Read input pattern, channels 17 to 32, and clears the 32 channel data memory and LAM at S2. Q response is generated in Memory Enable mode only.
F(8)•A(0)	Test LAM; a Q response is generated if L is ON.
F(9)•A(0)	Clears the data memory and LAM at S2. Q response is generated in Memory Enable mode only.
F(10)•A(0)	Test and clear LAM, clears LAM at S2 time. Q response is generated if L is ON. The clear LAM operation is not executed if Q response is missing.

GENERAL

Mode Selection:

A Memory Enable switch, accessible on the side of the module, selects one of the following modes:

Memory Disable:

Functions are disabled; the multiplicity calculation is performed on the overlap of the data inputs.

Memory Enable

The data inputs are latched; the multiplicity is determined by the number of leading edges of data input pulses occurring during the gate time. In this mode the unit needs to be cleared either by the reset input (RTI) or by a resetting function.

Cluster Selection:

The Cluster Enable switch, accessible on the side of the module, determines one of the two following modes:

Cluster Disable:

Each data input provides one hit on the Analog Majority Output AMIO; the Cluster Carry Input (CCI) is disabled;

Cluster Enable:

Any group of adjacent input data pulses will be considered as a single hit.

Provision has been made for the clusters to extend beyond the 32 inputs. If an input is present on the logically adjacent channel to input 1 of this unit but is located in another unit, the CCI can be used to indicate its presence. The CCO of this module indicates that channel 32 of this module is present.

Transit Times:

Data IN to AMIO	16 nsec
AMIO to MDO output	5 nsec
End of gate IN to Strobe OUT	6 nsec
Data IN to Data OUT	12 nsec
Data IN to OR OUT	16 nsec
Reset IN to Data OUT	20 nsec
Reset IN to OR OUT	24 nsec
Data IN 32 to Cluster Carry OUT	11 nsec
Cluster Carry IN to Data IN 1	2 nsec

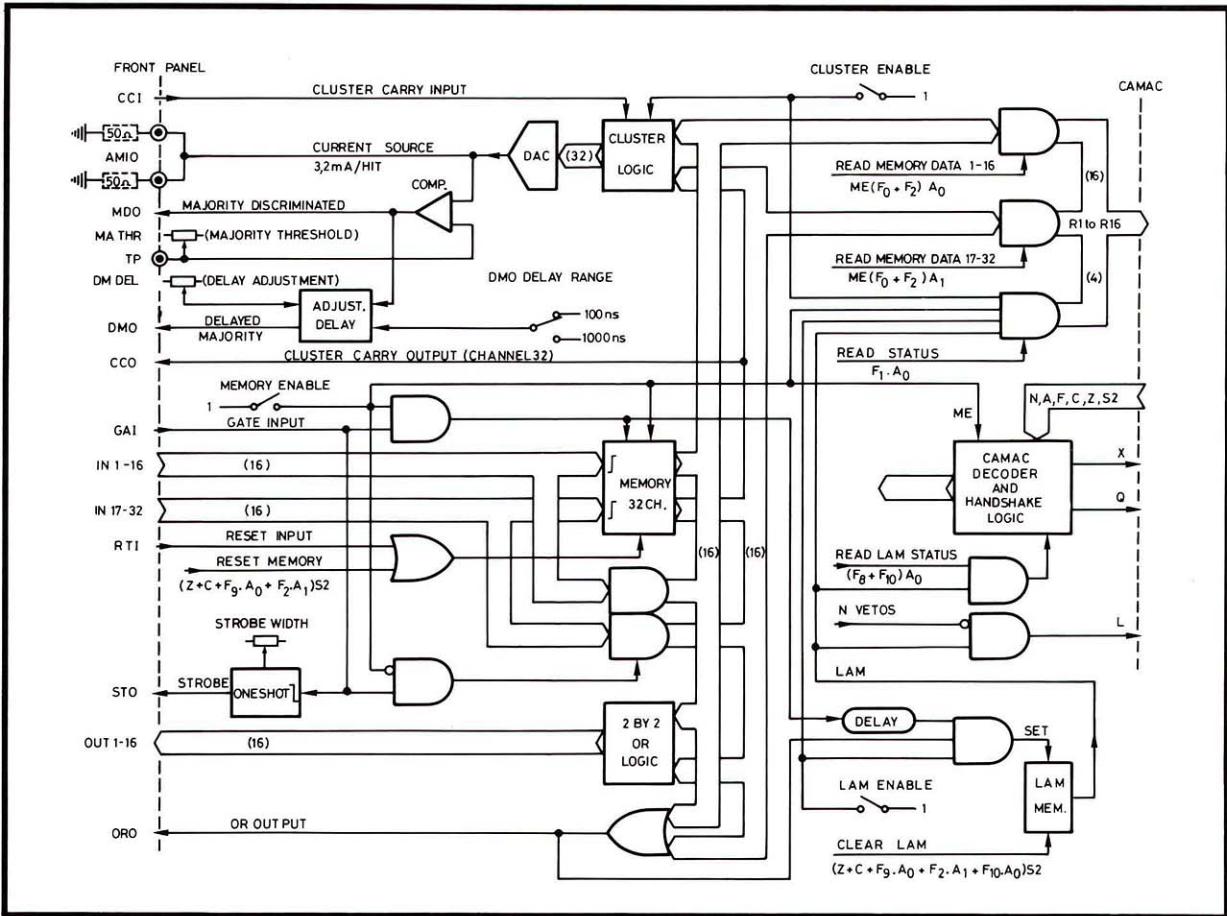
Gate pulse must precede Data pulse by at least 7 nsec.

Current Requirements:

- + 6 V at 200 mA
- 6 V at < 3.6 A (3 A when empty)
- + 24 V at 5 mA
- 24 V at 7 mA

Packaging:

Single-width standard CAMAC module.



BLOCK DIAGRAM MODEL 4532 MAJORITY LOGIC UNIT

SPECIFICATIONS SUBJECT TO CHANGE



CAMAC ECLINE Model 4564

16 to 64 Fold OR Logic Unit

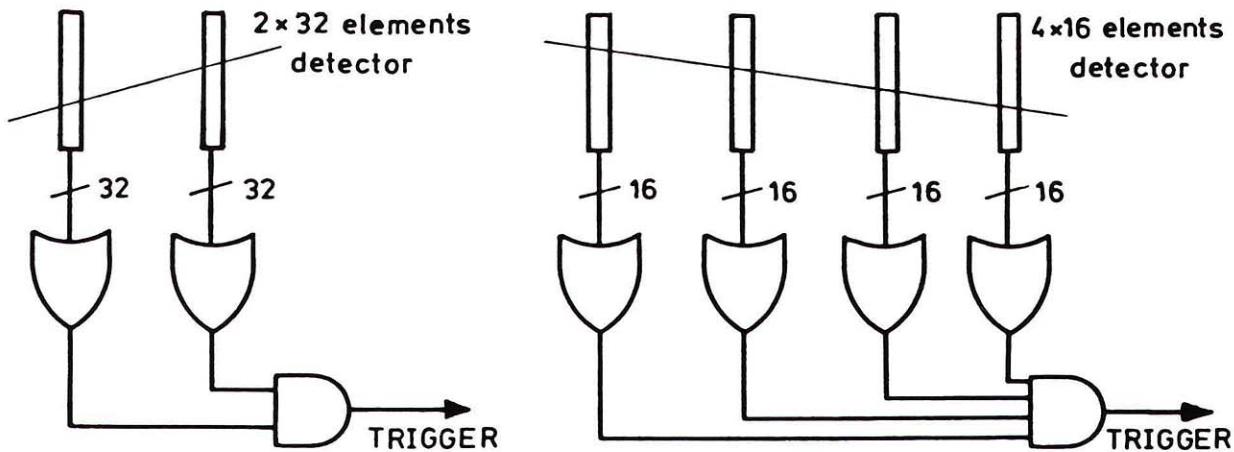
- **High Density:** 64 inputs.
- **Several OR Combinations:** 4×16 ; 2×32 ; 1×64 .
- **Constant Transit Time**
- **AND/OR Logic Functions:** all available simultaneously on the back panel.
- **4 Discriminator/Shaper Out:** jumper selectable.

The new generation of high energy physics experiments, involving extremely high counting rates and/or large detector arrays, requires a "total system" approach to instrumentation. LeCroy's new CAMAC 4000 Series of ultra-fast, high-density programmable instrumentation modules provides the solution to this requirement by allowing the experimenter to achieve full computer control of his data acquisition system within a single instrumentation standard.

The LeCroy Model 4564 is a simple and useful logic unit. It consists of four times 16 input OR's followed by a set of additional 2-fold and 4-fold OR and AND functions. The logic diagram on the back of this page, shows the internal architecture of the module. All the outputs are provided on a rear panel connector.

This CAMAC module provides a general purpose OR facility for inputs grouped in units of 16. It is especially useful with LeCroy ECLINE 16 Channel Discriminators. All logic connections follow the ECLINE Standard and use low cost multiconnector flat or twisted pair cable and connectors.

The following example illustrates a typical application for the Model 4564. A telescope of beam chambers or hodoscopes is shown and the Model 4564 performs a simple track or pattern recognition.



December 1982

SPECIFICATIONS

CAMAC ECLine Model 4564

16 TO 64 FOLD OR LOGIC UNIT

INPUT CHARACTERISTICS

Signal Inputs:

64 in four 2×17 pin front panel connectors; all inputs accept differential ECL levels; impedance: 110 ohms; minimum input pulse width 6 nsec maximum width DC; maximum input frequency > 100 MHz.

OUTPUT CHARACTERISTICS

Overlap Outputs:

Rear panel 2×17 pin connector, out 1 to 12; generate differential ECL levels; the output pulse width corresponds to the input pulse overlap (± 2 nsec for the desired logic combination. See logic diagram below for pin allocation to the different logic functions; minimum output width 5 nsec; maximum width DC maximum overlap output frequency > 100 MHz; transit time 12 nsec ± 1 nsec independent from the logic function.

Shaped Outputs:

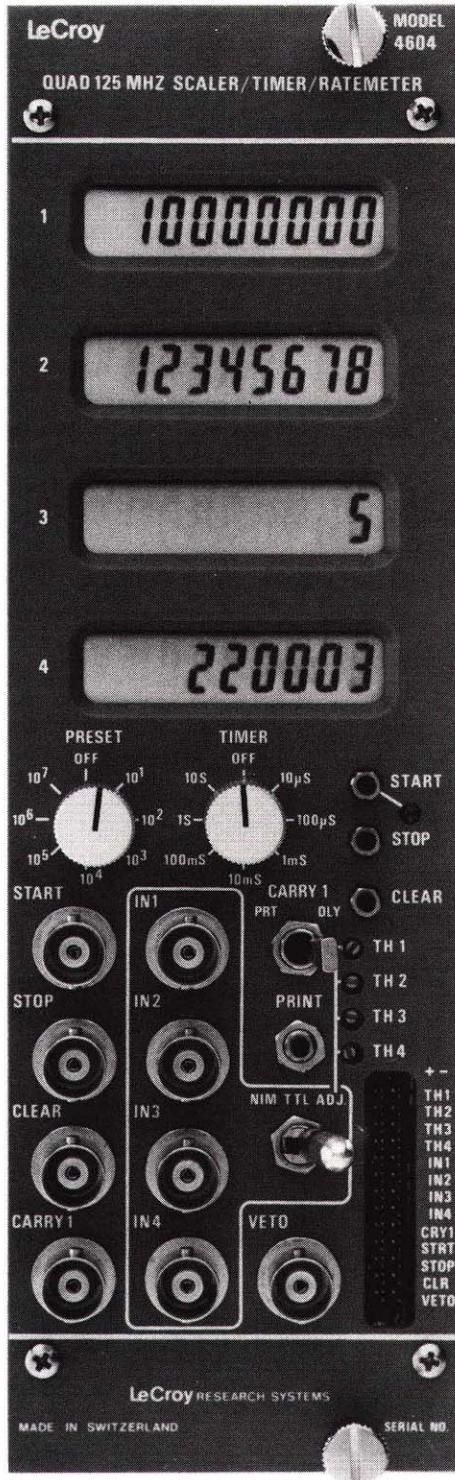
Rear panel connector, out 13 to 16; any of the overlap logic combinations can be connected, via jumper option to any of the four discriminator/shaper included in the unit; these four shaped outputs provide differential ECL levels and the output width is internally adjustable from 15 to 500 nsec; maximum frequency: 50 MHz; double pulse resolution 13 nsec.

NOTE: An option, where all rear panel multipin connector output are at NIM levels, can be provided upon request.

SPECIFICATIONS SUBJECT TO CHANGE

LOGIC DIAGRAM

INPUTS	OUTPUT CONNECTOR PIN #	LOGIC FUNCTION
16	1	A
16	2	B
16	3	C
16	4	D
16	5	A·B
16	6	C·D
16	7	A·B
16	8	C·D
16	9	A·B·C·D
16	10	A·B·C·D
16	11	(A·B)·(C·D)
16	12	A·B·C·D



NIM Model 4604

Quad 125 MHz Scaler / Timer / Ratemeter

- Four channels in a double width NIM module.
- 125 MHz operation.
- Large, easy-to-read 8 digit Liquid Crystal Displays.
- Accepts NIM, TTL, differential ECL or analog input signals.
- Choice of manual operation or remote control via NIM, TTL, or differential ECL signals.

The LeCroy Model 4604 is a general purpose Scaler, Timer and Ratemeter designed for test and measurement applications as well as experimental or industrial monitoring. This flexible four-channel unit may be used as a 125 MHz Scaler or multi-time base Timer with or without preset stop. The module features front panel push buttons or remote-controlled operation.

The large, 8 digit Liquid Crystal Displays with leading zero suppression, provide easy-to-read visual indications of the individual channel contents. To avoid complicated external level conversions, all scaler inputs accept NIM, TTL, differential ECL, or analog signals. For the latter choice, individual threshold levels may be adjusted between -1.5 V and +1.5 V.

Start, Stop and Clear actions may be executed either by front panel push buttons, or by external NIM, TTL or differential ECL signals. An external veto pulse may also be applied to inhibit counting for gated operation.

For both the Preset Scaler and Timer operations, the maximum content of the first channel may be preset via a front panel rotary switch from 10^1 to 10^7 counts. A carry pulse is generated upon overflow of the preset or of the scaler capacity, and counting may be stopped in all channels. The first channel may either count external pulses (scaler) or an internal crystal controlled clock (timer). When used as a timer, the time base may be set from 10 μsec to 10 sec via a front panel rotary switch.

Simple front panel connections transform the Model 4604 into a ratemeter.

SPECIFICATIONS

NIM Model 4604

QUAD 125 MHz SCALER / TIMER / RATEMETER

INPUT CHARACTERISTICS

Signal

(IN_i, i = 1,...,4):

Four channels; two front panel DC coupled inputs per channel; one BNC connector, accepts TTL, NIM or analog single ended signals, switch selectable; the input impedance, factory set at 50 Ω, may be changed to high impedance via an internal jumper option; one two-pin connector, 100 Ω input impedance, accepts differential ECL signals.

Minimum input pulse width, 4 nsec; maximum frequency, 125 MHz.

Start, Stop, Clear, Veto:

Two front panel connectors per function; one BNC connector (START, STOP, CLEAR, VETO) accepts NIM level (< -600 mV) or TTL level (> +1.5 V) signals; an internal jumper option selects 50 Ω or high input impedance; one two-pin connector (STRT, STOP, CLR, VETO), 100 Ω input impedance, accepts differential ECL signals; minimum pulse width for all signals, 10 nsec; a front panel LED is lit in response to a Start action; the Veto input is active for both scaler and timer operation modes. For safe operation, a Clear command is effective only when the scaler is stopped.

OUTPUT CHARACTERISTICS

Carry:

Two front panel connectors; one BNC connector (CARRY1), high output impedance (current source), generates NIM levels when terminated with 50 Ω; one two-pin connector (CRY1), generates differential ECL levels suitable for driving 100 Ω twisted pair cables; a carry signal is generated when Channel One overflows the scaler capacity. (See also CARRY switch).

GENERAL

START, STOP,

CLEAR Push Buttons:

Front panel push buttons generate the Start, Stop and Clear actions; a front panel LED is lit in response to a Start action.

PRINT Push Button:

The Model 4604 is equipped with an interface to the RS232 bus for connection to a printer; pushing the PRINT button sends the scaler contents to the RS232 bus rear panel connector.

NIM/TTL/ADJ Switch:

Front panel, three position switch; selects the signals accepted by the four scaler inputs:
NIM: accepts NIM levels (< -600 mV);
TTL: accepts TTL levels (> +1.5 V);
ADJ: accepts analog pulses; thresholds individually adjustable for each channel via front panel potentiometers (TH_i, i = 1,...,4); threshold range -1.5 V to +1.5 V; threshold precision ± 20 mV; 1:1 threshold monitor on the front panel.

PRESET Switch:

Front panel, 8 position rotary switch; permits preset selection of value 10ⁿ, n ranging from 1 to 7; this value will act as the preset value for Channel One both in scaler and timer operations modes; when the preset value is reached by Channel One, a carry output signal is generated and all four channels are stopped. When in OFF position, Channel One will be free-running.

TIMER Switch:

Front panel, 8 position rotary switch; selects the time base of the timer as 10 μsec, 100 μsec, 1 msec, 10 msec, 100 msec, 1 sec, or 10 sec; Channel one is used to count the time intervals. When in OFF position, Channel One will act as a normal scaler, accepting signals from the front panel input IN₁.

CARRY Switch:

Front panel two position switch.

In the PRT (PRompT) position, the carry signals are generated promptly after the overflow condition is detected. For scaler overflow, a 20 nsec pulse is generated. Under preset conditions, a level is generated which must be reset by the Clear signal.

The DLY (DeDelay) position is used when the Model 4604 functions as a ratemeter. The 30 nsec wide carry pulses are generated approximately 2 seconds after the overflow condition is detected. By connecting the CRY1 ECL output to the CLR ECL input and the CARRY1 NIM output to the START NIM input, the preset value stops the scalers, the results are displayed for 2 seconds, and the unit automatically is cleared and restarted.

Packaging:

RF-shielded, standard #2 width NIM module.

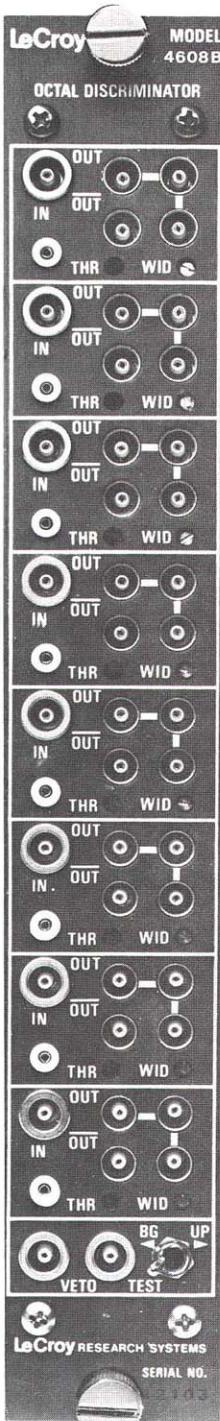
Power requirements:

2.0 A at +6 V; 1.5 A at -6 V; 200 mA at +12 V; 200 mA at -12 V.

SPECIFICATIONS SUBJECT TO CHANGE

TECHNICAL DATA

LeCroy



NIM Model 4608B

Octal 150 MHz Updating Discriminator

- High counting rate
- High density
- High fan-out
- Low threshold
- Burst Guard mode
- Fast veto
- Built-in test feature

The Model 4608B is a high performance, 8 channel leading edge discriminator featuring high sensitivity, high speed, and updating or Burst Guard mode. A common inhibit adds to the versatility of the Model 4608B, which may be used as an enable for pulsed-mode applications. A built-in test feature simulates an input signal for each channel upon receipt of a NIM level signal applied to a Lemo type front panel test input connector. This permits rapid, simultaneous testing of all discriminator channels.

The minimum threshold of the Model 4608B is -30 mV , variable up to -900 mV via front panel screwdriver adjustment. A monitor point is provided to permit measurement of the threshold level with a voltmeter rather than the more difficult and less precise analog measurement via oscilloscope, assuring accurate results even in varied operating environments. Because of the extremely low reflections from its input (4%), the Model 4608B is significantly better protected against the multiple pulsing due to reflections.

The Model 4608B operates at maximum rates of 150 MHz. Its updating design permits retriggering even while an output from a previous input is still present. The Model 4608B will respond to a second pulse within 5 nsec of the leading edge of the first pulse. Propagation delay through the Model 4608B is approximately 12 nsec.

In the Burst Guard mode (front panel switch selected), the output pulse duration is equal to the input pulse time over threshold or the preset output width, whichever is larger. In case of very high frequency bursts (above 500 MHz), the output will be true from the leading edge of the first pulse to the trailing edge of the last pulse in the burst.

The outputs of the Model 4608B are high impedance -48 mA current switching stages, providing output levels of -800 mV into three 50Ω loads. Unused outputs need not be terminated; the maximum output swing is amplitude limited to -1.2 V for a single output load. The single complementary output provides -16 mA (-800 mV into 50Ω) in the quiescent state. The output durations may be independently set via front panel screwdriver adjustment from 3 nsec to 40 nsec. Up to 100 nsec output width is possible with the restriction that input and output pulse widths cannot be equal. Output risetimes and falltimes are less than 2 nsec.

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SPECIFICATIONS

NIM Model 4608B

OCTAL 150 MHz UPDATING DISCRIMINATOR

INPUT CHARACTERISTICS

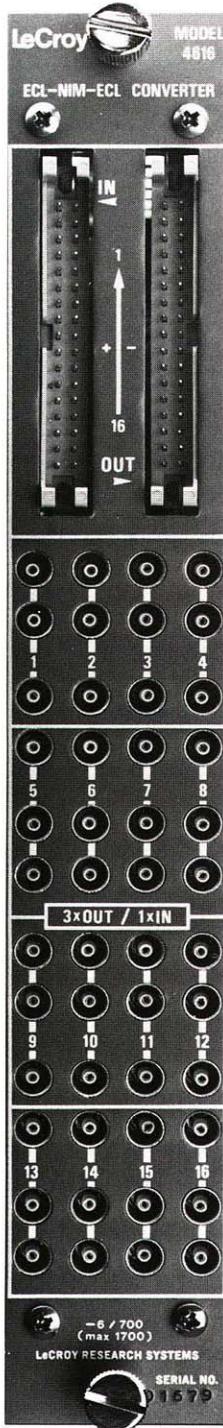
- Signal Inputs: 8, Lemo type front panel connectors, $50 \Omega \pm 2\%$ protected to ± 5 A for $0.5 \mu\text{sec}$ clamping at +1 and -6 volts.
Reflections <4% for input pulses of 2 nsec risetime.
Stability better than $0.25\%/\text{ }^\circ\text{C}$ over $20\text{ }^\circ\text{C}$ to $60\text{ }^\circ\text{C}$ operating range.
Offset ± 1 mV to -900 mV.
Threshold, -30 mV to -900 mV $\pm 5\%$; front panel screwdriver adjustable.
Threshold, monitor point on front panel has 10:1 ratio of monitor voltage to actual voltage $\pm 5\%$.
Hysteresis, typical 6 mV.
- Test Input: 1, Lemo type connector on the front panel, $50 \Omega \pm 2\%$, triggers all channels.
Requires NIM level direct coupled signal (> -600 mV).
Minimum width: 3.5 nsec.
Maximum rate: 150 MHz.
- Veto Input: 1, Lemo type front panel connector, $50 \Omega \pm 2\%$, permits simultaneous fast inhibiting of all channels; requires NIM level signal (> -600 mV).
Direct coupled.
Must precede input signal by approximately 3.5 nsec and overlap its leading edge in update mode or overlap complete input signal in Burst Guard mode.
Minimum duration: 4 nsec.

OUTPUT CHARACTERISTICS

- Negative Outputs: 3, 0 mA quiescently, -50 mA ± 6 mA during output, -800 mV into three 50Ω loads. Amplitude limited to -1.2 V.
Duration, 3 nsec to 40 nsec. 100 nsec output duration possible with the restriction that input and output pulse width cannot be equal.
Risetimes and falltimes less than 2 nsec.
Width stability better than $0.2\%/\text{ }^\circ\text{C}$ max.
- Complementary Output: 1, -16 mA ± 2 mA quiescently, 0 mA during output. Duration, risetimes, falltimes, and width stability specifications are identical to those of negative outputs.

GENERAL

- Maximum Rate: 150 MHz.
- Double Pulse Resolution: Typical, 5 nsec.
- Time Slewing: 500 psec for input amplitudes from 2 times to 20 times over threshold.
- Input-Output Delay: < 12 nsec.
- Test Output Delay: < 14 nsec.
- Multiple Pulsing: None, one and only one output pulse is produced for each input pulse regardless of input pulse amplitude and duration.
- Burst Guard: A front panel switch enables the Burst Guard operation for all channels.
- Power Requirements: 40 mA at +6 V
1.9 A at -6 V
150 mA at -12 V
40 mA at +24 V
25 mA at -24 V

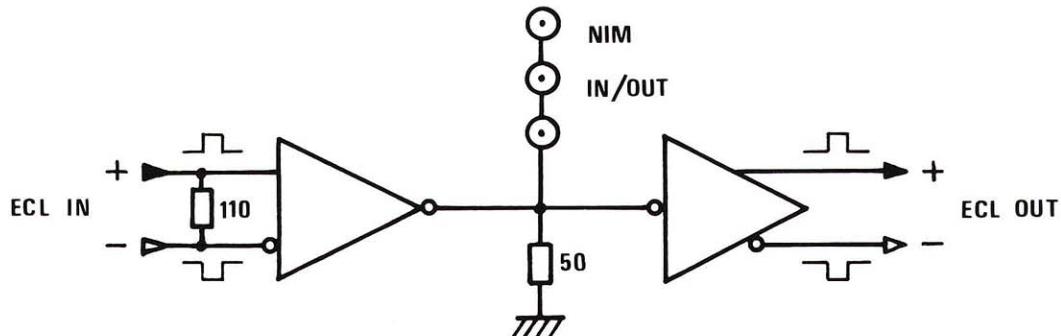


NIM Model 4616

16-Channel ECL/NIM/ECL Converter

- **High density:** 16 channels in a single-width NIM module.
- **ECLline full compatibility:** directly interfaceable with other ECLline circuits.
- **ECL/NIM/ECL in each channel:** each channel serves both for ECL-to-NIM as for NIM-to-ECL conversion.
- **Fan-out capability:** three NIM outputs and one ECL output per channel.
- **Low standby power consumption.**
- **High working frequency:** up to 150 MHz.
- **DC coupled.**

The Model 4616 is simultaneously an ECL-to-NIM and a NIM-to-ECL converter, specially designed to fill the gap between the new growing ECL circuitry and the old NIM electronics. The Model 4616 is designed so that each channel can be used for both applications. When ECL complementary pulses have to be converted, the circuit provides three NIM outputs and an additional ECL output. When a NIM pulse has to be converted, it is sent in one of the NM outputs (now used as an input) while the other two NIM outputs are unconnected. Thus, the circuit provides a single complementary ECL output. The accompanying diagram shows the basic circuit configuration of one channel.



March 1980

SPECIFICATIONS

NIM Model 4616

16-CHANNEL ECL/NIM/ECL CONVERTER

INPUT CHARACTERISTICS

- ECL Inputs: 16, one per section, in a 2 x 17 pin connector; accept complementary ECL levels; typical threshold 200 mV.
- NIM Inputs: 16, one per section, Lemo-type connector, to be chosen out of the three Lemo-type connectors in the channel; the other two have to be kept unconnected; input impedance $50 \Omega \pm 5\%$; reflections <10% for input risetimes >2 nsec.

OUTPUT CHARACTERISTICS

- ECL Outputs: 16, one per section, in a 2 x 17 pin connector; ECL complementary levels (-0.8 V and -1.7 V); risetime 2 nsec typical.
- NIM Outputs: 48, three bridged outputs per section, Lemo-type connectors; quiescently at 0 mV, >-700 mV into 3 x 50Ω loads, max. -1.2 V into 1 x 50Ω load, during output; risetime 2 nsec typical.

GENERAL

- Maximum Frequency: 150 MHz.
- Minimum Pulse Width ECL and NIM inputs/outputs 4 nsec.
- Transit Times: ECL input to NIM output <6 nsec.
ECL input to ECL output <10.5 nsec.
NIM input to ECL output <6.5 nsec.
- Power Requirements: -6 V quiescently at 700 mA, with all loads connected and all channels activated
max. 1.7 A.

SPECIFICATIONS SUBJECT TO CHANGE

CAMAC Series 4800 CAMAC Boosters (CAB)

Fast Programmable CAMAC Processors

- **16-bit bipolar processor:** 4 AM2901 bit slices provide multi-operand instructions.
- **Fast basic cycle time for all instructions:** operates at 5 MHz.
- **16-bit × 16-bit Multiplier/Accumulator and 16-bit Shifter:** both operate in 200 nsec.
- **4 K 24-bit Instruction Memory for Programs.**
- **4 K 16-bit Data Memory:** expandable by external memory units to an additional 64 K 16-bit words.
- **4 Models to choose from:** permits optimum design of the CAMAC readout and processing architecture for each application.

The LeCroy Series 4800 CAMAC Boosters (CAB) are a family of CAMAC Programmable Processors designed to distribute programmable intelligence within a CAMAC data acquisition system*. They represent a significant advance in data collection and handling in terms of system architecture, speed, flexibility, and real time processing power within the world-wide laboratory grade CAMAC System.

The evolution of larger and more complex experimental situations in Nuclear and Elementary Particle Physics, coupled with the growth of Real Time Industrial and Clinical applications, has forced a parallel evolution in data acquisition techniques. The Series 4800 CAB brings a new level of sophistication and performance to the idea of distributing programmable intelligence within the CAMAC system itself to meet these needs.

The speed of the CAB coupled with its extremely powerful instruction set permits performance of real time processing within the 1 μsec CAMAC cycle itself. The LeCroy flexible implementation of the CAB philosophy has resulted in a system permitting the insertion of this potential at virtually any point in the data acquisition chain.

CAB MODEL OPTIONS

The CAB is available in four models permitting either classic CAMAC systems or tree/parallel architectures with programmable intelligence located at each node. These options are described on the following pages and include:

1. The Model 4801 CAB C, a programmable CAMAC Crate Controller.
2. The Model 4802 CAB G, a programmable CAMAC Crate Controller that interfaces to the main data acquisition system through the IEEE-488 Bus (GPIB).
3. The Model 4804 CAB CG, a programmable CAMAC Crate Controller with an auxiliary GPIB Port.
4. The Model 4805 CAB BG, a Camac Branch Driver with an auxiliary GPIB Port.

*Initial development by LPNHE/Ecole Polytechnique Palaiseau, Paris.

CAB HARDWARE

The CAB family is designed around 4 AM2901 bit slice processors and the AM2910 Sequencer. The 16-bit bipolar processor runs at 5 MHz and is complemented by a 16-bit by 16-bit multiplier that also has a 200 nsec cycle time. The 4 K by 24-bit RAM instruction memory is separate from the 4 K by 16-bit RAM data memory. The data memory may be expanded by an additional 64 K words with up to 4 companion, 16 K Fast Triple Port Memory modules, the LeCroy Model 4302.

In addition to the data acquisition ports, each CAB has 3 NIM level inputs as well as 3 outputs for optional synchronization and external triggering.

CAB SOFTWARE

The Series 4800 CABs do not support internal software for editing, compiling and linking programs. They may have a simple on-board monitor for supervising the running programs. However, all support activities must be run on a host computer.

CABs are presently running under a wide range of hosts including computers manufactured by Digital Equipment Corporation, Hewlett Packard, Norsk Data, Control Data, and LeCroy Research Systems.

Each CAB is delivered with complete source code written in FORTRAN including Cross Assembler and Dynamic Debugger. In addition, test programs, sample programs, and a CAMAC Type A Crate Controller emulation program, written in CAB native code, are included.

APPLICATIONS

I. Classic CAMAC System with Data Preprocessing

A Model 4801 CAB C in a classic CAMAC system is shown in Figure 1. The CAB C resides on the standard CAMAC Branch Highway and controls its crate. Communication with the modules in the crate is via the crate's CAMAC Dataway and is limited to 1 μ sec per word. Data may be formatted, compressed, combined, and filtered by the CAB processor.

The CAB may perform up to 4 additional instructions between the 1 μ sec CAMAC reads or writes. For example, it could test on the Q response and, if present, update a memory location pointer. The data could have an offset or pedestal subtracted, or could be multiplied by a calibration constant and stored in Data Memory. This real time processing of the data would not compromise the readout speed of the system.

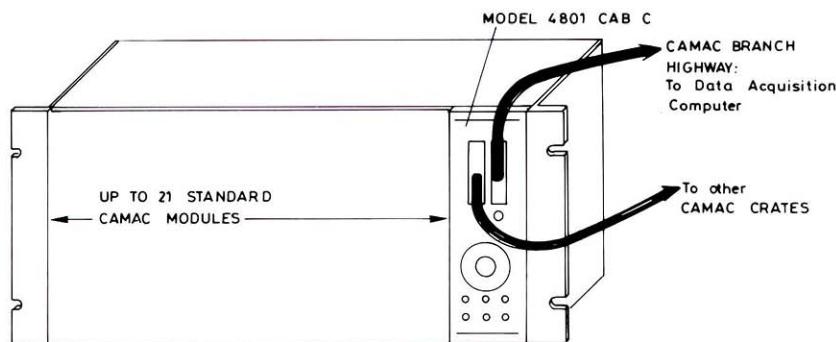


Figure 1

II. Fast Readout of the CAMAC Crate

A faster readout scheme is shown in Figure 2. A CAB C controls the operation of a crate full of LeCroy Model 4300, 16-Channel Fast Encoding and Readout ADC (FERA) modules, via the Dataway. The data readout of the units is by the memory extension module of the CAB, the Model 4302 Fast Triple Port Memory. This 16 K, 16-bit, 100 nsec memory unit has separate ports to the CAMAC Dataway and the CAB's internal busses.

Data may be entered via the front panel ECL port at a rate of 100 nsec per word. An entire crate of ADCs (over 300 channels) may be read out in about 30 μ sec. If the experiment uses the pedestal subtraction and data suppression options of the Model 4300 FERAs, this readout time may be further reduced. The data memory is sufficiently large that many events may be read out from several crates of front-end electronics and held in the Model 4302 memories. Data may then be processed asynchronously by the CAB and the compressed and processed data passed to the main data acquisition system.

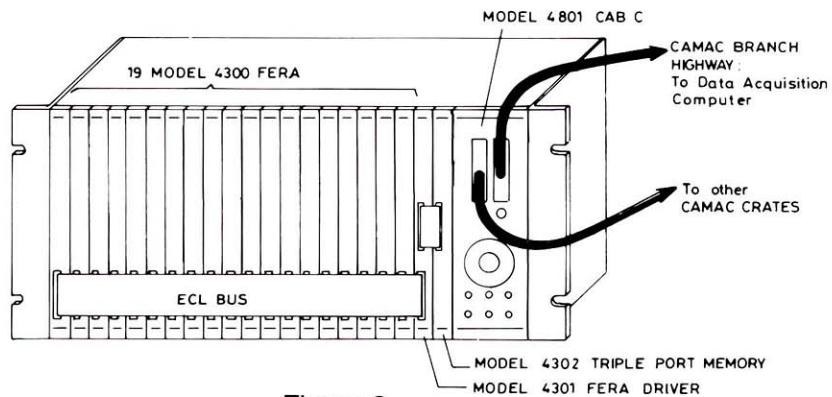


Figure 2

III. Personal Computer Data Acquisition

In Figure 3, a personal computer, such as a Hewlett Packard, Sage or Cromemco, is connected to a LeCroy Model 4802 CAB G via the GPIB (IEEE-488). The result is a CAMAC data acquisition system with all the advantages of CAMAC (hundreds of available data acquisition and control modules; 1 MHz parallel readout of these modules via the Dataway; standard power supply and crates; simple, user designed and constructed custom modules, etc.) and preprocessor powerful enough to perform data reduction, filtering, formating, etc.

This powerful, flexible, sophisticated data acquisition system is under the control of a relatively inexpensive personal computer. The personal computer handles the software maintenance for the CAB and stores the data on its own removable storage device such as floppy disks or streamer tapes. The CAB deals with the real time data acquisition and experiment control and performs the processing at a speed no personal computer could ever approach. In order to use the LeCroy software, the personal computer must be capable of running FORTRAN.

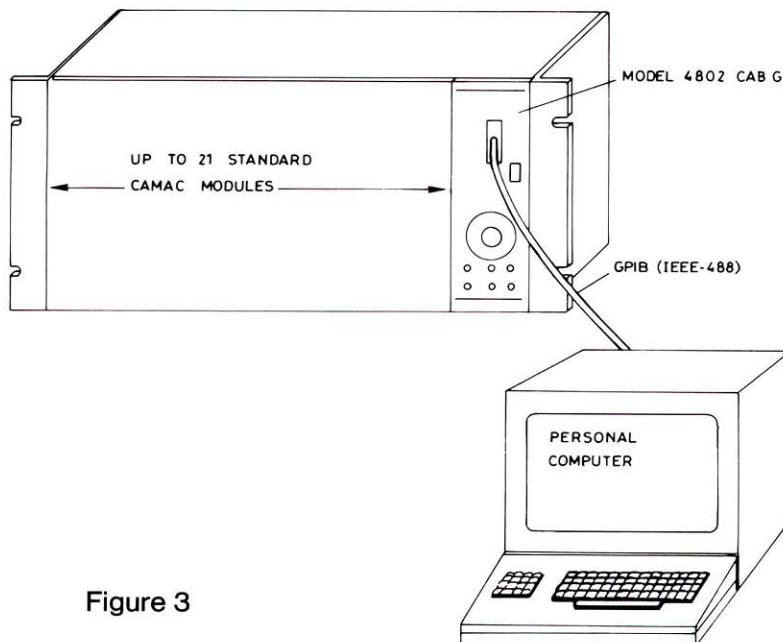


Figure 3

IV. Tree or Parallel Architectures

Figure 4 shows a proposed CAMAC architecture for an experiment at a major research facility in North America. It uses a Model 4804 CAB CG to introduce distributed programmable intelligence in the CAMAC crate that houses the programmable trigger electronics. The first level of trigger decision is made with these LeCroy ECLine programmable logic units. The second level decision is made in the CAB CG on data read by the LeCroy Model 4300 FERAs. A Model 4302 Fast Triple Port Memory is used for fast (100 nsec/word) transfer of the data to the CAB.

The second CAMAC crate of the main data acquisition contains a Model 4805 CAB BG. This programmable CAMAC Branch Driver is capable of driving up to 7 additional CAMAC crates forming a parallel branch in the data acquisition system architecture. Additional branch drivers located in the main or secondary branches would permit even more complex systems. The Model 4805 CAB BG has the advantage that the programmable processor may be located at the node of the tree-like data acquisition architecture, thus permitting the pre-processing of data from the entire Branch.

Software and constants used in both CABs are loaded from an independent computer via the GPIB Ports of both the CAB CG and the CAB BG. The LeCroy 3500 is used in this application, but any personal computer with a GPIB interface and FORTRAN could be used. By using the GPIB port for software support, the main CAMAC data acquisition system is free to perform only data transfers.

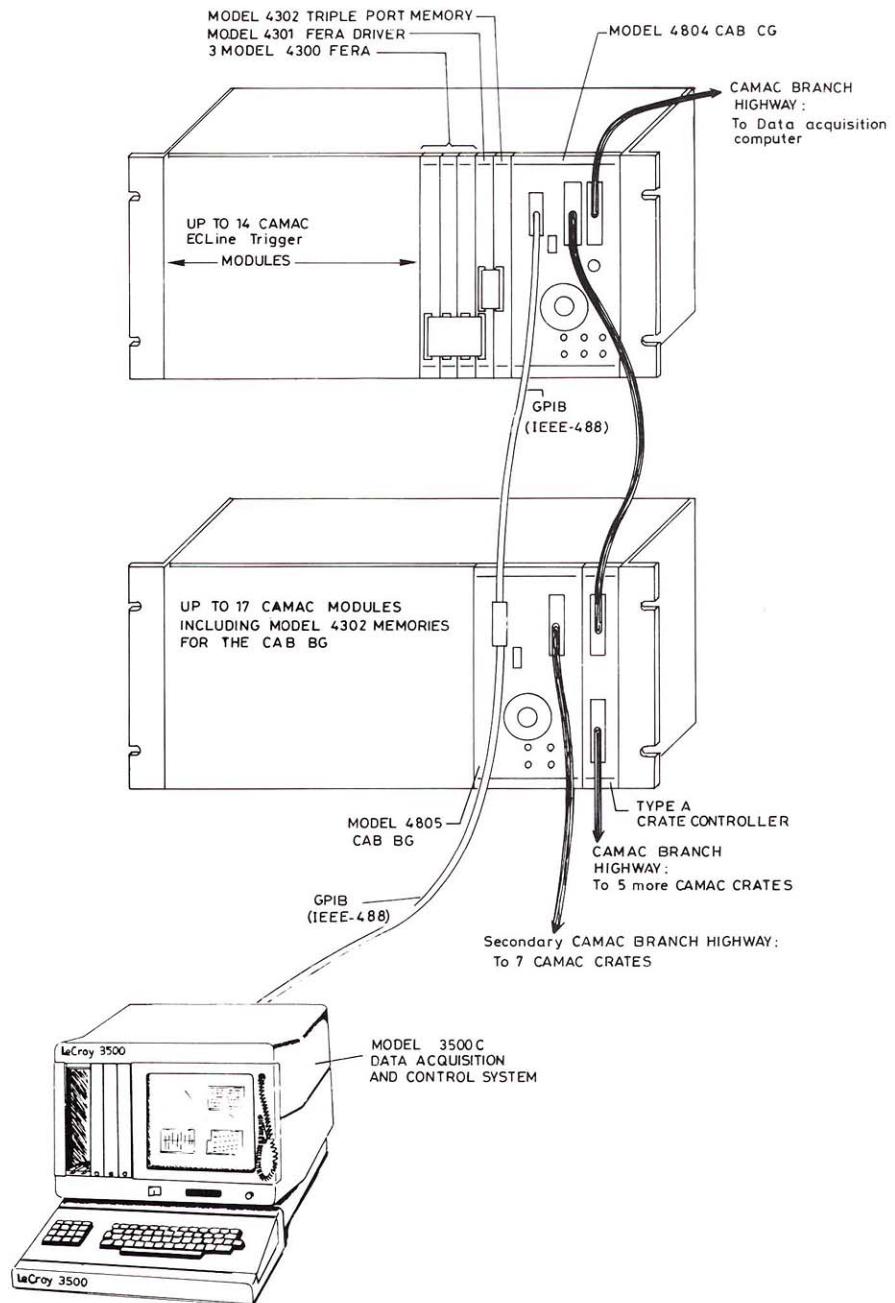


Figure 4

CAMAC Model 4801 CAB C Fast Intelligent Crate Controller

- **Dataway operations:** entirely controlled by software.
- **LAM Grader:** similar to a Standard Type A Crate Controller.
- **Connects to the CAMAC Branch Highway:** uses standard Hughes type connectors.

The Model 4801 CAB C is a programmable Crate Controller. It is a 4-wide CAMAC module that resides in the crate controller position within the crate. It is connected to the CAMAC Branch Highway via two standard Hughes type CAMAC Branch Highway Connectors. The CAB C is a slave to the Branch and master of the Crate.



CAMAC Model 4802 CAB G Fast Intelligent GPIB to CAMAC Crate Controller

- **Dataway operations:** entirely controlled by software.
- **LAM Grader:** similar to a Standard Type A Crate Controller.
- **Connects to the GPIB (IEEE-488):** uses standard IEEE-488 type connector.
- **May function as a "Talker" or a "Listener".**

The Model 4802 CAB G is a programmable Crate Controller that interfaces to the main data acquisition system through the IEEE-488 Bus (GPIB) via a standard IEEE-488 Bus connector. It may function as a "talker" or a "listener". The CAB G is a 4-wide CAMAC unit that resides in the crate controller position, and is a slave to the GPIB and master of the Crate.

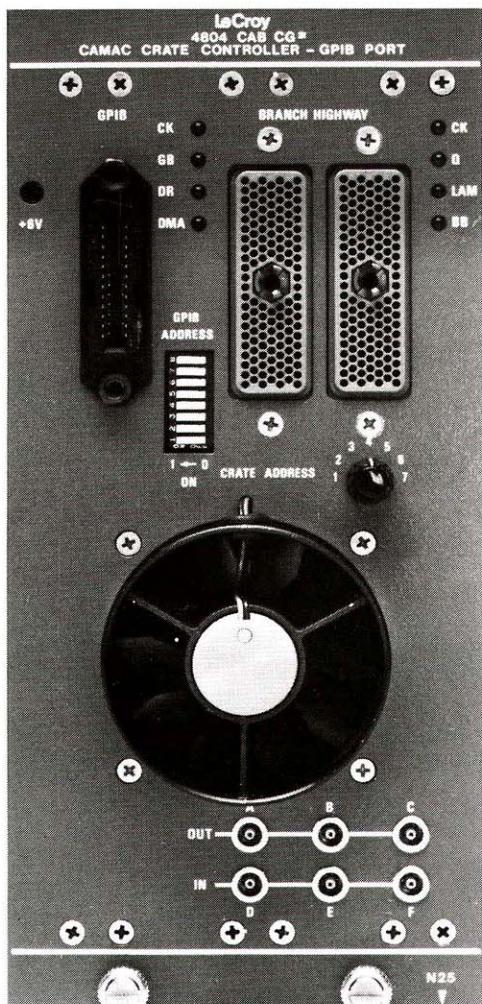


CAMAC Model 4804 CAB CG Fast Intelligent Crate Controller with GPIB Port

- **Dataway operations:** entirely controlled by software.
- **LAM Grader:** similar to a Standard Type A Crate Controller.
- **Connects to the CAMAC Branch Highway:** uses standard Hughes type connectors.
- **Connects to the GPIB (IEEE-488):** uses standard IEEE-488 type connector.
- **May function as a GPIB "Talker" or a "Listener"**

The Model 4804 CAB CG CAMAC Crate Controller with GPIB Port is a programmable Crate Controller with an extra interface port. It combines the features of the CAB C and the CAB G in that it is a slave to both the CAMAC Branch Highway and the GPIB. The CAB CG has both the dual Hughes type CAMAC Branch Highway Connectors and a standard IEEE-488 Bus connector. This 6-wide module is the master of the CAMAC Crate.

The GPIB Port frees the main CAMAC data acquisition system from the responsibility of downloading and maintaining the CAB's software, including constants. A separate computer or microprocessor may be used to handle this task.

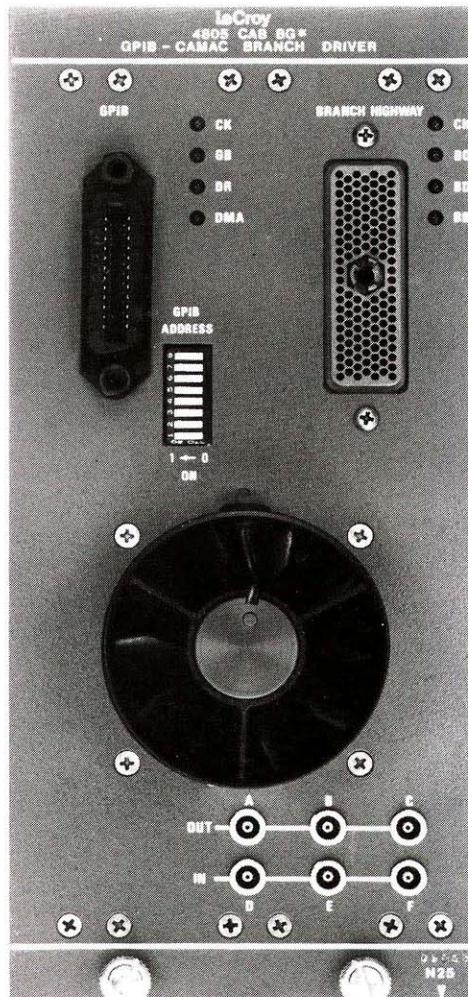


CAMAC Model 4805 CAB BG Fast Intelligent Branch Driver with GPIB Port

- **Branch operations:** entirely controlled by software.
- **Drives up to 7 CAMAC Crates via its own Branch Highway:** uses standard Hughes type connector.
- **Connects to the GPIB (IEEE-488):** uses standard IEEE-488 type connector.
- **May function as a GPIB "Talker" or a "Listener".**

The Model 4805 CAB BG CAMAC Branch Driver with GPIB Port resides in any position of a CAMAC Crate except the crate controller position. The CAB BG is a full CAMAC Branch Driver capable of driving a standard Branch with up to 7 crates. By using the CAB BG, tree-like or parallel architectures may be created in a CAMAC system with distributed programmable processing power located at each node.

The CAB BG is a slave on the Dataway of the CAMAC Crate in which it resides. The CAB BG is also a slave to its GPIB Port. It is a 6-wide module with a single Hughes type connector to drive its private CAMAC Branch, and a standard IEEE-488 connector to interface with the GPIB.





CAMAC Model 4801

Fast Intelligent Crate Controller (CAB C)

- **16-bit bipolar processor:** 4 AM2901 bit slices provide multi-operand instructions.
- **Fast basic cycle time:** 200 nsec.
- **16-bit times 16-bit Multiplier/Accumulator:** operates in 200 nsec.
- **High speed Multibit Shifter.**
- **4 K 16-bit RAM Data Memory.**
- **4 K 24-bit RAM Instruction Memory.**
- **Dataway operations:** entirely controlled by software.
- **Programmed with micro-instructions:** precise control of the processor operation.

The LeCroy Model 4801 CAB C is a fast bit-slice processor configured as a CAMAC Crate Controller. Developed by LPNHE/Ecole Polytechnique Palaiseau to accelerate data handling, the CAMAC Booster or CAB permits very high speed processing and control to be distributed within CAMAC networks.

HARDWARE DESCRIPTION

The CAB C, shown in the simplified block diagram of Figure 1, consists of three processor boards and one interface board, interconnected by a 16-bit data bus and a 24-bit instruction bus.

The sequencer board contains 4 K of 24-bit instruction memory which is addressed by an AM2910 microprogram controller. The use of a pipeline register at the output of the RAM allows the simultaneous execution of an instruction while the next one is being fetched. The powerful instruction set of the AM2910 sequencer permits a large choice in the program flow direction, including conditional and unconditional jumps, subroutine calls, do-loops, etc. The next-instruction address may be chosen entirely under program control, from either the internal micro-program counter, an internal 5-deep stack, an indirect instruction address register or the instruction being executed. The instruction memory can be read and written into by CAMAC instructions from the Branch Highway.

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The arithmetic and logic unit board consists of 4 AM2901 4-bit slices, configured as a 16-bit processor with 16 internal registers, and a 4 K 16-bit data memory. The ALU can perform 16-bit additions, subtractions and logic functions (AND, OR, etc.) on 2 operands, usually internal registers. One operand may be the external data bus. It is also possible to shift the result of an ALU-function by one bit to the left or to the right in the same instruction. The data memory is addressed by the sum of 2 address sources: a direct data address contained in the instruction itself and the contents of the indirect data address register. The use of the address register is optional and it may be turned off under program control.

The multiplier board contains a multi-bit shifter and a TRW1010J multiplier/accumulator. The shifter permits shifting a 16-bit word to the left by up to 15 bits in a single instruction. The result is a 32-bit word. A right-shift by n bits is accomplished by a (16-n) left-shift with the result in the 16 most significant bits. It is also possible to normalize numbers, i.e., shift them to the left until the left-most bit is a one. The multiplier has an associated memory of 256 16-bit words. It takes just one instruction cycle to multiply a 16-bit word from the data bus with a 16-bit word from the multiplier memory. Optionally, the product may be added to an internal 35-bit accumulator within the same instruction cycle. This mode is very useful for matrix multiplications, Fourier transforms, etc., where expressions of the form

$$p = a_0x_0 + a_1x_1 + a_2x_2 + \dots + a_nx_n \text{ occur.}$$

The interface board contains all circuitry necessary for communication with the CAMAC Dataway and the Branch Highway. The CAB C is master of the dataway; it has full programmed control over the 24 Read- and Write-lines as well as the function and address lines. The LAM's are encoded by priority and can be read on the data bus. They cannot interrupt the processor directly, but the presence of a LAM can be tested. The CAB C communicates with the Branch Highway on 16 bits only (BRW1-BRW16), but all 24 Branch Read-Write lines are bridged across the 2 Hughes 132-pin connectors, so that the Branch Highway remains 24 lines wide. The CAB responds directly only to Branch Highway functions with N(31) (See section on CAMAC functions). CAMAC-commands with $N \neq 31$ require response by controller simulation software which is delivered with the unit.

INSTRUCTION SET

The CAB processor is programmed in micro-instructions, i.e., each instruction is immediately executed in a single 200 nsec cycle.

Since the instruction and data memories are separate, execution and next-instruction fetch are simultaneous. The program-counter is identical to the microprogram-counter, and is an internal register of the AM2910 sequencer. Therefore, all 16 registers of the ALU may be freely used as general purpose registers. Four types of instructions are distinguished: internal ALU operations, transfer functions on the data bus, branch instructions for the sequencer, and general purpose functions. All operations involving the shifter and the multiplier are considered transfers. The CAB cannot be interrupted directly, apart from stopping it by the CAMAC-command N(31)•F(25)•A(0). Normal interrupts are simulated by testing interrupt bits.

ALU Operations:

These instructions follow very closely the internal structure of the ALU (Fig. 2). The 16 internal registers form a dual port RAM, i.e., it is possible to simultaneously read two registers. If the A-address is equal to the B-address, the same register contents appear both at the A-output and the B-output. The inputs to the arithmetic logic unit are chosen from the internal registers A and B, the external "DATA IN" register, the value zero and the additional temporary storage registers Q. Most, but not all, combinations of two out of these five sources are possible (for details, see the CAB Users' Handbook). The following operations among the two chosen operands are possible:

R + S	R AND S
S - R	R AND S
R - S	R EX-OR S
R OR S	R EX-NOR S

where R and S are the various ALU inputs.

Some information on the result of the operation, e.g., sign, overflow or zero, is available to the jump-instructions for conditional branches. The result of the ALU may have up to 3 different, simultaneous destinations: DATA OUT, the Q-register and the internal register addressed by B. In addi-

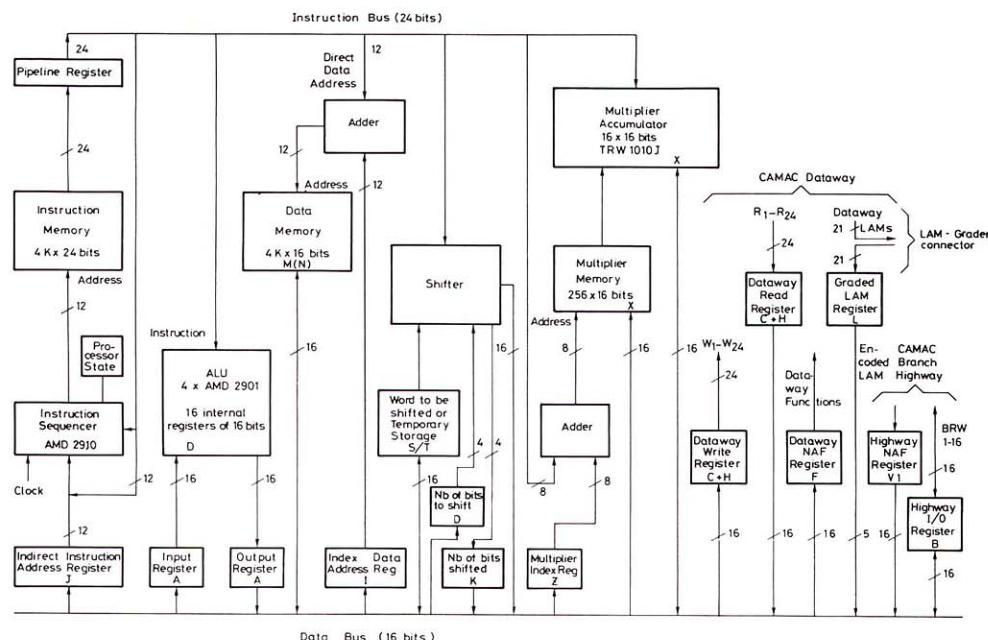


Figure 1. Internal configuration of CAB C

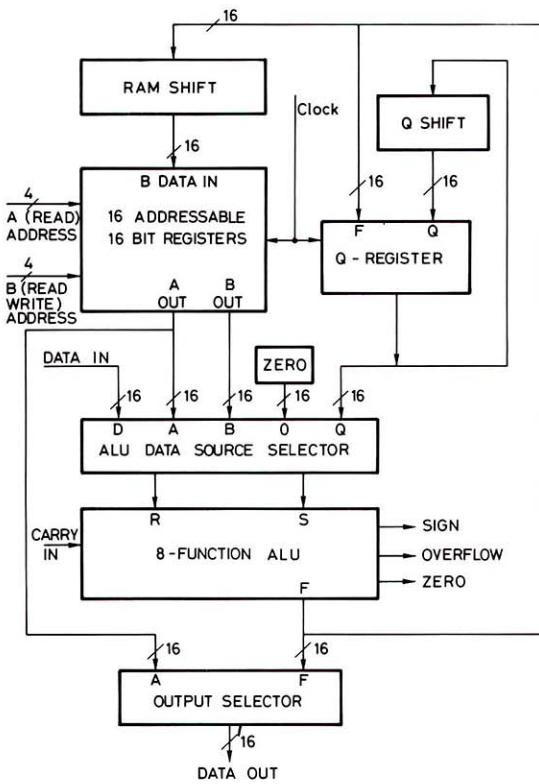


Figure 2. Internal structure of the 16-bit arithmetic logic unit

tion, the result may be left- or right-shifted by 1 bit before being loaded into the B-register. It is even possible to simultaneously shift the contents of the Q-register.

The assembly instructions for the ALU have the following format:

DESTINATION LINK R OPERATION S (+ CARRY)

The destination which may be up to three different locations, is always specified in the order RAM-register (Bn), DATA OUT and Q-register.

The link-operator specifies if the result is to be shifted before loading it into B or Q. The following eight combinations of destinations and link-operators are possible:

RAM (B-Address)	Data Out	Q-Reg	Link Operator	Destination Code
N	F	F	=	0
N	F		=	1
Fn	Am		=	2
Fn	F		=	3
Fn	F	Q	Ri	4
Fn	F		Ri	5
Fn	F	Q	Li	6
Fn	F		Li	7

"N" means that the internal RAM-register is not loaded, i.e., it keeps its original values. When the Q-register is not specified as a destination, it is simply omitted. Fn with n = 0, 1, ..., 15 indicates into which internal register the ALU-result is loaded. The link-operators L and R indicate left- or right-shift of the ALU-result before loading it into the internal register, whereas the equal sign means no shifting. In the case of destination codes 4 and 6, the contents of the Q-register are simultaneously shifted before being reloaded into Q. The R- and L- operators require an additional letter i = Z, U, C, D which indicates what is to be shifted into the

leftmost or rightmost bit, namely a zero, a one (unity) or the bit being shifted out (circular shift). D indicates double precision shifting, considering the B-register and the Q-register as a single 32-bit word.

Examples of ALU-instructions:

(1) NFF = A4 + B5

The ALU-operands R and S are the internal registers 4 and 5 on which an addition is performed. The result goes to "DATA OUT" and the Q-register (destination code 0). No new value is loaded into B5, since N (= none) is indicated.

(2) F7A7 = B7 + 1

The ALU-operands R and S are the internal register 7 and the value zero (which is omitted). To this sum added the optional carry-bit 1. Thus the register 7 is incremented by 1 in the ALU. This result goes to register 7, whereas the original contents of register 7 (A7) go to "DATA OUT" (destination code 2). This instruction is very useful for post-incrementing an address register while stepping through a block of data.

(3) F2F = D

This instruction transfers the contents of the external "DATA IN"-register to the internal register 2. Simultaneously, the value of D also appears at "DATA OUT" (destination code 3).

(4) F3F LZ B3 – A2

The ALU generates the difference between internal registers 3 and 2. This result is transmitted (non-shifted to "DATA OUT"). Internal register 3 is loaded with the ALU-result, but shifted left by 1 bit. "Z" indicates that the new rightmost bit must be a zero. Thus, the new contents of register 3 are 2^1 (Reg 3 - Reg 2). The destination code of this instruction is 7.

(5) F2FQ LD B2 – A15

The ALU produces the difference between the internal registers 2 and 15. The result is sent to internal register 2 and to the "DATA OUT" register. It is left-shifted by 1 bit before being loaded into B2. Simultaneously, the contents of the Q-register are shifted to the left and reloaded into Q. The symbol "LD" specifies the left-shift as a double-precision operation, i.e., B2 and Q are considered a 32-bit word to be shifted left. Thus, the most significant bit of Q is transferred into the least significant bit of B2. Such instructions are very useful for the software implementation of a 32-bit by 16-bit division algorithm.

Transfer Instructions:

These operations always involve the transfer of 16-bit data from a sender to a receiver on the data bus. Some examples of data senders are:

Mnemonic	Location
A	"DATA OUT" register of ALU
M addr	Data memory (directly addressed)
N addr	Data memory (indirectly addressed)
S L	16 least significant bits of shifter output
S M	16 most significant bits of shifter output
C	16 least significant bits of CAMAC dataway R-lines
H	8 most significant bits of CAMAC dataway R-lines

The data memory can be either directly or indirectly addressed. In the first case, "addr" specifies the absolute data memory address; in the second, the sum of "addr" and the contents of the indirect data address register (I) is used as the memory address.

Some examples of data receivers:

Mnemonic	Location
A	"DATA IN" register of ALU
M addr	Data memory (directly addressed)
N addr	Data memory (indirectly addressed)
I	Data memory index register
J	Indirect instruction address register
F	CAMAC dataway NAF register
S n	Shifter (n indicates the number of bits to shift).

The transfer of a data word into the NAF-register automatically starts a dataway operation. Similarly, transfers to the shifter or the multiplier start the shift- or multiply-operation.

Certain registers require specifiers in addition to the single-letter mnemonic such as "M addr" or "S n". Because of limitations in the instruction word size, it is not possible to directly transfer data between two such registers. In particular, data cannot be sent directly from the data memory to the shifter or to the multiplier. They must be sent through the ALU or in certain cases, through a temporary storage register.

The assembly instructions for the transfers have the following format:

T sender receiver (specifier)

All transfer instructions begin with the letter T, which is followed by the single-letter mnemonics for the sender and the receiver. A specifier is added if the sender or receiver requires one. For a complete list of the senders, receivers and the restrictions on transfers, refer to the CAB Users' Handbook.

Examples of transfer instructions:

(6) TAI

The contents of the "DATA OUT" register of the ALU are copied into the indirect data address register.

(7) TNA 0

A data memory word is transferred to the "DATA IN" register of the ALU. The memory address is the contents of the indirect data address register I (to which the offset zero was added).

(8) TMF NAF

A data memory word is transferred to the CAMAC dataway NAF-register and a dataway operation is started. The memory address is the value of the symbol "NAF."

(9) THS 2

The most significant 8 bits of the CAMAC dataway Read-lines are transferred to the shifter and left-shifted by 2 bits.

(10) TSA L

The least significant 16 bits of the shifter-output are transferred to the "DATA IN" register of the ALU.

(11) TAX CNST SUM

The value of the "DATA-OUT" register of the ALU is transferred to the multiplier. This number is immediately multiplied with the contents of the multiplier memory which are defined at the address by the value of the symbol "CNST." SUM indicates that the product is to be added to the value already contained in the accumulator of the multiplier. This instruction, like all the others, takes just 200 nsec.

Branch Instructions:

The CAB permits full advantage to be taken of the complex, but very powerful, instruction set of the AM2910 instruction sequencer. It is possible to execute conditional as well as unconditional jumps, calls to subroutines, do-loops, 2-way and 3-way branches, etc. This highly efficient way of controlling the program flow is one of the keys to the CAB's high speed. Among the condition codes which may be tested are the sign of the ALU-result, overflow of the ALU-operation, X-or Q-response of the CAMAC Dataway, the presence of a LAM or of an external NIM-level interrupt, etc.

The assembly instructions for the branch-instructions have the following format:

branch-type condition-code branch-address

Examples of branch types are:

C	Call subroutine
J	Jump
R	Return
XC	Execute conditionally
RC	Load register-counter (internal to sequencer)
STOP	Halt
XP	Execute repeat

The branch-instructions RC and STOP are unconditional instructions; they need neither condition codes nor an address. However, RC needs the number which is to be loaded into the register-counter. The first four branch-types in the list above may be modified with condition codes which always consist of two letters.

The first letter can only be:

N if not
F if

The second is one of 16 single-letter mnemonics for condition bits. Examples are:

N	Result of ALU negative
Z	Result of ALU zero
L	LAM present
Q	Dataway Q-response

Since a blank is interpreted as absence of any condition, the two condition code letters must follow the branch-type immediately.

Examples of branch instructions:

(12) C SUBR

Call subroutine SUBR. The address of the next instruction is pushed onto a stack in the sequencer and is available to the return-instruction at the end of the subroutine.

(13) CNN SUBR

Call, if not negative, subroutine SUBR. Similar to instruction (12), but with a condition.

(14) JFZ NEXT

Jump, if zero, to routine NEXT. The return address is not put onto the stack, i.e., it is not possible (in a simple way) to return to the instruction following this one.

(15) JNL*

Jump, if no LAM, to itself. The asterisk is equivalent to the value of the program-counter. This instruction loops on itself until a LAM-signal is present.

(16) RFN

Return if negative. If the result of the last ALU-operation was negative, return from the subroutine; otherwise continue. This instruction allows conditional returns from subroutines. "R" by itself would specify an unconditional return.

(17) RC TEN

Load register-counter with the value TEN. The register-counter, internal to the sequencer, can be used as loop-counter. This instruction allows its setup. Loading it with the value n will result in executing a given loop $n+1$ times.

(18) XP

Execute and repeat. This branch instruction, typically inserted at the end of a loop, decrements the register-counter by one. If the result is zero, the next instruction is the one following the current one, i.e., the execution of the loop is terminated. If the result is non-zero, the next address is taken from the internal stack of the sequencer which should contain the address of the beginning of the loop. Both the register-counter and the stack must have been set up correctly before executing the loop. There is an instruction available to do both in a single cycle.

(19) XCFZ FAIL

Execute conditionally and leave if zero. XC is the most complex instruction since it allows a three-way branch. Upon execution, it simultaneously decrements the register-counter and tests the condition code. If the condition is satisfied, the program leaves the loop and continues immediately after the instruction XC. If the condition is not satisfied and the register-counter is non-zero, the next instruction address is taken from the internal stack (which must contain the address of the beginning of the loop), i.e., the loop is repeated. If the condition is not satisfied and the register-counter has reached zero, the program branches to the routine FAIL. This instruction is very useful, e.g., for a memory search which is to be terminated when finding the desired memory content or when reaching the search limit.

General functions:

There are a few control functions which do not fit into the other three categories of instructions. The assembly instructions for the general functions have the following format:

G function-mnemonic

Examples of general functions:

(20) G Z

Generates a Z on the CAMAC Dataway

(21) G I

Inhibits execution of dataway instructions.

(22) G IB

Generates a 100 nsec wide NIM-pulse at the front-panel LEMO-output B. There are 3 such LEMO-outputs, labelled A, B and C.

Other general functions include BX, BQ response, branch demand BD and acknowledge BTB on the CAMAC Branch Highway.

Unlike a crate controller type A, the CAB C responds to commands with $N=31$. These commands are the only ones to which the CAB C responds independently of the state of the processor. All CAMAC commands with $N \neq 31$ have only the effect of loading two data registers in the CAB C, i.e., the highway I/O register (B) with BRW1-16 and the highway NAF register V1 with BN, BA and BF (see Figure 1). In addition a test-bit B is available to the CAB-branch instructions for checking on the presence of a Branch Highway command. There is no way of controlling the CAMAC dataway directly with Branch Highway commands. All such commands must pass through an emulator program resident in the instruction memory of the CAB C. A program package which emulates the CAMAC Crate Controller type A exists, and is made available with the unit. A list of all recognized CAMAC functions with $N=31$ is found on the last page of this data sheet. The instruction memory can be read and written into directly, provided the processor is stopped. However, reading or writing into the data memory, requires the CAB to run a communication routine since the data memory address cannot be controlled directly. Repeated application of $N(31)\cdot F(25)\cdot A(0)$ steps the processor through the instructions one by one. Since the instruction address and the instruction itself can be read at any time, debugging from the host system is possible.

SOFTWARE

A host computer is needed to develop applications software for the CAB. There exists the following range of development aids, some of which were developed at the European Organization for Nuclear Research (CERN) in Geneva, Switzerland:

Name	Program Language
Cross Assembler	FORTRAN
Debugger	FORTRAN
Micro Exec	CAB Assembly Language
Test Programs	CAB Assembly Language

The Debugger stays resident in the host computer; it contains facilities to down-load applications or test programs to the CAB, start or stop it, and to follow the execution of CAB programs step by step.

The "Micro-Exec" is a very simple form of an operating system for the CAB processor. Its minimum form contains the emulation of the type A crate controller. Further programs which exist, include a histogramming package and a memory management routine (which requires external memory modules on the CAMAC dataway). In addition, it is planned to develop packages for floating point operations and Fourier transforms. These programs may be optionally down-loaded into the CAB. The minimum Micro-Exec may be down-loaded from the host computer or provided in the form of a programmable read only memory. Some of the above mentioned development aids which run on the host machines, are currently being adapted in order to obtain a complete set capable of running on either one of these processors:

VAX-11	Nord-10/100
PDP-11	HP-1000
LeCroy 3500	CDC-6600/7600

CAMAC FUNCTIONS

The CAB C can be addressed from the CAMAC Branch Highway. Like a type A controller, it has a seven-position switch to select a crate number between 1 and 7.

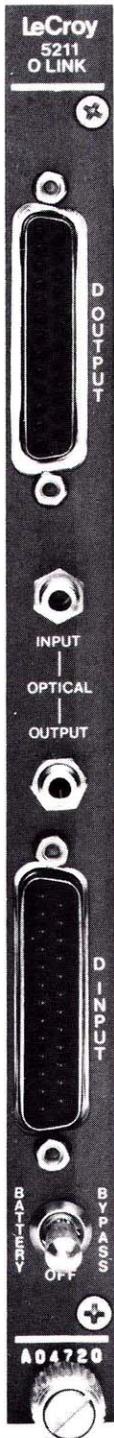
SPECIFICATIONS

CAMAC Model 4801

FAST INTELLIGENT CRATE CONTROLLER (CAB C)

ALU:	4 AM 2901 bit slice processors.																																				
Program Sequencer:	AM2910.																																				
Data Memory:	4 K 16-bit RAM.																																				
Program Memory:	4 K 24-bit RAM.																																				
Multiplier/Accumulator:	TRW1010J 16 × 16 bit—35-bit result.																																				
Shifter:	Max. 15-bit shift (hardwired AM 25510 based).																																				
Speed:	Every instruction executed in 200 nsec.																																				
Front Panel:	3 input Lemo for external NIM [™] interrupts; 3 output Lemos for external NIM pulses; LED's for CLOCK, Q response, LAM, I/O indications.																																				
Highway Connectors:	2 Branch Highway connectors 132 pin Hughes.																																				
CAMAC Commands And Functions:	<p>Listed functions are recognized by 4801 CAB C model when addressed with N = 31. For 1 ≤ N ≤ 21 every command is transmitted via software emulation to the addressed module. For 22 ≤ N < 31, CAB C accepts standard commands of type A Crate Controller.</p> <table border="0" style="width: 100%;"> <thead> <tr> <th style="text-align: left;"><i>Functions</i></th> <th style="text-align: right;"><i>CAB Response</i></th> </tr> </thead> <tbody> <tr> <td>F(0)•A(0) Read Data</td> <td style="text-align: right;">X = 1, Q = 1 Data Ready</td> </tr> <tr> <td>F(0)•A(2) Read 8 MSB Instruction</td> <td style="text-align: right;">X = 1, Q = 1 CAB Stopped</td> </tr> <tr> <td>F(0)•A(3) Read Address</td> <td style="text-align: right;">X = 1, Q = 1 CAB Stopped</td> </tr> <tr> <td>F(1)•A(1) Read 16 LSB Instruction and Address Increment Load Instruction Register</td> <td style="text-align: right;">X = 1, Q = 1 CAB Stopped</td> </tr> <tr> <td>F(8)•A(0) Test Branch Demand</td> <td style="text-align: right;">X = 1, Q = 1 if BD present</td> </tr> <tr> <td>F(9)•A(0) Initialize CAB</td> <td style="text-align: right;">X = 1</td> </tr> <tr> <td>F(16)•A(0) Write Data</td> <td style="text-align: right;">X = 1, Q = 1 if Data Taken</td> </tr> <tr> <td>F(16)•A(2) Write 8 MSB Instruction</td> <td style="text-align: right;">X = 1, Q = 1 CAB Stopped</td> </tr> <tr> <td>F(16)•A(3) Write Address</td> <td style="text-align: right;">X = 1, Q = 1 CAB Stopped</td> </tr> <tr> <td>F(17)•A(1) Write 16 LSB Instruction and Address Increment</td> <td style="text-align: right;">X = 1, Q = 1 CAB Stopped</td> </tr> <tr> <td>F(24)•A(0) Mask Branch Demand</td> <td style="text-align: right;">X = 1</td> </tr> <tr> <td>F(25)•A(0) Step By Step Stop CAB</td> <td style="text-align: right;">X = 1</td> </tr> <tr> <td>F(25)•A(1) Start CAB (Run)</td> <td style="text-align: right;">X = 1</td> </tr> <tr> <td>F(26)•A(0) Unmask Branch Demand</td> <td style="text-align: right;">X = 1</td> </tr> <tr> <td>F(27)•A(0) Test Branch Demand Mask</td> <td style="text-align: right;">X = 1, Q = 1 if BD Enabled</td> </tr> <tr> <td>F(27)•A(1) Test Data Taken</td> <td style="text-align: right;">X = 1, Q = 1 if Data Taken</td> </tr> <tr> <td>F(27)•A(2) Test CAB Stopped</td> <td style="text-align: right;">X = 1, Q = 1 if CAB Stopped</td> </tr> </tbody> </table>	<i>Functions</i>	<i>CAB Response</i>	F(0)•A(0) Read Data	X = 1, Q = 1 Data Ready	F(0)•A(2) Read 8 MSB Instruction	X = 1, Q = 1 CAB Stopped	F(0)•A(3) Read Address	X = 1, Q = 1 CAB Stopped	F(1)•A(1) Read 16 LSB Instruction and Address Increment Load Instruction Register	X = 1, Q = 1 CAB Stopped	F(8)•A(0) Test Branch Demand	X = 1, Q = 1 if BD present	F(9)•A(0) Initialize CAB	X = 1	F(16)•A(0) Write Data	X = 1, Q = 1 if Data Taken	F(16)•A(2) Write 8 MSB Instruction	X = 1, Q = 1 CAB Stopped	F(16)•A(3) Write Address	X = 1, Q = 1 CAB Stopped	F(17)•A(1) Write 16 LSB Instruction and Address Increment	X = 1, Q = 1 CAB Stopped	F(24)•A(0) Mask Branch Demand	X = 1	F(25)•A(0) Step By Step Stop CAB	X = 1	F(25)•A(1) Start CAB (Run)	X = 1	F(26)•A(0) Unmask Branch Demand	X = 1	F(27)•A(0) Test Branch Demand Mask	X = 1, Q = 1 if BD Enabled	F(27)•A(1) Test Data Taken	X = 1, Q = 1 if Data Taken	F(27)•A(2) Test CAB Stopped	X = 1, Q = 1 if CAB Stopped
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Power Requirements:	11 A at + 6 V; 200 mA at - 6 V.																																				
Packaging:	RF-shielded #4 width CAMAC module.																																				

SPECIFICATIONS SUBJECT TO CHANGE



Model 5211

CAMAC Byte-Serial Optical Link

- 100% electrical isolation of Serial Highway
- One fiberoptic cable between crates
- 40 Mb/sec data rate
- Battery backup
- 62 crate system at full speed
- Up to 500 m between crates
- EMI RFI immune
- No electromagnetic radiation

The LeCroy Model 5211 Optical Link is a fiberoptic receiver/driver designed for use in CAMAC Serial Highway systems. Operating in the byte serial mode, it provides data transfer rates of up to 5 MB/sec or 40 Mb/sec. By connecting the Model 5211 to the D-Ports of the Serial Highway Driver and L2 Crate Controllers, the control loop is converted to fiberoptics. Up to 62 crates can be interconnected.

LeCroy's exclusive Automatic Threshold Control makes direct coupling of all circuitry possible. As a consequence, a uniquely simple encoding scheme is employed. It operates at less than a 10^{-12} bit error rate. A bypass mode further enhances system data reliability by automatically providing battery backup during a power down condition in the crate. This feature is activated within 10 msec of a loss of CAMAC power.

During power down operation, a self-contained normally charging battery pack is automatically connected to the fiberoptic transmitter and receiver within the Model 5211. A data bypass path is established between the transmitter and receiver, enabling them to operate as a repeater.

Interconnection of Model 5211 Optical Links is performed with strengthened, $50\ \mu$ graded index, optical fiber. To permit maximum performance, a fiber with a bandwidth of 200 MHz-km or greater and a numerical aperture of 0.2 or greater is required. The fiber should be terminated with an Amphenol type 906 SMA connector or equivalent.

SPECIFICATIONS

Model 5211

BYTE-SERIAL CAMAC OPTICAL LINK

Electrical Input/Output:	Standard D connectors pin-for-pin compatible with the Serial Highway. Used in conjunction with the L2 crate controller or the Serial Highway Driver. Levels and impedance specified by RS422 (CCITT Recommendation V.II (X.27).
Optical Input/Output:	Front panel connectors to mate with the Amphenol 906 series or equivalent. Byte clock and data via a single fiber.
Data Rate:	0-5 MB/sec, as determined by the CAMAC system clock.
Data Integrity:	$<10^{-12}$ bit error rate for up to 500 m with recommended fiber.
Recommended Fiber:	50 μ graded index fiber with an attenuation of <6 dB/km, a numerical aperture of 0.2 and a bandwidth of 200 MHz-km.
Data Encoding:	Byte clock and data via one fiber. Transmitted at 60M Baud. Data rates to 5 MB/sec (40 Mb/sec).
Battery Backup:	Within 10 msec of loss of CAMAC power, causes electrical shunt of fiberoptic input to output without regeneration. Powered by rechargeable NiCad batteries. Up to two crates in a row can lose power and the rest of the loop integrity is maintained. Battery capacity 30 minutes. Recharge time 30 minutes per minute of operation.
Battery/Bypass Switch:	Front panel switch. In the OFF position, battery backup is defeated. Used for storage of the Model 5211. In the BYPASS position, the Model 5211 serves only as a repeater with battery backup. In the BATTERY mode, normal operation with battery backup is provided.
Power Requirements:	800 mA at +6 V 2.5 A at -6 V 25 mA at +24 V 25 mA at -24 V
Packaging:	In conformance with CAMAC standard for nuclear modules ESONE Committee Report EUR4100 or IEEE Report 583. RF-shielded CAMAC #1 module.

SPECIFICATIONS SUBJECT TO CHANGE

TECHNICAL DATA

LeCroy

Series 5310A 100 Mb/sec Fiberoptic Digital Link

- **High Data Rate:** DC to 100 Mb/sec NRZ
- **DC Coupled:** Synchronous or Asynchronous data
- **Low Error Rate:** 10^{-9} at 10 μW input power
 10^{-12} at 12 μW
- **Low Jitter:** 400 psec rms at 10 μW input power
- **Schottky TTL Levels**
- **Automatic Threshold Control (ATC):** No set up required

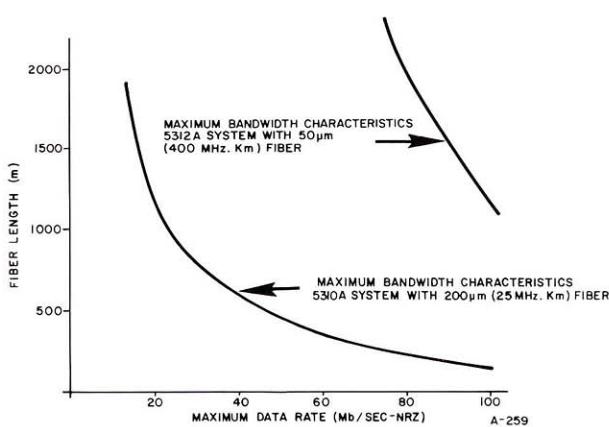


The 5310A Series is a family of 100 Mb/sec fiberoptic link transmitter-receiver pairs designed to provide data transmission over the entire TTL bandwidth. An R suffix denotes the receiver module and a T suffix, the transmitter.

All of the circuitry in both the transmitter and the receiver is DC coupled. A unique Automatic Threshold Control (ATC) sets and maintains the threshold level within the receiver. It operates independently of the data rate with no setup or control required by the user. The ATC operates over a 20 to 1 range of input amplitudes. DC coupling eliminates the need for the complicated encoding schemes which AC coupled circuits employ to eliminate rate effects. The 5310A Series will respond accurately to a single pulse without any need for setup.

The 5310A Series is compact and easy to use. It features fiberoptic input and output connectors compatible with standard Amphenol 905/906 fiberoptic connectors. Electrical connections are supplied via a 16 contact pc edge. The 5310A Series requires ± 5 V only. Their small size is compatible with direct panel mounting and pc mounting.

The Series is designed for use with a variety of optical fibers. Selection of the correct fiber should take into account the length and the bandwidth required. For maximum economy with short runs or low data rates, a 200 μm core fiber may be used. For high rates and long distances, a 50 μm core fiber is recommended. The bandwidth properties typical of these cable/LED combinations is shown in the figures below. Consult the ordering information below to select the corresponding transmitter. The 5310AR receiver is used with any of the transmitters.



Model 5600 NIM Housings

The Model 5600 Transmitter or Receiver Housing is a single width NIM Module. It accommodates a maximum of two receiver channels or two transmitter channels of fiberoptic links of the 5300 or 5400 Series. Up to 12 NIM housings can be installed in a NIM Bin for a maximum of 24 channels.

The Model 5600 provides a system capability for fiberoptic analog and digital links. Front panel LED's on the NIM Housings provide link on/off status. The use of NIM packaging allows IEEE standard power supplies and provides additional EMI shielding for the system.

SPECIFICATIONS

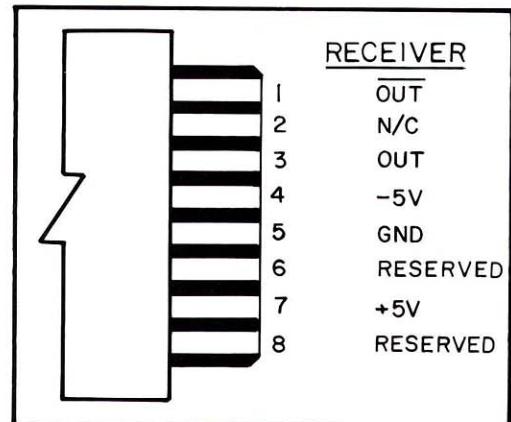
Series 5310A

DIGITAL FIBEROPTIC LINKS

TOP VIEW

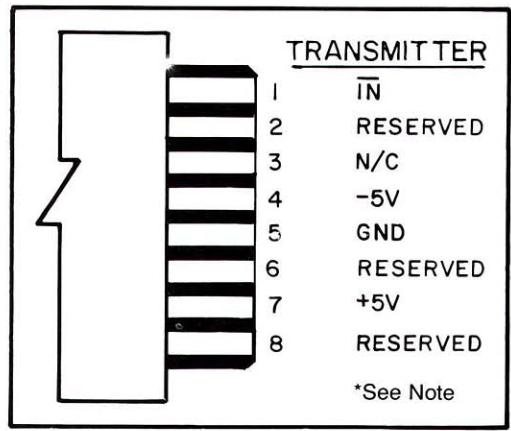
MODEL 5310AR FIBEROPTIC RECEIVER

Input Power for 10^{-9} BER at 100 MBPS-NRZ:	$10 \mu\text{W}$ typical (-20 dBm)
Maximum Data Rate:	100 Mb/sec-NRZ
Dynamic Range:	Greater than 13 dB
Data Output Time Jitter:	0.4 nsec rms, typical
Data Output Logic Level:	TTL, $\overline{\text{TTL}}$
Data Error Rate:	10^{-9} BER with $10 \mu\text{W}$ input 10^{-12} BER with $12 \mu\text{W}$ input
Power Supplies:	+ ($5 \pm .25$) V, 40 mA - ($5 \pm .25$) V, 50 mA
Detector Type:	PIN Diode



MODELS 5310AT-5312AT FIBEROPTIC TRANSMITTERS

Useful Output Power:	200 μW (-7 dBm) for 5310T*
	70 μW (-11.5 dBm) for 5312T**
Output Rise and Falltimes:	Typically less than 5 nsec
Input Logic Levels:	TTL, 5 V CMOS compatible
Power Supply:	+ 5 V at 120 mA - 5 V at 85 mA
Emitter Type:	820 nm LED

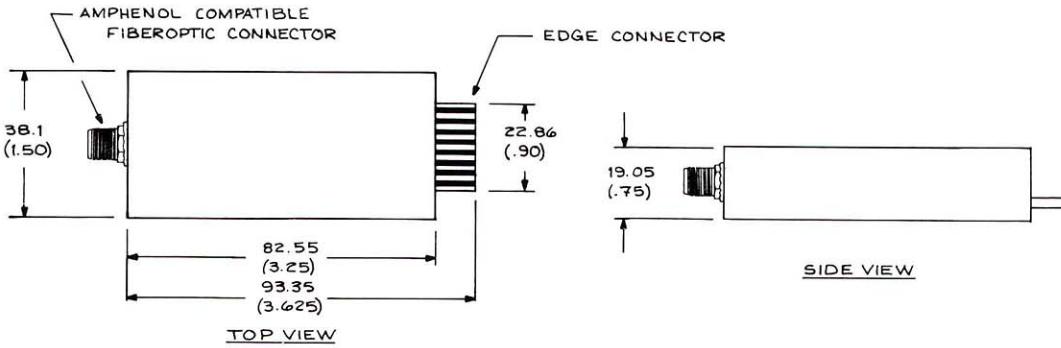


Transmitter Ordering Information:	Model No.	Link Performance Option
	5310AT	200 μm core cable
	5312AT	50 μm core cable

* Measured at the end of 100 m of 200 μm fiber

** Measured at the end of 100 m of 50 μm fiber

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NOTE: Underside of connector tongue is ground plane. Dual 8 connector 0.1 inch spacing PC card-edge connector right angle mounting. LeCroy Part No. 455-660-016



SPECIFICATIONS SUBJECT TO CHANGE

TECHNICAL DATA

LeCroy

Series 5330A

ECL Digital Fiberoptic Link with Automatic Threshold Control (ATC)

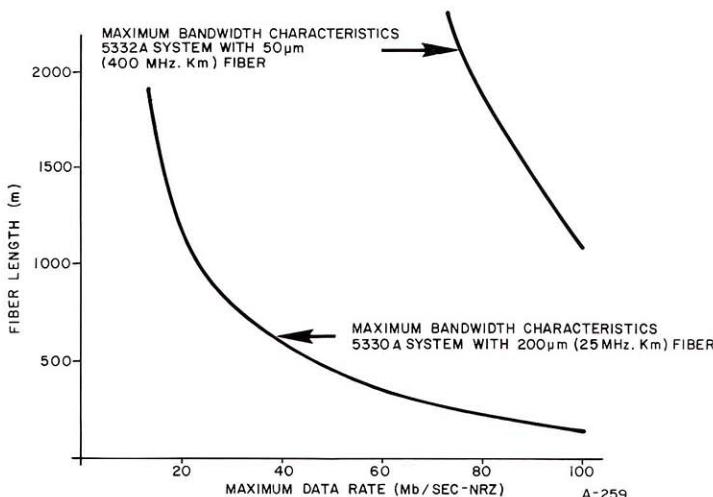
- **High Data Rate:** DC to 100 Mb/sec NRZ
- **DC Coupled:** Synchronous or Asynchronous data
- **Low Error Rate:** $<10^{-9}$ at 10 μW input power
 $<10^{-12}$ at 12 μW
- **Low Jitter:** 400 psec rms at 10 μW input power
- **Differential ECL Levels**
- **Automatic Threshold Control (ATC):** No setup required

The 5330A Series is a family of 100 Mb/sec fiberoptic link transmitter-receiver pairs providing single-ended or differential ECL inputs and outputs. An R suffix denotes the receiver module and a T suffix, the transmitter.

All of the circuitry in both the transmitter and the receiver is DC coupled. A unique Automatic Threshold Control (ATC) sets and maintains the threshold level within the receiver. It operates independently of the data rate with no setup or control required by the user. The ATC operates over a 20 to 1 range of input amplitudes. DC coupling eliminates the need for the complicated encoding schemes which AC coupled circuits employ to eliminate rate effects. The 5330A Series will respond accurately to a single pulse without any need for setup.

The 5330A Series is compact and easy to use. It features fiberoptic input and output connectors compatible with standard Amphenol 905/906 fiberoptic connectors. Electrical connections are supplied via a 16 contact PC edge. The 5330A Series requires ± 5 V only. Their small size is compatible with direct panel mounting and PC mounting.

The Series is designed for use with a variety of optical fibers. Selection of the correct fiber should take into account the length and the bandwidth required. For maximum economy with short runs or low data rates, a 200 μm core fiber may be used. For high rates and long distances, a 50 μm core fiber is recommended. The bandwidth properties typical of the combination of the fiberoptic link and the fiber is shown in the figure below. Consult the ordering information below to select the corresponding transmitter. The 5330AR receiver is used with any of the transmitters.



A-259



Model 5600 NIM Housings

The Model 5600 Transmitter or Receiver Housing is a single width NIM Module. It accommodates a maximum of two receiver channels or two transmitter channels of fiberoptic links of the 5300 or 5400 Series. Up to 12 NIM housings can be installed in a NIM Bin for a maximum of 24 channels.

The Model 5600 provides a system capability for fiberoptic analog and digital links. Front panel LED's on the NIM Housings provide link on/off status. The use of NIM packaging allows IEEE standard power supplies and provides additional EMI shielding for the system.

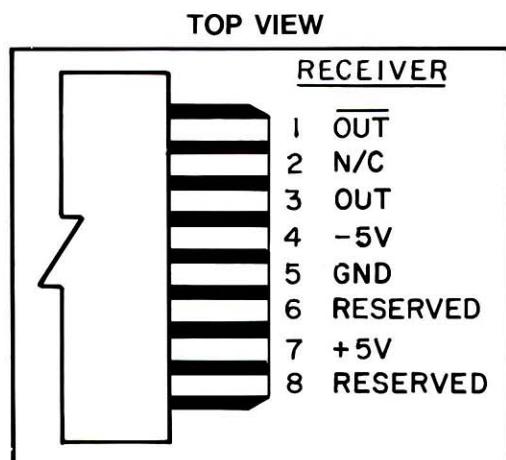
SPECIFICATIONS

Series 5330A

DIGITAL FIBEROPTIC LINKS

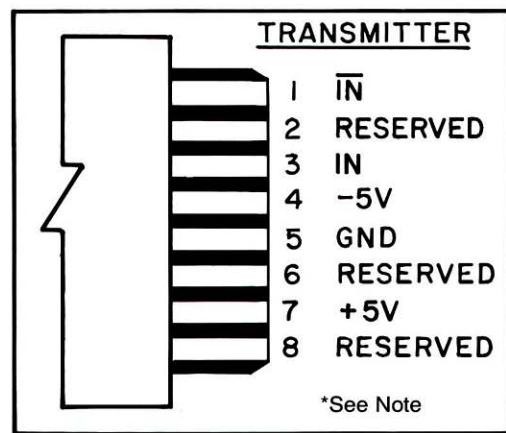
MODEL 5330AR FIBEROPTIC RECEIVER

Input Power for 10^{-9} BER at 100 Mb/sec-NRZ:	10 μW typical (-20 dBm)
Maximum Data Rate:	100 Mb/sec-NRZ
Dynamic Range:	>13 dB
Data Output Time Jitter:	0.4 nsec rms, typical
Data Output Logic Level:	ECL, $\overline{\text{ECL}}$
Data Error Rate:	< 10^{-9} BER with 10 μW input < 10^{-12} BER with 12 μW input
Power Requirements:	40 mA at +(5 ± 0.25) V 50 mA at -(5 ± 0.25) V
Detector Type:	PIN Diode



MODELS 5330AT-5332AT FIBEROPTIC TRANSMITTERS

Useful Output Power:	200 μW (-7 dBm) for 5330AT*
	70 μW (-11.5 dBm) for 5332AT**
Output Rise and Falltimes:	Typically less than 5 nsec
Input Logic Levels:	Differential ECL For single ended ECL, connect unused input to Pin 2
Power Requirements:	120 mA at +(5 ± 0.25) V 85 mA at -(5 ± 0.25) V
Emitter Type:	820 nm LED



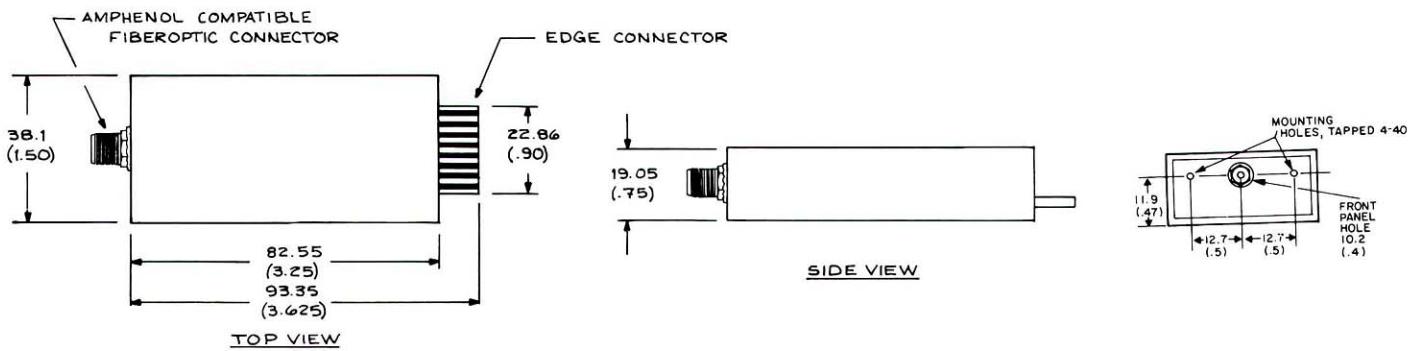
*See Note

NOTE: Underside of connector tongue is ground plane. Dual 8 connector 0.1 inch spacing PC card-edge connector right angle mounting. LeCroy Part No. 455-660-016

Transmitter Ordering Information:	Model No.	Link Performance Option
	5330AT	200 μm core cable
	5332AT	50 μm core cable

* Measured at the end of 100 m of 200 μm fiber

** Measured at the end of 100 m of 50 μm fiber



SPECIFICATIONS SUBJECT TO CHANGE

TECHNICAL DATA

LeCroy

Series 5403A

Analog Fiberoptic Link with Automatic Gain Control (AGC)

- **Wide Bandwidth:** 250 MHz typical
- **Long Range:** 300 m
- **Economical:** uses 50 μm fiber
- **Fiddle Free:** Automatic gain control



The LeCroy Models 5403AT Fiberoptic Transmitter and 5403AR Fiberoptic Receiver have been designed to provide a ≥ 200 MHz analog link over distances of up to 300 m. An automatic gain control circuit within the pair eliminates concerns over degradation of the LED, the optical fiber or the optical coupling.

The 5403A pair covers the bandwidth range of <60 Hz to >200 MHz with a dynamic range response of 40 dB. The device accepts signals of up to 800 mV p-p for linear response.

Using 50 μm fibers such as LeCroy FC-50-M, the full bandwidth is maintained for distances of up to 300 m. For longer fibers, the attenuation and dispersion of the fiber limits the system bandwidth.

Model 5600 NIM Housings

The Model 5600 Transmitter or Receiver Housing is a single width NIM Module. It accommodates a maximum of two receiver channels or two transmitter channels of fiberoptic links of the 5300 or 5400 Series. Up to 12 NIM housings can be installed in a NIM Bin for a maximum of 24 channels.

The Model 5600 provides a system capability for fiber-optic analog and digital links. Front panel LED's on the NIM Housings provide link on/off status. The use of NIM packaging allows IEEE standard power supplies and provides additional EMI shielding for the system.

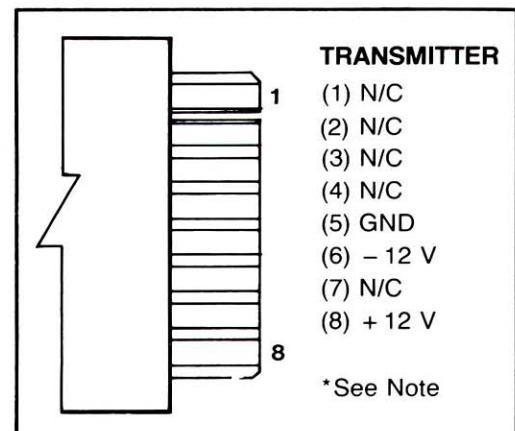
SPECIFICATIONS

Series 5403A

ANALOG FIBEROPTIC LINK

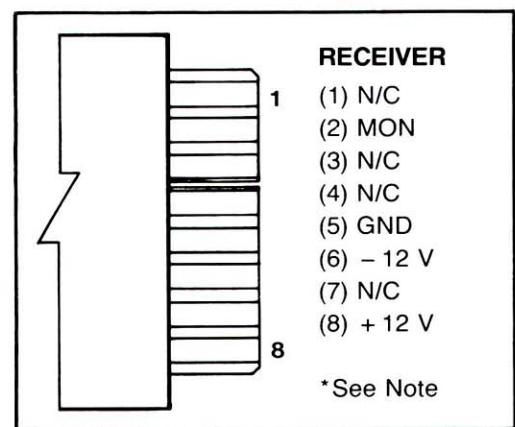
5403AT ANALOG TRANSMITTER

Input: RG196A/U coaxial pigtail, terminated in
 $50 \Omega \pm 5\%$
 Input Range: 800 mV p-p maximum for linear operation
 Overload Voltage: 2 V maximum
 Output: 80 μ W (mean) into 50 μ m at a wavelength
 of 850 nm
 Output Connector: Amphenol 906
 Power Requirements: 100 mA typical at $-(12 \pm 0.1)$ V



5403AR ANALOG RECEIVER

Input: Amphenol 906
 Minimum Input Power: 0.5 μ W
 Output: RG196A/U coaxial pigtail. Requires a
 50 Ω termination.
 Output Voltage: 80 mV p-p maximum
 Output Impedance: Suitable for driving a 50 Ω load.
 Power Requirements: 100 mA at $+(12 \pm 0.5)$ V
 50 mA at $-(12 \pm 0.5)$ V

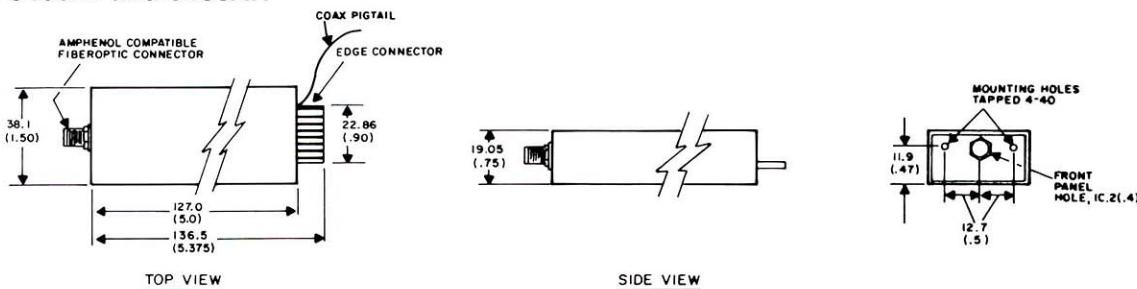


OVERALL PERFORMANCE

Risetime: 1 nsec (10% to 90%)
 Bandwidth: <60 Hz to >250 MHz typical
 (200 MHz minimum)
 Integral Nonlinearity: <5% deviation from a best straight line fit over the range 0-800 mV p-p
 Output S/N Ratio: 30 dB at 10 μ W input to Receiver
 Mid Frequency Response: Flat to within a 5% deviation from best straight line
 Overall Gain: 0.1
 Gain Stability: $\pm 1\%$ from 0 to 120°F
 $\pm 1\%$ for changes $<\pm 50\%$ in optical signal
 850 nm

NOTE: Underside of connector tongue is ground plane. Dual 8 connector 0.1 inch spacing PC card-edge connector right angle mounting. LeCroy Part No. 455-660-016 (TEKA 011-08441-290).

MODELS 5403AT and 5403AR



TECHNICAL DATA

LeCroy

Series 5413A

Analog Fiberoptic Link with Automatic Gain Control (AGC)

- Bandwidth to 50 MHz
- 2 km range
- Compatible with 50 μm and 100 μm fiber
- Automatic gain control

The LeCroy Model 5413AT Transmitter and 5413AR Receiver provide transmission of analog signals through 50 μm optical fiber. These modules transmit signals within a 150 Hz to 50 MHz bandwidth between points that can be up to two km apart. Automatic gain control is used to maintain a constant system gain despite changes in the optical path attenuation. This feature is an effective way to eliminate variations due to degradation of the LED or to changes in the optical path.

5413AT TRANSMITTER

The Transmitter incorporates an amplifier to give an input full scale range of ± 1 V. The amplifier provides a degree of high frequency pre-emphasis that can be adjusted to compensate for the characteristics of the cable used.

5413AR RECEIVER

The receiver converts signals from the transmitter back into electrical form. An AGC circuit is used to maintain the system gain (output range equals 2 V p-p for a 2 V p-p input), regardless of the strength of the input optical signal. The only effect of a reduction in signal strength is to reduce the system signal to noise ratio. A factory set potentiometer cuts out the AGC at a S/N ratio around 20 dB.



Model 5600 NIM Housings

The Model 5600 Transmitter or Receiver Housing is a single width NIM Module. It accommodates a maximum of two receiver channels or two transmitter channels of fiberoptic links of the 5300 or 5400 Series. Up to 12 NIM housings can be installed in a NIM Bin for a maximum of 24 channels.

The Model 5600 provides a system capability for fiberoptic analog and digital links. Front panel LED's on the NIM Housings provide link on/off status. The use of NIM packaging allows IEEE standard power supplies and provides additional EMI shielding for the system.

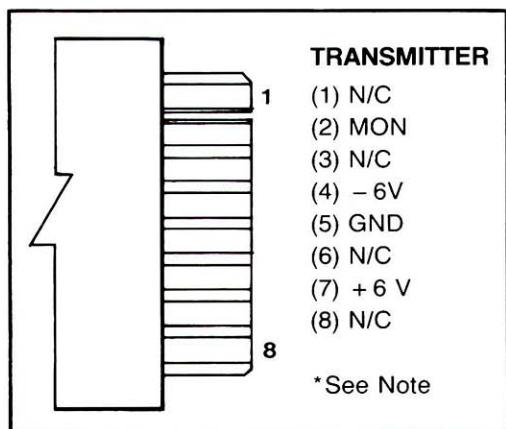
SPECIFICATIONS

Series 5413A

ANALOG FIBEROPTIC LINK

5413AT ANALOG TRANSMITTER

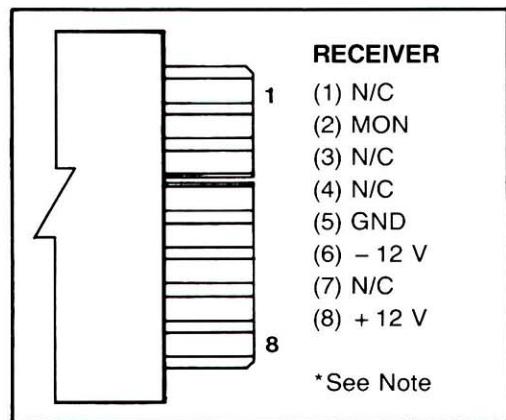
Input: Coaxial pigtail
 Input Range: 2 V p-p
 Input Impedance: 50 Ω ± 5%
 Overload Voltage: ± 5 V DC maximum
 Output: Amphenol 906 connector
 Output Power: 80 μW mean
 Modulation Depth: 4 μW/mV
 Linearity: < 1%
 Bandwidth: 150 Hz to 50 MHz
 Monitoring: MON output for LED to indicate drive electronics are functioning
 Power Requirements: 125 mA at -(6 ± 0.25) V
 125 mA at +(6 ± 0.25) V



5413AR ANALOG RECEIVER

Input: Amphenol 906 connector
 Input Range: 0.5 to 20 μW mean
 Note: This assumes a minimum loss of 60 μW in the fiberoptic cable assembly because output of the transmitter is 80 μW. An input over 20 μW will overdrive the receiver.
 Output: Coaxial pigtail. (Requires a 50 Ω termination)
 Output Impedance: Approximately 5 Ω (suitable for driving a 50 Ω load).
 Output Voltage: 2 V p-p into 50 Ω
 Output S/N Ratio: > 40 dB at 10 μW input
 Monitoring: MON output for LED to indicate that the input signal is within the AGC range
 Power Requirements: 110 mA at +(12 ± 0.25) V
 110 mA at -(12 ± 0.25) V

NOTE: A LED (MV5222) connected between the MON (pin #2) and -6V will provide an indicator that the transmitter is active.



5413A SYSTEM

Range: ≤ 2 km
 Note: For fibers of < 500 m, saturation of the receiver is possible. This will be evidenced by vastly reduced bandwidth. To reduce the power at the receiver, add one or more couplings such as an additional short length of fiber at the receiver.
 Mid-frequency Response: Flat to within 1/4 dB
 Gain Stability: ± 1% from 0 to 120°F
 ± 1% for changes < ± 50% in optical signal 850 nm

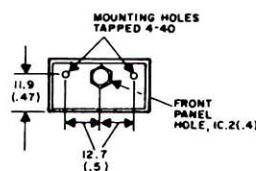
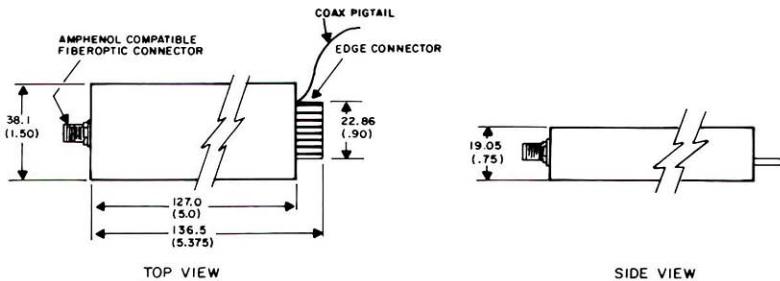
NOTE: A LED (MV5222) connected between the MON (pin #2) and ground will provide an indication that the receiver is operating within the range of the unit's AGC.

NOTE: Underside of connector tongue is ground plane. Dual 8 connector 0.1 inch spacing PC card-edge connector right angle mounting. LeCroy Part No. 455-660-016 (TEKA 011-08441-290).

CONNECTORS

PC Edge: Right angle PC mountable edge connector for power and signal input/output. LeCroy Part Number 455-660-016.

MODEL 5413AT and MODEL 5413AR



Models 5612 and 5613

DC to 1 MHz Analog Fiberoptic Transmission System with Remote Transmitter Control

- **Dynamic range:** 54 dB
- **Frequency response:** DC to 1 MHz
- **Programmable input sensitivity:** manually set at receiver or computer programmed via CAMAC
- **Self-calibration**
- **CAMAC compatible:** ideal for multichannel applications
- **Transmits analog data to a CAMAC crate via fiberoptic cable:** permitting Transient Recorders and A/D Converters to be electrically isolated
- **Software supported:** LeCroy's Transient Acquisition Software Package (MAPS) and the Model 3500C CAMAC Data Acquisition and Control System
- **Battery powered transmitter**
- **Two channel receiver module:** permits control and signal acquisition for two transmitters using one receiver



The Model 5612 Transmitter and the Model 5613 Receiver together with a suitable cable pair form a complete analog fiberoptic transmission system. They provide a means by which analog signals from transducers that are located in noisy environments, at high electric potentials, and at great distances, can be monitored while maintaining high signal integrity.

By implementing the latest in frequency modulation technology, the 5612-5613 System is able to transmit analog signals up to 1 kilometer with better than 54 dB of usable dynamic range and a 1 MHz bandwidth. The System is well matched to the front end characteristics of LeCroy's medium speed Transient Recorders as shown in the comprehensive catalog.

The link is bidirectional. Analog information is sent from the transmitter and reconstructed at the receiver. A remote control link is used to send calibration and operational mode commands to the transmitter, enabling the full scale input to match the transducer output. To extend battery life during long experiments, the transmitter can be turned off and on by remote control.

The full scale input range (± 0.2 V to ± 100 V in 1, 2, 5 sequence) and four test voltages (\pm Full Scale, 0.00 V, and Battery Check) are all selectable over this remote control link. These settings are determined either by front panel switches located on the 5613 Receiver, or by a standardized computer interface.

The 5612 enclosure is designed to operate in a high EMI environment. Thus signal integrity is preserved even when the phenomena which are measured induce electromagnetic noise. The unit is ideally suited for applications where fiberoptic isolation is necessary and a systems level approach is desired. The remote control feature is useful in experimental situations where it is costly or hazardous to change the input characteristics of the transmitter once the experiment has begun, such as in power transmission line monitoring, weapons simulation experiments, weapons testing, fusion research, laser diagnostics, high energy physics and high explosive research.

SPECIFICATIONS

Models 5612 and 5613

ANALOG FIBEROPTIC LINK

5612 TRANSMITTER

Input Impedance:	10 M Ω \pm 5%, shunted by less than 30 pF
Size:	4 \times 6 \times 8.25 inches
Weight:	9 lbs.
Battery:	12 V, 6 Amp-hour, gelled electrolyte rechargeable battery
Power Consumption:	250 mA Transmitter ON 200 μ A Transmitter OFF
Fiberoptic Connectors:	Amphenol 905/906
Operating Temperature:	- 10°C to + 40°C
Signal Connector:	Female, Lemo Size 3 triaxial. Male Lemo connector may be ordered from LeCroy and it is suitable for mounting on RG 174/W cable.
Auxiliary Power Connector:	External 12 V battery input. Battery charger input.
Power Switch:	Three position slide switch that determines whether the transmitter is internally powered, power is off, or the external power input is connected.
Local/Remote Control:	Slide switch. When set to Local, the transmitter operational status may be manually set at the transmitter. When set to Remote, the transmitter operational mode may be set by the computer interface or by the manual controls on the front panel of the receiver module.
Range Switch:	Sixteen position rotary switch. Used to set the calibration input or input range when the Local/Remote switch is in its Local position.
Optical Output:	65 μ watts mean power

5613 RECEIVER

Signal Output:	Negative Full Scale, 0.00 Volts and Positive Full Scale signals applied to the transmitter inputs will produce - 1.00, 0.00, and + 1.00 Volts, respectively. A \pm 2.5 V output option is available. Output impedance 50 Ω . Differential Lemo type connector. LeCroy Model CKDLEM is the mating connector. Suitable for mounting RG/174C cable.
Dimensions:	CAMAC #2 module
Optical Input Sensitivity:	4 μ watts
Front Panel Controls and Indicators:	Two LED displays indicate the range setting of the two independent channels A and B. Toggle switches are used to select ranges. Two LED's show whether the transmitters are in the power on or power off mode. An on-off switch is provided for each channel. Diagnostic LED's indicate when the module is addressed and when its LAM output is asserted.
Fiberoptic Connectors:	Amphenol 905/906 connectors are mounted on the rear of the module.

5612-5613 SYSTEM

Bandwidth:	1 MHz (-3 dB) 500 KHz (-1 dB)
Transient Response:	Risetime less than 500 nsec Overshoot less than 3%
Linearity:	$\pm 0.1\%$ deviation from best straight line
Signal-to-Noise Ratio:	54 dB
Full Scale Accuracy:	$\pm 0.1\%$ (± 1 Volt input)
Full Scale Input:	± 100 V, ± 50 V, ± 20 V, ± 10 V, ± 5 V, ± 2 V, ± 1 V, ± 0.5 V, ± 0.2 V. The full scale range is programmable by front panel switches, or by computer using the CAMAC interface.
Calibration:	To calibrate the System, three precision reference voltages may be switched across the input of the transmitter. These voltages are +1.00 V, GND, and -1.00 V.
Battery Voltage Check:	The transmitter can be instructed to connect its battery terminals to the signal input. A full scale signal output at the receiver indicates that the battery is fully charged.
Manual/Computer Control:	All of the operational parameters including the full scale input range, calibration signal, battery test and the transmitter on/off status can be set by front panel switches on the receiver module, or can be programmed by the CAMAC interface.

CAMAC COMMANDS

Z or C:	Clears all registers, sets transmitters A and B to off, and their input ranges to ± 100 V. Resets and disables LAM.
X:	X = 1 (command accepted) response is generated when a valid F and A are present.
Q:	Q = 1 is returned on an F(8)•A(0) if, and only if, the internal LAM is asserted.
LAM:	LAM (Look-At-Me) line is asserted if it has been enabled with an F(26)•A(2) and the operational parameters of either link have been manually altered.

CAMAC FUNCTION CODES

F(0)•A(0):	Read Range of Transmitter A. See Table 1.
F(0)•A(1):	Read Range of Transmitter B. See Table 1.
F(0)•A(2):	Read Status Byte. R1 and R2 True indicate that Transmitters 1 and 2, respectively, are ON. False indicates that the transmitters are OFF. R3 and R4 True indicate that channels A and B have been set manually.
F(6)•A(0):	Read module identity on R1-R16. Decimal value decoded as 5613 or as set on internal 16-bit switches.
F(8)•A(0):	Test LAM
F(10)•A(0):	Clear LAM
F(16)•A(0):	Set range of Transmitter A using W1-W4. See Table 1.
F(16)•A(1):	Set range of Transmitter B using W1-W4. See Table 1.
F(24)•A(0):	Disable Transmitter A

- F(24)•A(1): Disable Transmitter B
 F(24)•A(2): Disable LAM
 F(26)•A(0): Enable Transmitter A
 F(26)•A(1): Enable Transmitter B
 F(26)•A(2): Enable LAM

TABLE 1

DECIMAL VALUE ON WRITE LINES	TRANSMITTER SETTING/MODE
0	100 V
1	50 V
2	20 V
3	N/A
4	10 V
5	5 V
6	2 V
7	N/A
8	1 V
9	0.5 V
10	0.2 V
11	N/A
12	Ground Reference
13	Battery Voltage
14	+ Calibration
15	- Calibration

SPECIFICATIONS SUBJECT TO CHANGE

TECHNICAL DATA

LeCroy

Hybrid Model HIL401 Quad Wire Chamber Amplifier/Discriminator

- Compact
- Low Power
- ECL Compatible
- Low Cost
- $2 \mu\text{A}$ Threshold
- Protected against HV Discharge

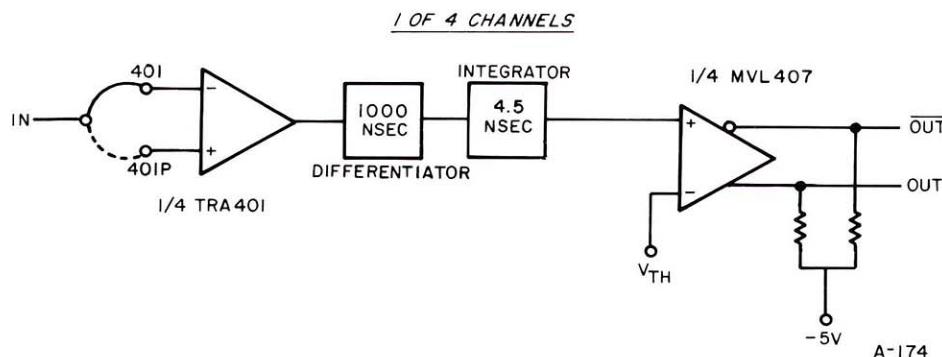


The hybrid Model HIL401 accepts inputs from 4 multiwire proportional chamber wires. It accepts inputs, which are amplified and pulse height discriminated, providing a minimum input threshold of $-2 \mu\text{A}$. (A positive version is also available for large quantity requirements.) The threshold of the 4 channels can be commonly adjusted via an externally applied control voltage. The inputs are protected against discharges of $\pm 3 \text{ kV}$ from up to 250 pF source capacitance.

The hybrid uses LeCroy's multichannel custom integrated circuits, the TRA401 Quad Preamplifier and MVL407 Quad Discriminator, resulting in simplicity, hence reliability and economy. Together, they offer high sensitivity and low power dissipation typically of 250 mW per channel.

The front-end amplifier of the HIL401 was designed for multiwire proportional chamber inputs. Its low impedance, current-sensitive inputs provide no pulse integration, thus offering high rate capability and optimum sensitivity to current pulses from wire chambers. Protection against HV discharge is provided at the input. The inputs must be AC-coupled unless driven from a high impedance source such as a floating chamber wire.

The outputs of the HIL401 are differential ECL, suitable for driving a 100Ω twisted-pair cable. The shaper preceding the discriminator, with 1000 nsec differentiating and 4.5 nsec integrating time constants, provides some noise filtering and leads to stable operation. Within the limits of this shaper, the output duration is equal to the time over threshold.



SPECIFICATIONS

Hybrid HIL401

4 CHANNEL WIRE CHAMBER AMPLIFIER/DISCRIMINATOR

Note: Input Pulse = 5 nsec risetime, 100 nsec decay constant, threshold set to $-2 \mu\text{A}$ unless stated otherwise.

Number of Channels:	4
Input Impedance:	100 Ω nominal
Input Protection:	Protected against discharges of up to 3 kV from 250 pF
Input Sensitivity:	Negative (Positive version available for quantities over 1000—Model HIL401P).
Input Offset:	-0.7 V nominal
Threshold Control Voltage:	$+12 \text{ mV}/\mu\text{A} \pm 20\%$
Minimum Threshold:	$-2.0 \mu\text{A}$ (typically $-1.0 \mu\text{A}$ bench test)
Interchannel Isolation:	>40 dB
Opposite Polarity Pulse Rejection:	>50 μA . Better for faster pulses.
Propagation Delay:	<20 nsec at $2 \times$ threshold <12 nsec at $20 \times$ threshold
Slewing:	<8 nsec, $2 \times$ to $20 \times$ threshold
Double Pulse Resolution:	<35 nsec at $5 \times$ threshold, for 8 nsec wide input pulses.
Shaping Time Constants:	Integrating, 4.5 nsec Differentiating, 1000 nsec
Hysteresis:	0.8 μA nominal
Output Pulse Width:	Equal to time over threshold except for effects of hysteresis and shaper time constant. 12 nsec minimum.
Minimum Input Pulse Width:	Approx. 8 nsec at $2 \times$ threshold
Package:	24-pin DIP (1.3" \times 0.8").
Power Requirements:	130 mA maximum at +5 V (+4.75 to +5.25 V) 120 mA maximum at -5 V (-4.75 to -5.5 V) 50 mA maximum at -2.5 V (-2.4 to -2.6 V)

SPECIFICATIONS SUBJECT TO CHANGE

TECHNICAL DATA

LeCroy

Hybrid Model HIL440/HIL441 4 Channel Drift Chamber Amplifier/Discriminator

- Compact
- Low Power
- ECL Compatible
- Low Cost
- $2 \mu\text{A}$ Threshold
- Protected against HV Discharge

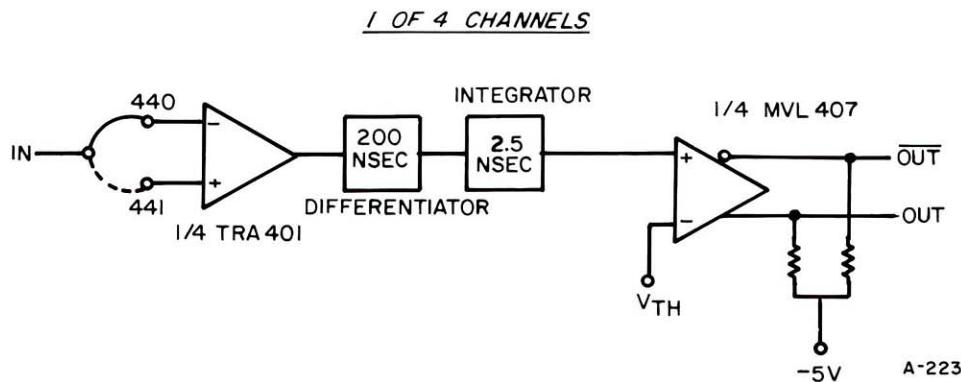


The hybrid Model HIL440/HIL441 accepts inputs from four chamber wires. The HIL440 accepts negative inputs, and the HIL441 accepts positive inputs, which are amplified and pulse height discriminated, providing a minimum input threshold of $-2 \mu\text{A}$. The threshold of the four channels can be commonly adjusted via an externally applied control voltage. The inputs are protected against discharges of $\pm 3 \text{ kV}$ from up to 250 pF.

The hybrid uses LeCroy's multichannel custom integrated circuits, the TRA401 Preamplifier and MVL407 Discriminator, resulting in simplicity, hence reliability and economy. Together they offer high sensitivity and low power dissipation of typically 250 mW per channel.

The front-end amplifier of the HIL440/HIL441 was designed for wire chamber inputs. Its low-impedance, current-sensitive inputs are uniquely suited to chamber applications, providing no pulse integration. They thus offer high rate capability and optimum sensitivity to fast current pulses from wire chambers. Protection against HV discharge is provided at the input. The inputs must be AC coupled unless driven from a high impedance source such as a floating chamber wire.

The outputs of the HIL440/HIL441 are differential ECL, suitable for driving a 100Ω twisted-pair cable. A wideband shaper preceding the discriminator, with 200 nsec differentiating and 2.5 nsec integrating time constants, provides some noise filtering. Within the limits of this shaper, the output duration is equal to the time over threshold.



SPECIFICATIONS

Hybrid HIL440/HIL441

4 CHANNEL DRIFT CHAMBER AMPLIFIER/DISCRIMINATOR

Note: Input Pulse = 5 nsec risetime, 20 nsec decay constant, threshold set to $-2 \mu\text{A}$ unless stated otherwise.

Number of Channels:	4
Input Impedance:	100 Ω nominal
Input Protection:	Protected against discharges of up to 3 kV from 250 pF
Input Sensitivity:	Negative (HIL440) or Positive (HIL441)
Input Offset:	-0.7 V nominal
Threshold Control Voltage:	$+15 \text{ mV}/\mu\text{A} \pm 20\%$
Minimum Threshold:	$-2.0 \mu\text{A}$ (typically $-1.0 \mu\text{A}$ bench test)
Interchannel Isolation:	$>40 \text{ dB}$ for 10 nsec risetime. Better for slower signals.
Opposite Polarity Pulse Rejection:	$>50 \mu\text{A}$
Propagation Delay:	$<15 \text{ nsec}$ at $2 \times$ threshold $<11 \text{ nsec}$ at $20 \times$ threshold
Slewing:	$<4 \text{ nsec}$, typical $<5 \text{ nsec}$, maximum ($2 \times$ to $20 \times$ threshold)
Double Pulse Resolution:	$<18 \text{ nsec}$ at $5 \times$ threshold, for 5 nsec wide input pulses.
Shaping Time Constants:	Integrating, 2.5 nsec Differentiating, 200 nsec
Hysteresis:	10 mV nominal ($0.6 \mu\text{A}$ referred to the input).
Output Pulse Width:	Equal to time over threshold except for effects of hysteresis and shaper time constant. 7 nsec minimum.
Minimum Input Pulse Width:	Approximately 5 nsec at $2 \times$ threshold
Package:	24-pin DIP (1.3" long \times 0.8" wide).
Power Requirements:	130 mA maximum at +5 V (+4.75 to +5.25 V) 120 mA maximum at -5 V (-4.75 to -5.5 V) 50 mA maximum at -2.5 V (-2.4 to -2.6 V)

SPECIFICATIONS SUBJECT TO CHANGE

Model HQV810**8 Channel Hybrid Preamplifier**

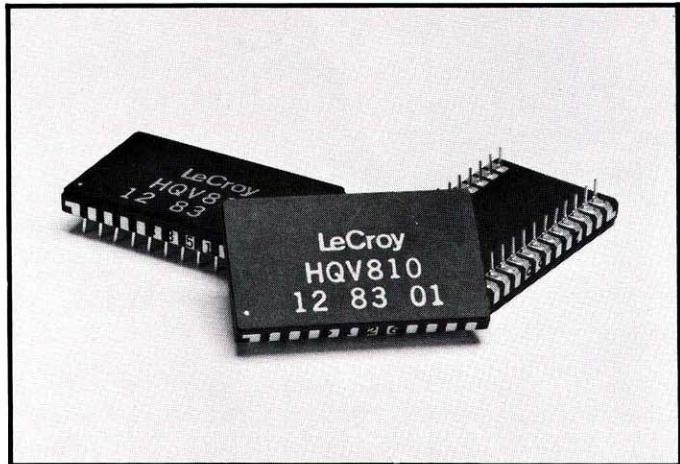
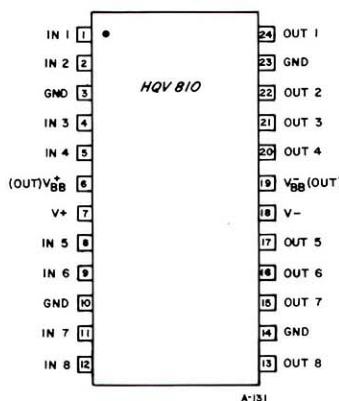
- **Compact:** 8 channels in 24-pin DIP
- **Low Noise:** <450 electrons rms (100 nsec shaping)
- **High Charge Sensitivity:** 0.5 V/pC
- **Wide Dynamic Range:** >30,000:1
- **Fast Signal Risetime:** <30 nsec
- **Drive Capability:** 50 Ω
- **Wide Range of Supply Voltages:** 3 to 13 V
- **Low Power Consumption:** <20 mW/channel
- **Input Protection:** via diodes

The LeCroy Model HQV810 is an extremely compact, low noise charge sensitive hybrid preamplifier in an 8 channel package. It can be used wherever total output charge is a key parameter. The HQV810 is ideally suited to applications requiring shaping times of <2 μsec. Typical applications include silicon strip detectors and time projection chambers.

The HQV810 is packaged in a 24-pin DIP making it ideal for high density applications. It has been designed to be operated from a wide range of supply voltages from 3 V to 13 V. At the lower setting it dissipates <20 mW/channel with remote out-

put driver pull-down resistors. This is also ideal for high density applications. When used with a high supply voltage, the HQV810 can provide extremely high dynamic range response at the expense of power dissipation.

With its extremely high resolution of <100 aC, signals in the sub-pC regime can be processed. The amplifier may be used with a high capacitance source without showing any instability. The output can drive 50 Ω loads with signal amplitudes up to several volts.



SPECIFICATIONS

Model HQV810

8 CHANNEL HYBRID PREAMPLIFIER

Note: Unless otherwise stated, all specifications at $T_A = 25^\circ C$, $V^+ = 6 V$, $V^- = -6 V$, pull down resistor (1 mA standing current in output emitter follower) load = 200Ω .

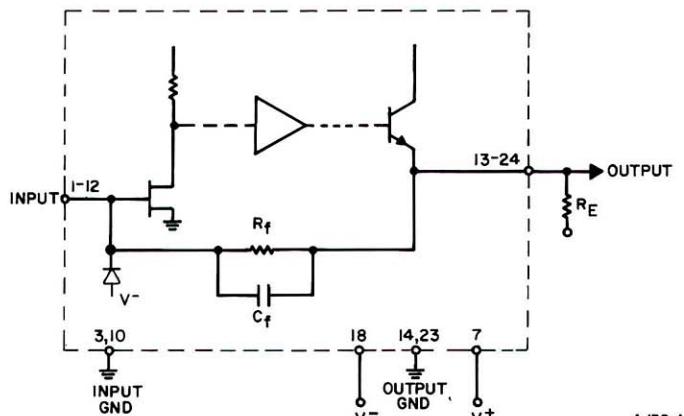
Channels:	8
Input:	Charge sensitive. Quiescent voltage (-0.8 ± 0.5) V.
Input Noise:	<450 electrons rms ($C_S = 0$ and shaping times $\tau_i = \tau_d = 100$ nsec)
Conversion Gain:	$-0.5 \pm 20\%$ V/pC inverting
Output:	Open ended emitter follower. Quiescent voltage (-1.1 ± 0.9) V.
Signal Risetime:	20 nsec typical
Signal Decay Time Constant:	4 μ sec
Maximum Output Voltage Swing:	2 V ($\geq 50 \Omega$ load) positive swing, 1 V negative swing ($\geq 200 \Omega$ load). See Figure 4 for other supply voltages than ± 6 V.
Output Impedance:	<10 Ω , depending on pull down resistor used
Open Loop Gain:	1,000 typical
Integral Non-linearity:	<0.2%
Channel-to-Channel Crosstalk:	<0.3%
Supply Voltages:	$V^+ = +3$ to $+13$ V $V^- = -3$ to -12 V <20 mW/ch with ± 3 V supplies
Package:	24-pin DIP

SPECIFICATIONS SUBJECT TO CHANGE

CIRCUIT DESCRIPTION

Each channel of the HQV810 consists of a junction FET in the input stage, a multi-transistor amplifier, and a Darlington emitter follower as an output driver stage (see Figure 1). The feedback network (R_f , C_f) is connected between the input and the output within the hybrid. The HQV810 comes with a $2 M\Omega$ value for the feedback resistor R_f and a very low value for the feedback capacitor C_f resulting in high conversion gain and low noise. The user may shunt R_f or C_f or both with external components in order to match the amplifier's performance to special needs. A typical circuit diagram of the device is shown in Figure 2.

For the operation of the amplifier, two bias voltages V_{BB^+} and V_{BB^-} are required. They are generated internally to the hybrid in common for all eight channels. The bias voltages are brought out to pins for test and bypass purposes. In most applications the internal bypass is adequate.



Input and output circuit of one channel of HQV810. Feedback network may be shunted by external components, if desired.

Figure 1

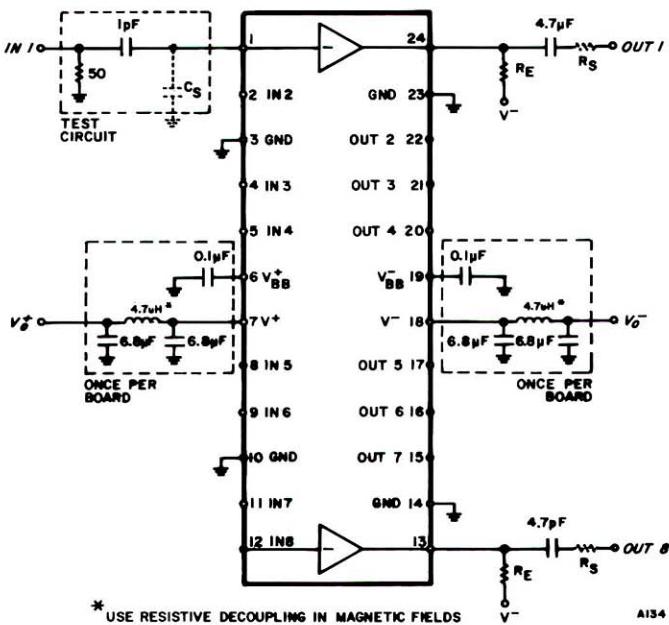


Figure 2

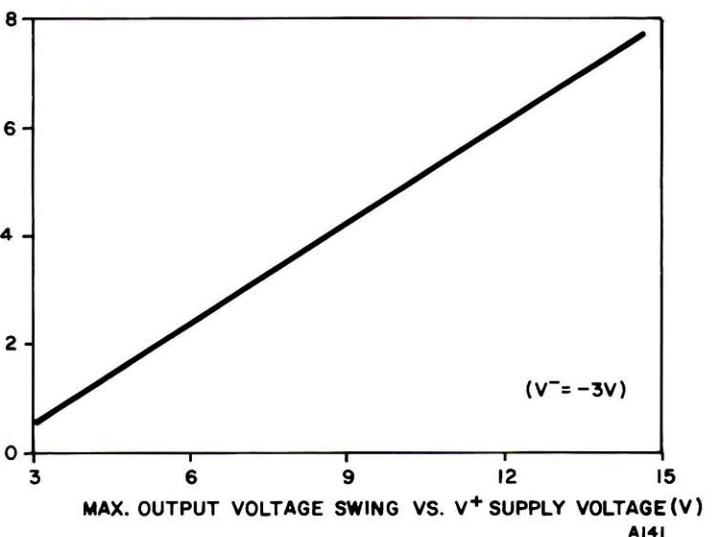


Figure 4

POWER SUPPLIES

Two voltages are employed for operation of the HQV810. All voltages utilized are internally bypassed with ceramic capacitors, yielding extremely stable operation of the device. Additional capacitance may be required on the circuit board (6.8 μ F for each of several devices).

The positive supply voltage, V^+ , may be varied for the application. See Figure 3 through Figure 6. For large values of V^+ , dynamic range response is optimized at the expense of power dissipation. Also, some small improvement in noise is obtained if $V^+ > 6$ V (see Figure 6). For high density applications, low values are preferred, minimizing power dissipation.

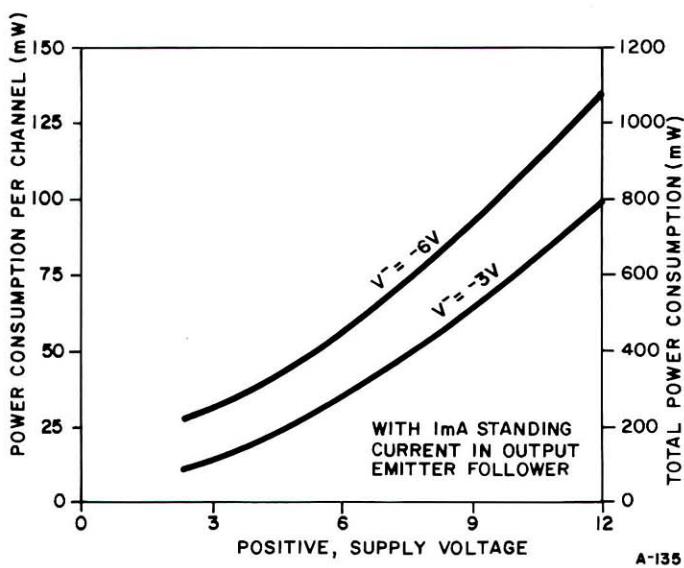


Figure 3

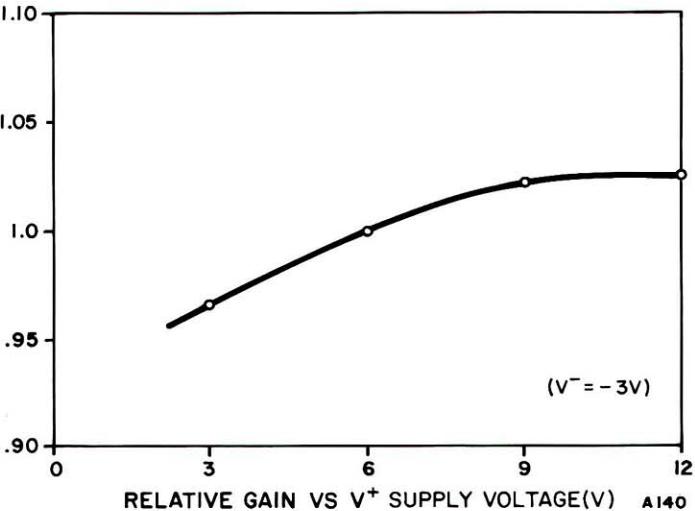


Figure 5

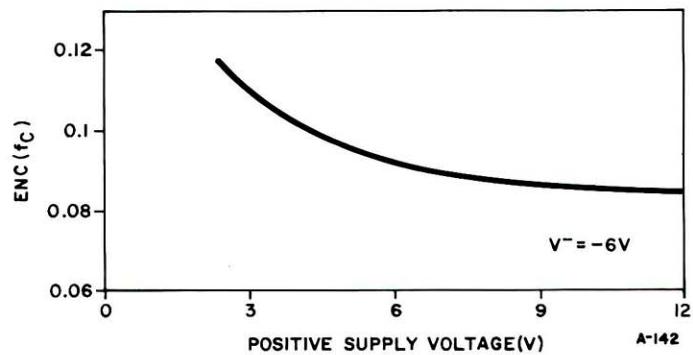


Figure 6

OUTPUT STAGE

The output of the HQV810 is an emitter follower with no pull-down resistor. Therefore, each channel requires one external resistor, R_E to a negative voltage and an appropriate value of AC output coupling capacitor. See Figure 1. The resistors may be located at the remote end of the output transmission line, thus minimizing local power dissipation. The current standing in the emitter follower sets the maximum negative output swing of the HQV810. The maximum current allowed is 50 mA DC and 100 mA for <10% duty cycles. For positive output applications, 1 k Ω to V⁻ is adequate. Other resistor values may be calculated from the specified quiescent output voltage and the value of supply voltage available.

For applications with negative inputs, values of V⁻ as low as -3 V are acceptable, however, values as large as -12 V may be employed. When negative outputs are required (i.e. positive inputs), larger values of V⁻ are required.

NOISE

The noise performance of the HQV810 depends upon the operating conditions. Figures 7 and 8 serve as a summary. In general, higher noise occurs when the capacitance of the source is large. To achieve low noise with large capacitance requires long shaping times.

All noise measurements have been made using an Ortec 450 to provide shaping. Here the shaping time is $\tau_m = \tau_i = \tau_d$.

A composite circuit (preamplifier and amplifier/shaper) is shown in Figure 9. Here an HQV810 channel is used as a shaper circuit following the HQV810 used as a preamplifier. The device has the following performance.

Integration: in first stage (preamp)

$$V_o(t) = \frac{1}{C} \int i(t) dt, C = 2 \text{ pF nominal}$$

$$\tau_i = R_d C_i$$

Differentiation: $\tau_{d1} = R_d C_d$

$$\tau_{d2} = R_i C_i$$

$$\tau_{d3} = R_L C_L$$

If $\tau_i = \tau_{d1} = \tau_{d2} = \tau$ and $R_i C_L > \tau$.

The transfer function of the shaper is given by:

$$g(s) = \frac{\tau s}{(1 + \tau s)^2}$$

$$s = j\omega$$

Assuming the falltime of the preamplifier stage is much longer than τ , the voltage gain of the shaper circuit is $g \cong 0.25$.

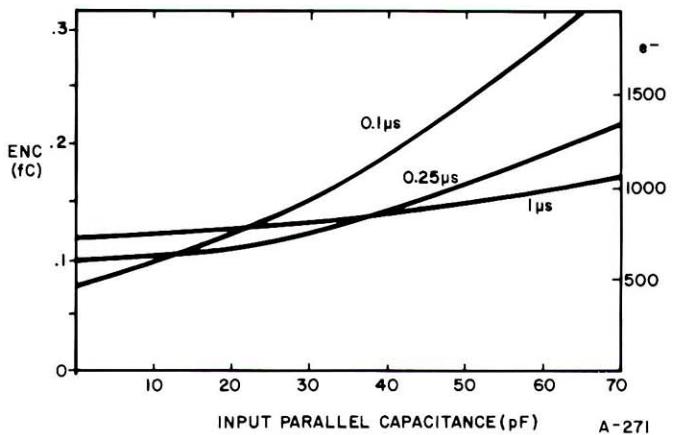


Figure 7

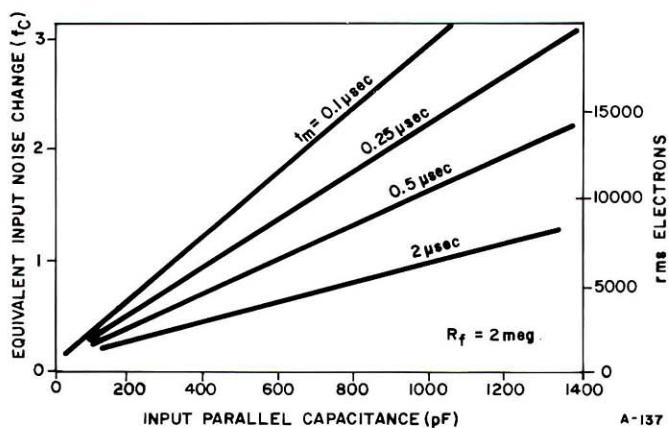


Figure 8

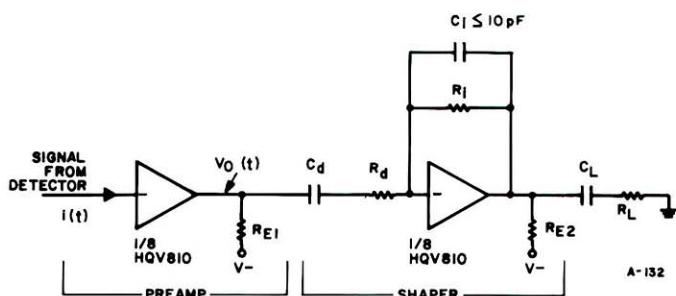


Figure 9

TECHNICAL DATA

LeCroy

System HV4032A Photomultiplier/Wire Chamber HV System

The LeCroy 4032A is a modular programmable high voltage power system for photomultiplier and wire chamber applications. The HV4032A/M mainframe provides up to 32 different voltage channels, negative or positive, ranging up to 3.3 kV or 7 kV, depending on the plug-in pods selected.

- **Comprehensive control and monitor instruction set.**
- **High density—Up to 32 channels per mainframe.**
- **Remote control—CAMAC or TTY**
- **Control daisy chain—Up to 16 mainframes per controller.**
- **Local control—Via front panel.**
- **Human engineered—Easy to use and understand.**
- **Safety features—Interlocks, trips, reporting, etc.**



Six models of plug in pods, **useable and interchangeable in any combination of up to eight pods** per HV4032A/M mainframe, are available.

Channels/ Pod:	2 channels	4 channels	2 channels
Voltage Range:	0 - 3.3 kV / 5 mA	0 - 3.3 kV / 2.5 mA	0 - 7 kV / 500 μ A
Negative	HV4016A1N	HV4032A1N	HV4032A7N- Series VII
Positive	HV4016A1P	HV4032A1P	HV4032A7P- Series VII



2 Channels

4 Channels

2 Channels

The 7 kV pods include the LeCroy Series VII design features, offering programmable current-limit, current monitor, current trip and added safety and control. The 3.3 kV pods are designed with a fixed current limit. The characteristics of all six models are summarized to the left, with details on page 7.

System Description . . .

The 4032A system consists of up to 8 pods in each HV4032A/M mainframe, with provision for remote operation of all channels in up to 16 mainframes. A single LeCroy Model 2132 Interface (described in the inset on page 8) permits daisy-chain control from CAMAC. This provides the continuous, closed-loop gain control needed for practical operation of large systems. The system also provides total status outputs which allow for a remote HIGH VOLTAGE ON indicator, and a HIGH VOLTAGE FAULT alarm.

Each voltage channel employs a high-efficiency switching supply with low ripple and a safe, low stored-energy output stage. Channel output is controlled by a microprocessor in the mainframe which establishes demand settings, continuously measures the output voltage (using a 12-bit ADC), compares the output with the 12-bit programmed demand, and adjusts the output to maintain constant voltage. Any channel which cannot be brought into regulation, either due to overload or channel failure, is shut down and reported by the CPU.

Voltage run-up and run-down are performed at safe rates of 1 kV/sec for 3.3 KV channels and 2 kV/sec for Series VII channels. Series VII also allows for current-limited run up at less than 2 kV/sec. Under current-limited conditions, the voltage run-up speed is set by the rate at which the load capacitance can be charged. Series VII has special algorithms to automatically allow for this mode.

The system is failsafe against erroneous voltage or current-limit demands which occur in day-to-day programming. Series VII provides for setting individual hardwired voltage and current limits, using rear panel terminals. This safeguard is in addition to the mainframe front panel vernier which sets the system voltage limits. The vernier setting establishes the maximum demand voltage of the 3.3 KV pods and sets a Series VII limit at twice this value.

Numerous safeguards and error checking subroutines are included in the HV4032A/M microprogram. The memory stores all of the system parameters (demand voltages for each channel, current limits for Series VII channels, idle-down voltages for the system and the mainframe pod complement) and is safeguarded by battery back-up. The auto-rechargeable battery guards against memory loss due to power failures of up to 24 hours, and includes fail-safe self checking of memory integrity at power up.

All pods are voltage programmable, and Series VII pods are also programmable for current limit, with separate settings for each channel in 1 μ A steps. Each Series VII pod also has a fast current trip circuit, sensitive to current surges. All pods identify themselves to the CPU and may therefore be randomly placed in the mainframe, without restriction. Placement of one or more Series VII pods in a mainframe activates special firmware to perform current limit and current monitor functions on those stations containing Series VII channels.

Series VII supplies include innovative load-protection features. An extremely fast current surge detector allows each channel to initiate a trip sequence as soon as a fault is detected. Power supply output is stopped within 50 μ sec of the sensing of the fault. This trip feature is the **first** step in the load protection sequence of Series VII. To fully protect the chamber, the energy stored in the HV cable and Series VII output filter capacitor must be dissipated. It is shunted to ground and discharged with a response time of typically less than 1 msec. Application of such a crowbar to HV protection is a first from LeCroy. Any and all Series VII channels (up to 16) can be ganged for common trip to prevent the potentially dangerous voltage imbalances which can result from the shutdown of only one channel. When configured as a daisy chain, the channel initiating the trip reports its action to the user.

For the unexpected, the HV4032A/M also includes Panic Off, allowing all channels to be shut down in less than 20 msec (full load). Local PANIC OFF is accommodated via a large illuminated front-panel button, with remote activation via a front-panel INTERLOCK connector. The trip is reported in CAMAC or TTY mode operations.

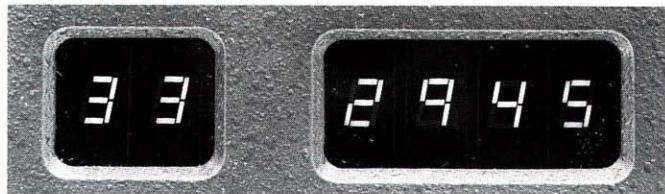


Features . . .

FAST, FLEXIBLE, INITIALIZATION AND SET-UP

Full digital control for all functions is provided locally via front panel push-buttons, and provided remotely via computer or TTY. Front panel decimal displays identify which channel is addressed for control, as well as the value of the parameter that is inserted. Channel numbers 0 through 31 identify a voltage channel. For 7 kV supplies, the odd numbered channels are omitted, and a "c" register is added to indicate current settings. Thus, with 7 kV pods in locations 1 and 2, and 3.3 kV pods in the remaining locations, the active channel numbers would be 0, 0c, 2, 2c, 4, 4c, 6, 6c, 8, 9. . . Demand voltage for the selected channel is set via each of the Channel 0 through 31 registers (except those registers assigned a current demand-value, as just described). Preset registers contain settings for groups of channels, so that all groups can be set to a common value for system initialization. This parallel load feature is active only when the HV is off.

Address 33 3.3 kV Preset Register



is used to set all 3.3 kV pods (negative and positive) to a common value. This feature is especially useful for system initialization. All channels can start out at a common value and then be trimmed individually as required. Resolution is 1 V, with a channel-to-channel accuracy of $\pm(0.1\%+1.5\text{ V})$.

Address 70 Series VII Preset Register



is used to set all 7 kV pods (negative and positive) to a common value. Resolution is 2 V, with a channel-to-channel accuracy of $\pm(0.1\%+3\text{ V})$.

Address 70c

Series VII Current Preset Register



is the register used to preset the current limit of all Series VII pods. Setting is made in 1 μA steps, with an accuracy of $\pm(5\%+5\text{ }\mu\text{A})$

Address 43

3.3 kV Idle-Down Register



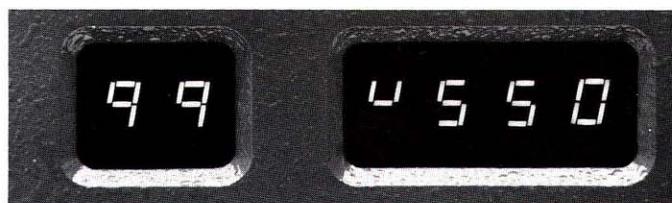
is the register used to set the idle down voltage for all 3.3 kV supplies. Entering the Idle-Down mode sets all 3.3 kV channels to this idle-down value. This feature may be used to drop all voltages during high intensity periods such as storage ring filling times. To enter, select either channel 43 or 47 and use the ZERO function. To exit, use the RESTORE function. This feature may be activated only when HV is on.

Address 47

Series VII Idle-Down Register



is the register used to set the idle-down voltage for all Series VII supplies. It functions exactly as register 43, permitting all Series VII supplies to have their own common idle-down voltage. The two idle-down registers are activated together, however, if the register for either the 3.3 kV group or the 7 kV group is set to 0, that group will remain at full voltage while the other group drops to the idle down-value set into its register. This allows the user to place only one group in the idle-down mode, if so desired.



is used for calibration and diagnosis, using procedures described in the manual. This mode may be entered via a ZERO function applied to channel 99. Returning to normal mode requires a RESTORE function on channel 99. In this mode error checking, channel failure, and digital regulation are suspended, and minimum programming values are defeated. This mode allows for the unusual application and is especially useful for system diagnosis. A \sqcup superimposed on the 1000's digit of the front panel voltage display indicates that this mode is active.

MODULAR CONSTRUCTION

The six pod models which supply the full range of voltages, currents and polarities are modular plug-in units which may be interchanged to suit the application. All six types may be used simultaneously, in any combination. Modules may be installed quickly and easily via rear panel access. The chassis may remain mounted and no cover plates need be removed.

AUTOMATIC 3.3 KV/7 KV IDENTIFIER

The internal dataway of the HV4032A/M allows pods to identify themselves. This operation functions automatically, allowing any pod to be placed in any position. When 7 kV dual channel pods are installed, their odd addresses are suppressed and used instead as current subaddresses, matching the corresponding even numbered channel address. The current address has the suffix c, and is used to store and indicate the current limit for that channel, just as the group limit is used at address 70c, shown in the photo above. On power-up, the pod complement is checked and compared to the previous configuration. Any pod stations which have been changed have their voltage demand set to zero.

CONTINUOUS MEMORY

Battery backup, continuously recharged whenever a-c power is available, protects the integrity of internal memory for 24 hours. This makes the memory immune to occasional power failures.

INTELLIGENT POWER-DOWN/POWER-UP

The microprocessor control differentiates between power failure and routine shut-off. Upon loss of a-c power, the microprocessor, with full battery backup, loads the status of the key switch into memory. A self-test bit pattern is also loaded into memory. On restoration of normal power the bit pattern is checked for integrity. A positive memory test assures that the HV4032A/M has preserved all demand voltages and current limits in memory, so that the system may be operated with full confidence. If shutdown was by user switch-off, the Model HV4032A/M stands by. If shutdown was the result of power failure at a time when HV was on, the HV4032A/M executes a controlled voltage run-up. If any stations contain Series VII pods, the ramp-up feature is overridden and the system stands by.

The register display following a power up having a positive memory test shows channel 00. If the memory test was negative the register will display either address 33 or 70, depending on which pods are installed in the mainframe. The demand voltage indication will default to the midrange value, which is also the initialization value. The preset value is entered by pressing the V button.

DIGITAL VOLTAGE SENSING

A 12-bit system ADC reads the actual output voltage or current, NOT the demand setting.

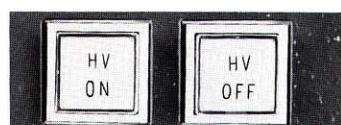
DIGITAL FEEDBACK

Voltage outputs and current limits are controlled with digital precision. The microprocessor utilizes the ADC to measure all outputs. This provides the user with continuous calibration and also identifies any channel failures. Internal programming utilizes 14 bits, corresponding to 250/500 mV for 3.3/7 kV modes.

PROGRAMMED RUN-UP/RUN-DOWN

Receipt of a HV turn on command initiates a ramp-up of all channels.

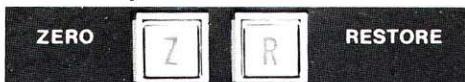
The rate is a safe 1 kV/sec for 3.3 kV supplies and 2 kV/sec for 7 kV supplies. A turn-off command ramps down similarly. Series VII supplies also permit programmed current limited run up over the range of 10 to 500 μ A. In this mode, the voltage run-up rate is determined by the value of the load capacitance, C, and the current limit, i.



$$\frac{dV}{dt} = \frac{i}{C}$$

ZERO/RESTORE

Allows any channel to be set to zero via a programmed run-down and returned to its original Demand setting. This is especially useful as a system diagnostic and as a safety feature.



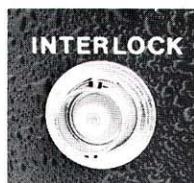
PANIC OFF

A front-panel pushbutton shuts down all supplies promptly. Protects against human error and the unexpected.



INTERLOCK

A front-panel BNC input accepts a TTL input, triggering a panic-off. Internal programming jumper allows user assignment of logic levels, allowing the input to be used as a failsafe interlock or a remote panic off.

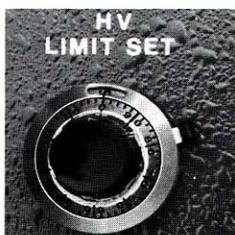


INTELLIGENT FAILURE DETECTION

The built-in ADC monitors the output of all channels. Output voltage in error by >2% of full scale, caused by an overcurrent condition, or a channel failure, is detected by digital feedback. Failures are reported by front panel indication in the local mode and to CAMAC or TTY in the remote mode.

VOLTAGE LIMIT

A front panel adjustment sets a hardware limit for all channels. The clamp point for 7 kV channels is twice that for 3.3 kV channels. When a demand voltage exceeds the limit, the CPU detects a failure, zeroes the channel, and reports the shutdown. Series VII Channels also offer a rear panel current and voltage clamp for each channel.



CURRENT LIMIT

All channels of the ± 3.3 kV supplies have fixed current limits. Each Series VII channel is separately limited in programmable $1 \mu\text{A}$ increments. The accuracy of the programming is $\pm(5 \mu\text{A} + 5\%)$.

CURRENT TRIP

A feature of Series VII pods only. Shuts down when a current surge is detected. Protects against detector damage caused by high voltage breakdown. Initiates a crowbar action. For details, see LeCroy application note AN-7.

THERMAL PROTECTION

A temperature monitor on the internal power supply shuts off the high voltage in the event of overheating. This can be the result of excessive loading, clogged fan filters, or high ambient temperatures.

INTELLIGENT DAISY-CHAIN

Up to 16 mainframes may be operated remotely. Serial Transmit and Receive lines, a Bus Request line and Grant line are used. Also, an Identifier line allows the system to differentiate between CAMAC and TTY modes. This allows for ASCII coding for TTY operation and binary coding for CAMAC operation. Binary coding greatly simplifies programming. The HV4032A system *automatically* knows which remote device is active.



SOPHISTICATED INTERACTIVE TTY OPERATION

Offers all of the features available through the front panel and more. An easy-to-understand interactive mnemonic language is used.

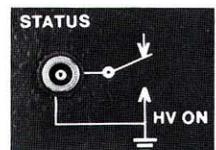
Each channel in the daisy-chain can be set, read, zeroed, and restored. Simple routines allow the preset function, turn-on, and turn-off. The system can offer a status report and print out an array of measurements of all outputs within the mainframe or within all mainframes. Channel failures are reported along with an audible alarm.



Each mainframe may be assigned a unique address. This allows commands to be referred to each chassis. Special shorthand allows the addressing to be skipped after the first reference.

STATUS OUTPUT

A front-panel Lemo output used to indicate HV present at rear connectors. May be used for personnel safety interlocks or as an independent indicator.



COMPLETE CAMAC PROGRAMMABILITY

All the operations which may be performed from either the TTY or the front panel are available through the Model 2132 CAMAC interface. A simple binary control word scheme makes programming easy. A unique RESPONSE feature may be enabled, indicating completion of each command.

MAINFRAME SPECIFICATIONS

HV4032A/M

DISPLAY

CHANNEL (register) Display: 2 flicker-free LED Decimal Digits. Indicates the channel selected corresponding to output voltage or demand shown in VOLTAGE display.

VOLTAGE (current) Display: 4 flicker-free LED Decimal Digits. Displays the measured output voltage. The demand voltage indicated when V button is depressed. The left most digit indicates C when an output current is displayed rather than a voltage.

HV ON Indicator: High intensity red lamp indicates HV ON. Illuminated when high voltage is present at rear connectors. Integral with READY indicator and PANIC OFF.

READY Indicator: High intensity yellow lamp indicates READY. Illuminated when PANIC OFF is not depressed and INTERLOCK is not disabled. Integral with HV ON indicator and PANIC OFF.

CONTROL

Voltage (current) (V)/Channel (register) (C): Two momentary pushbuttons; enables VOLTAGE or CHANNEL to be changed by INCREASE/DECREASE switch. When V is depressed, the demand voltage of the selected channel is displayed. When V is released, the measured output is displayed. Active only in the LOCAL mode. V is also used to set current limit for 7 kV pods.

Increase (▲)/Decrease (▼): Two momentary pushbuttons; increases (decreases) channel number if CHANNEL control is selected; increases (decreases) voltage of selected channel if VOLTAGE control (V) is selected. Voltage in excess of pod design is prohibited by software.

HV ON: Momentary front-panel pushbutton. Loads the demand voltages for all channels and executes a controlled-rate voltage run-up. Active only in the LOCAL mode.

HV OFF: Momentary front-panel pushbutton. Loads the zero voltages for all channels and executes a controlled-rate voltage run-down. Active only in the LOCAL mode.

ZERO (Z): A momentary pushbutton sets selected channel demand to zero. (Actual output <100 V with no load, supplying <20 μA, not a hazard to personnel.) The Z operation activates a slow controlled-rate rundown voltage of the channel selected. The demand voltage of the channel is saved in a temporary buffer. Active only in the LOCAL mode.

RESTORE (R): A momentary pushbutton; complements the Z operation; if the HV is on, a controlled-rate run-up is performed. Active only in the LOCAL mode.

LOCAL/REMOTE: A front-panel slide switch selects LOCAL control or REMOTE control. In REMOTE control the unit can distinguish between the TTY or LeCroy Model 2132 CAMAC Interface. ASCII or Binary response is offered correspondingly. In TTY operation 110 or 300 BAUD may be user-selected by internal plug option. Factory set at 300 BAUD.

MAINFRAME ADDRESS: Front-panel 16-position rotary switch used to select the unit number (of address) of a HV4032A when multiple units are tied to a TTY or a CAMAC Interface. The last HV4032A in the daisy-chain must be designated number 16.

SAFETY

PANIC OFF: Front-panel momentary pushbutton unconditionally disables all channels. Outputs decrease in ≤20 msec (1/e time for full load). Integral with HV ON and READY indicators. Trip reported to Model 2132 or TTY in REMOTE operation.

INTERLOCK: TTL compatible input with internal 4.7 kΩ pull-up resistor. Negative edge triggers a PANIC OFF. While the INTERLOCK is low, the READY indicator is extinguished and all commands will be ignored. Internal jumper option complements the disabling state of the INTERLOCK. Trip is reported in the REMOTE mode.

STATUS: Front-panel Lemo connector. Clamp-to-ground when HV is present at rear connectors. Sinks ≥35 mA; up to 32 mainframes may be daisy-chained.

Power ON/OFF: Key switch controls a-c main power. Key required to turn on unit. Rechargeable battery supplies memory power for 24 hours when main power is off or lost, recharges when a-c power is on.

Continuous Memory: Demand voltages are maintained by rechargeable batteries; capacity 24 hours when fully charged. Full recharge in ≤48 hours. System software checks the integrity of memory upon power-up.

HV LIMIT SET: Front-panel vernier sets a hardware high voltage limit. Approximate limit = (300) × (reading + 1.00) volts for HV4032A1; doubled for HV4032A7 pods. Channels are shut down when the difference between demand and actual voltage exceeds 64/128 V for 3.3 kV/7.0 kV respectively.

GENERAL

Pods/Mainframe: 8

I/O Connectors: Two multipin connectors, with front-panel retainer, provide "daisy-chain" capability. Five pairs interconnect the modules, two pairs are 20 mA current loops (transmit and receive), two pairs are used for bus control, one pair mates with LeCroy Model HVCK-14. Differentiates between CAMAC and TTY remote operation.

Packaging: 19" rack-mount chassis, 17"×28½"×6½". Side-panel slides facilitate internal access.

Voltage Required: 100-130 V, 60 Hz or
205-260 V, 50 Hz. (<750 watts at full load.)
Selected by rear-panel switch.

Maximum Output:	208 watts — all channels.
Operating Temperature:	5-40°C.
Voltage Regulation:	0.05% line; ± 0.5 V load.
Common Voltage Limit:	Mainframe Front Panel Control $0 \leq S$ (setting) ≤ 10 3.3 kV pods: $V_{max} = ((.314 \times S) + .24)$ kV Series VII pods: $V_{max} = ((.628 \times S) + .96)$ kV
HV Output Connector:	SHV (Note 1).
Ambient Humidity:	0-90% Relative humidity.

SPECIFICATIONS

High Voltage Plug-In Pods

SERIES VII SAFETY

Current Surge Detector:	One per channel. Responds to current surges of ≥ 50 μ A and risetime < 25 μ sec. Initiates fast current trip and output crowbar.
Fast Current Trip:	Shuts down supply within 50 μ sec of surge detector output. Residual energy remains on output filter capacitance and cable until output crowbar is activated. Up to 32 channels may be ganged via rear panel connector. Current trip by any one causes all to trip.
Output Crowbar:	Discharges output filter capacitance and cable capacitance by a clamp to ground through 5 k Ω .
Crowbar Response Time:	Typically < 2 msec.
Manual Voltage Limit:	One voltage programmable rear panel node per channel. Internally connected to $+15$ V via 5.6 k $\Omega \pm 5\%$. $V_{max} = 0.8 V_{node}$ kV (Note 2).
Manual Current Limit:	One voltage programmable rear panel node per channel. Internally connected to $+15$ V via 4.3 k $\Omega \pm 5\%$. $I_{max} = 50 V_{node}$ μ A. (Note 2).

Pod Designation:	HV4032A1N & HV4032A1P	HV4016A1N & HV4016A1P	HV4032A7N & HV4032A7P
Channels/Mainframe:	32 max.	16 max.	16 max.
Channels/Pod:	4	2	2
Voltage Output: for HV40**A*N for HV40**A*P (Recommended range for rated performance)	0 to -3.3 kV (Note 3) 0 to $+3.3$ kV $\geq \pm 1$ kV	0 to -3.3 kV (Note 3) 0 to $+3.3$ kV $\geq \pm 1$ kV	0 to -7 kV (Note 4) 0 to $+7$ kV $\geq \pm 1.5$ kV
Current Output/Channel: (For rated performance.)	2.5 mA max.	5 mA max.	500 μ A max.
Current Limit/Channel:	3 ± 0.3 mA Fixed. (Also limited by maximum power output. See below.)	6 ± 0.6 mA Fixed.	Programmable/channel 5-500 μ A. $\pm (5\% + 5 \mu$ A) at 25°C.
Current Limit Programming Step:	N/A	N/A	1 μ A
Current Trip:	Limit only.	Limit only.	Surges of ≥ 100 μ A in ≤ 25 μ sec.
Current Trip: Response Time:	N/A	N/A	Typically 50 μ sec.
Power Output:	6.5 W/channel max. Derate at 75 mW/ $^{\circ}$ C above 30° C ambient.	13 W per channel max. Derate at 150 mW/ $^{\circ}$ C above 30° C ambient.	3.5 W/channel max.
Current Monitor:	NO	NO	1 per channel.
Current Monitor Resolution:	—	—	1 μ A
Voltage Monitor Resolution:	1 V	1 V	2 V
Programming Step:	1 V	1 V	2 V
Voltage Regulation:	0.05% line; ± 0.5 V load.		.05% line; ± 1 V load.
Voltage Accuracy: (Channel-to-channel matching)	$\pm (0.1\% + 1.5$ V) (In HV4032A/M mainframe at 25° C after 30 min stabilization at a fixed demand voltage.)	$\pm (0.1\% + 1.5$ V) (In HV4032A/M mainframe at 25° C after 30 min stabilization at a fixed demand voltage.)	$\pm (0.1\% + 3$ V)
Ripple: (at rated load)	< 25 mV rms for > 1 kHz < 100 mV wideband (Note 5)		Typically 25 mV p-p < 50 mV rms wideband (Note 6)
Output Voltage Temperature Coefficient:	Typically 0.005%/C at 2 kV	Typically 0.005%/C at 2 kV $< 0.01\%/{\circ}C$ (+45°C ambient).	Typically 0.005%/C at 5 kV
Interchangeability:	May be used in HV4032 and HV4032A/M mainframes, but NOT HV4032P.		HV4032A only.

Notes: 1. Kings type 1064-1 connectors available at extra cost on Series VII only. Specify HV4032A7N/200 or HV4032A7P/200.

2. V_{node} = voltage applied at voltage/current limit connector.

3. Minimum non-zero demand voltage is 80V.

4. Minimum non-zero demand voltage is 160V.

5. Digital regulation updates of ± 250 mV dc ≥ 250 msec apart.

6. Digital regulation updates of ± 500 mV dc ≥ 250 msec apart.

ORDERING INFORMATION

(See Current price list.)

For any configuration, including fewer than eight pods, order the HV4032A/M Mainframe and up to eight pods, which may be mixed in any combination of the six models shown in the table on page 1. Although a mainframe may hold eight pods, any number from one to eight may be installed.

INTERFACE

To interface up to 16 mainframes to the CAMAC control system, order one Model 2132 CAMAC Interface and the appropriate cables as described below. Larger systems require one additional Model 2132 CAMAC Interface for each 16 additional mainframes.

HARDWIRED VOLTAGE AND CURRENT LIMIT FIXTURE

Model HV4032A/7X is an optional plug-in board with four trim pots used to set the voltage and current limits for the

two channels in a pod. Order one board per Series VII pod if this feature is desired.

EXTERNAL TRIP CIRCUIT CONNECTOR

Commoning of surge detector trip circuits requires that all channels which must crowbar together be linked through external wiring. Connection diagrams, supplied with the mainframe, require use of an AMP 87456-7 12-contact housing (with inserts) for each Series VII pod.

NOTE

On units received before 1 May 1981 an HVUK upgrade kit is required for Series VII features. User installation time less than 30 minutes.

ACCESSORIES

Model HVDC-14L

A data cable used to connect HV4032A chassis to one another or to the Model 2132. Includes one LeCroy HVCK-14 connector at each end. The length in feet, L, must be specified.

Model HVTC-14

A terminator for the HV4032A daisy-chain. One employed at the end opposite the controller (CAMAC or TTY). One required per daisy-chain.

Model HVTT-14

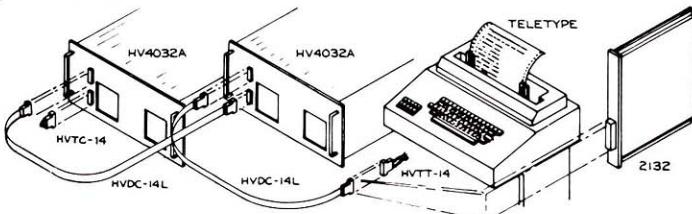
Consists of all the parts required to connect a HV4032A daisy-chain to a teletype. The HVTT-14 consists of the mating connector to the HVCK-14 with a pair of pigtailed to be connected to the teletype.

Model HVCK-14A

Connector kit to mate with the HV4032A front-panel daisy-chain connectors.

Model HVAK

Adapter kit to allow change of retention hardware to mate with a HV4032 system connector.



MODEL 2132 CAMAC INTERFACE

Model 2132 is a single-width CAMAC Interface designed for use with up to 16 of the Model HV4032A's in a daisy-chain. The unit is also compatible with the Models HV4032 and HV4032P. The unit offers 40 words of buffering on both input and output. The 2132 employs two interrupt registers, L₁ and L₂. One is designed to offer a CAMAC LAM upon non-routine phenomena such as channel failures, whereas the other is used for routine responses. Control words and responses employ a simple binary code. A control line is employed to identify the controller in use as either Model 2132 or a TTY.

SUMMARY OF CAMAC FUNCTIONS

F(0)-(A(0)+A(1))-N	Read LAM Register (R1=L1, R2=L2).
F(2)-(A(0)+A(1))-N	Read and advance input buffer (data valid if Q=1).
F(9)-A(0)-N	Clear buffers, L ₁ and L ₂ .
F(9)-A(1)-N	Clear input buffer.
F(16)-N	Write into output buffer (Q=1 if word is accepted at output buffer. Data transfer will then proceed to the HV4032A).
F(27)-(A0)-N	Test L ₁ .
F(27)-(A1)-N	Test L ₂ .
F(10)-A(0)-N	Clear L ₁ .
F(10)-A(1)-N	Clear L ₂ .
F(26)-A(0)-N	Enable L ₁ .
F(26)-A(1)-N	Enable L ₂ .
F(24)-A(0)-N	Disable L ₁ .
F(24)-A(1)-N	Disable L ₂ .
Z-S2	Clear L ₁ , clear L ₂ , clear buffers, enable L ₁ , disable L ₂ .
C-S2	Clear L ₁ , clear L ₂ , clear buffers.

Test Equipment

Model IP-2/Instapulser®

Battery-Powered, Pocket-Sized
Nanosecond Pulse Generator



FEATURES:

- Nanosecond pulses
- Replaceable Hg cell
- All silicon, potted circuit
- No controls, always ON
- Rugged, almost damage-proof
- Direct-coupled output
- 50 Ω matched output impedance
- 10 KC pulse rate
- 2 nanosecond risetime
- 1.2 volt amplitude into 50 Ω
- 5 nanosecond duration

The Model IP-2 Instapulser® —a battery-powered, pocket-sized, nanosecond pulse generator—provides a convenient source of fast trigger pulses for all kinds of fast circuit testing. Used with high speed amplifiers, discriminators, logic circuits, oscilloscopes, etc., it affords a ready source of pulses of known, stable characteristics. Extremely low current drain from the self-contained mercury battery eliminates any need for an On-Off switch. Battery life is greater than one year. All circuit components are sealed in epoxy resin for maximum ruggedness and reliability. The output is direct-coupled and reverse-terminated—drives any load of any impedance, through a cable or directly, cleanly and without reflections. In addition, the output is protected against incoming transients up to 100 volts. These output characteristics adapt the unit to almost any application requiring a fast nanosecond trigger pulse, and assure a long, safe operating life. The instapulser is a simple, inexpensive item of test equipment whose convenience and usefulness are far out of proportion to its small size.

November 1982

Model 4001 Logic ECL Probe



- Ideal for ECL signal probing
- > 150 MHz operation
- Oscilloscope probe supply compatible
- Complementary 100 Ω input stage

The Model 4001, an active scope probe, has been designed for convenient monitoring of complementary ECL signals. The 1.5 meter long 100 Ω twisted pair input cable is equipped with a female bipolar connector which matches standard single twisted pair connectors as well as multipin connectors for the flat cables of the LeCroy ECLline series of CAMAC modules.

The differential input stage has a common mode range of more than 10 V when operated with a -15 V power supply. The complementary input signal is translated into a negative single ended logic signal which can be viewed on an oscilloscope via a BNC female output connector.

SPECIFICATIONS

Model IP-2

NANOSECOND

PULSE GENERATOR

Length:	9 cm.
Diameter:	2 cm.
Weight:	65 grams.
Pulse Duration	Approximately 5 nanoseconds
Pulse Amplitude:	2.5 V into open circuit or into 50Ω load.
Output Impedance:	50Ω
Output Protection:	± 3 V DC and ± 100 V transient
Output Risetime:	Approximately 2 nanoseconds.
Battery:	6.7 volt mercury (Mallory TR-115R or equivalent).
Battery Life:	1 year.
Repetition Rate:	Approximately 10 KC.
Output Coupling:	Direct.
Output DC Level:	0.00 V DC
Output Connector:	Lemo-type female.

SPECIFICATIONS SUBJECT TO CHANGE

SPECIFICATIONS

Model 4001

LOGIC ECL PROBE

Input Impedance:	100 Ω , DC coupled.
Common Mode:	- 0.5 V to 10 V at - 15 V supply.
Maximum Differential Input Voltage:	5 V.
Input Frequency:	DC to > 150 MHz.
Differential Sensitivity:	200 MV typical.
Output Swing:	Typically - 0.3 V into 50Ω or - 0.6 V into high impedance with a - 15 V supply for ECL signals.
Rise/Falltime:	< 2 nsec for input signals with T_r and T_f < 10 nsec.
Output Connector:	BNC female.
Power Supply:	Typically 15 mA at - 15 V compatible with oscilloscope probe supply.

SPECIFICATIONS SUBJECT TO CHANGE

Monolithic Model MIQ401

4 Channel Charge Multiplexer—QMUX

- Integrate and store
- Used for ADC Systems
- Wide Dynamic Range
- High/Low Scheme
- High Resolution

The MIQ401 QMUX circuit is a 4 channel monolithic, designed to supply the integrate-and-store function required for event-based signal recording. It provides a multiplexed current source output for the four charge signals, thus allowing simple readout of many signal sources to a single ADC. The device provides two integrators per channel with sensitivity in the ratio 8 to 1. This allows a high/low encoding scheme to be used, achieving a 15-bit equivalent dynamic range.

Each input of the QMUX provides a virtual ground current input and voltage sensitive reference input. This configuration allows negative current pulses to be received or positive voltage pulses to be sampled. The quasi-differential input configuration allows the signal source ground to be used as a low frequency reference, providing rejection of hum.

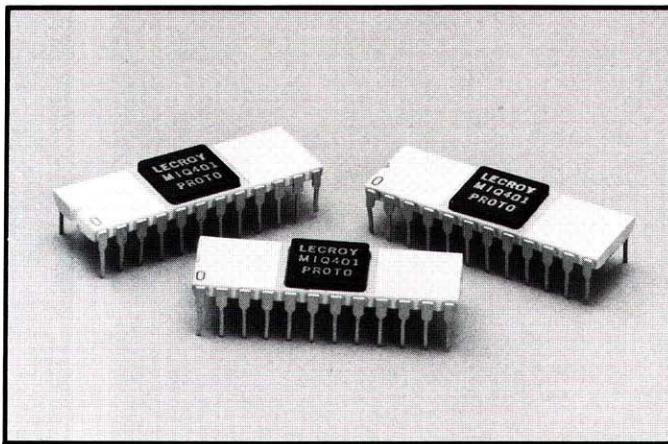
The QMUX provides a differential ECL gate input, accepting gates as short as 20 nsec. The action of the gate is to determine the integration time for the four channels. The QMUX integrates the input signals for the duration of the gate signal (application of a gate pulse narrower than the input signal is the equivalent of amplitude sampling). The integrated charge for each of the four channels is stored on internal capacitors,

one used for high-level signals and the other for low level. These two circuits are called High Range and Low Range.

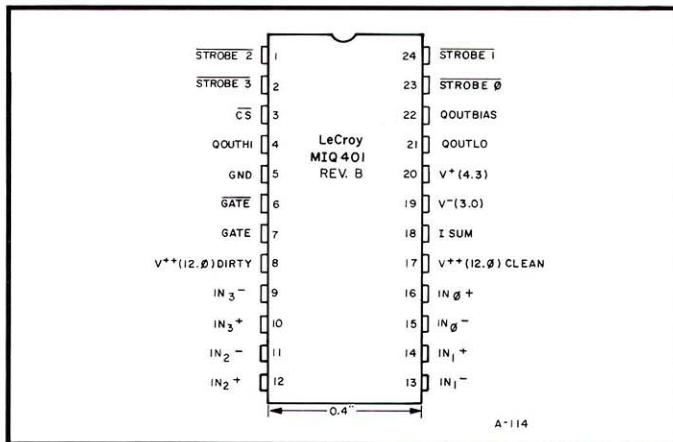
The Fast Clear allows an analog reset of the eight integrating capacitors. Within 600 nsec of a Fast Clear operation, the capacitors are cleared from full scale to within 50 fC of null. Fast clear is accomplished by applying all four readout strobes and a chip select level, i.e., clear is strobe out of all four channels at once.

Readout of the QMUX is accomplished using a Chip Enable Input and a separate readout strobe per channel. Two outputs are provided for the QMUX. These provide signals proportional to the charge received at the selected input. The High output provides 1/10 of the charge and the Low output provides 8/10 of the same signal. The maximum High linear signal is 1800 pC with noise of <50 fC. The QMUX outputs are current sources allowing many QMUX chips to be ganged to a common digitizer circuit.

To allow the signal sources to participate in the second level trigger, an ungated input sum output is provided. Because this signal, called the Current Sum output, is a current source, multiple chips may be ganged.



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Circuit Description

The equivalent circuit of the MIQ401 is shown in Figure 1. The input circuit for each channel consists of a virtual ground node called IN^- . The feedback circuit within the device maintains the input at a voltage equal to that of the IN^+ node.

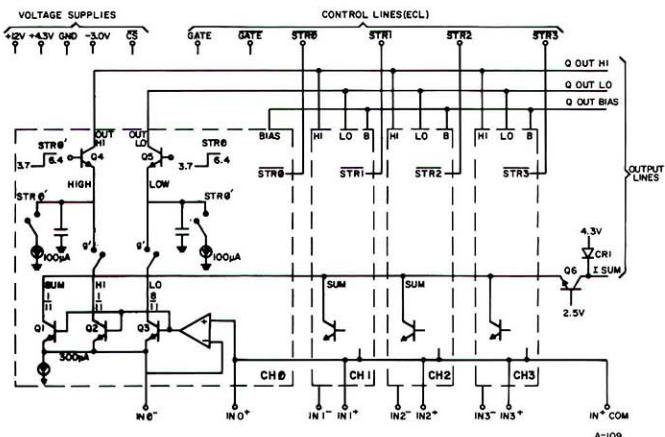


Figure 1
MIQ401 Equivalent Circuit

Notes:

1. The low impedance input bias current is cancelled by circuits internal to the chip and not shown here. For this reason less than $\pm 5\%$ of the bias current is integrated and contributes to the pedestal.
2. The gate is pictured as a switch and the gate-off state is shown.
3. The strobe current switches are shown in the off state. The voltage waveforms shown at the bases of the output transistors (Q_4, Q_5) depict a transition from hold to strobe-out-charge states.
4. Differential gate is internally buffered to each channel.
5. CS High disables all STR inputs.

The input provides great versatility. It can be used for single-ended negative inputs as shown in Figure 2. Note that the input is shown in a quasi-differential configuration so that common mode rejection of low-frequency signals is provided. The input can also be used for positive inputs (Figure 3) or differential inputs (Figure 4).

Readout of the MIQ401 is accommodated using the Chip Select and STR (strobe) inputs to successively remove the charge pulses from the eight storage capacitors. High and Low Range outputs are read out in parallel via the QOUT HI and QOUT LO outputs (Figure 5).

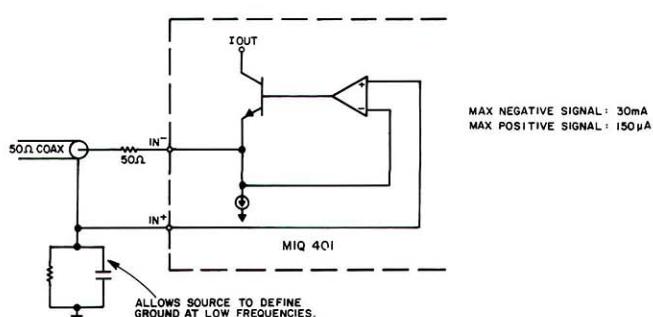


Figure 2
Single-Ended Negative Input Scheme

The readout circuit must employ an integrator such as the one shown in Figure 6. The QMUX readout circuit provides a temperature compensation output, QOUT BIAS which must be integrated and subtracted from the signal. To assure good temperature compensation, the capacitors, C_{int} , shown in Figure 6, must be well matched.

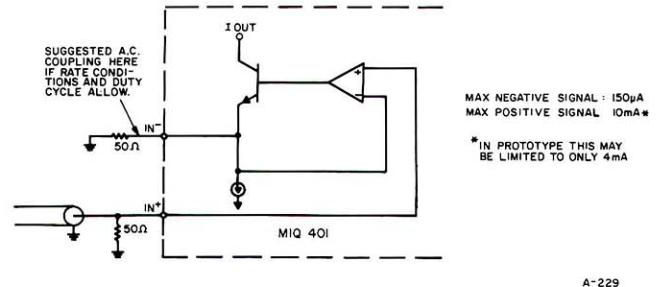


Figure 3
Single-Ended Positive Input Scheme

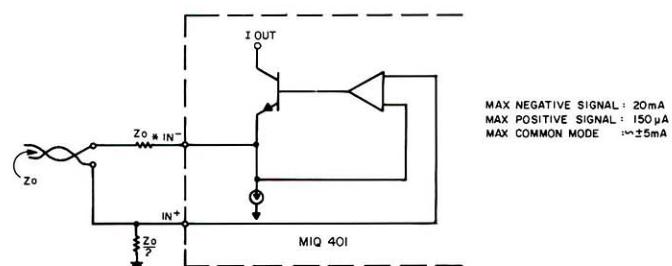


Figure 4
Differential Input Scheme

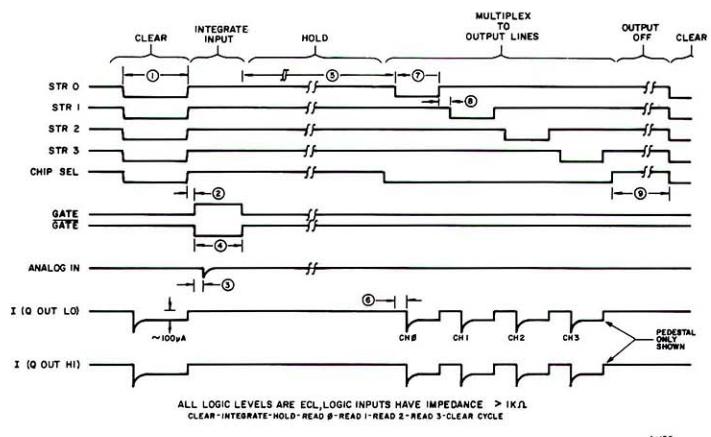


Figure 5
MIQ401 Timing Diagram

Notes:

1. Clear time for 12-bit Clear <600 nsec.
2. Clear off to Gate on time >20 nsec.
3. Gate on to leading edge of signal >10 nsec.
4. 50 nsec < gate width <2 µsec for maximum dynamic range.
5. Hold time ≥500 µsec for droop on order of .025% F.S.
6. Output current switch takes 50 nsec to turn on if only pedestal was present.
7. Output strobe time >600 nsec for 12-bit resolution.
8. Wait time between consecutive strobes >100 nsec.
9. Output off state <500 µsec. See Note 5.

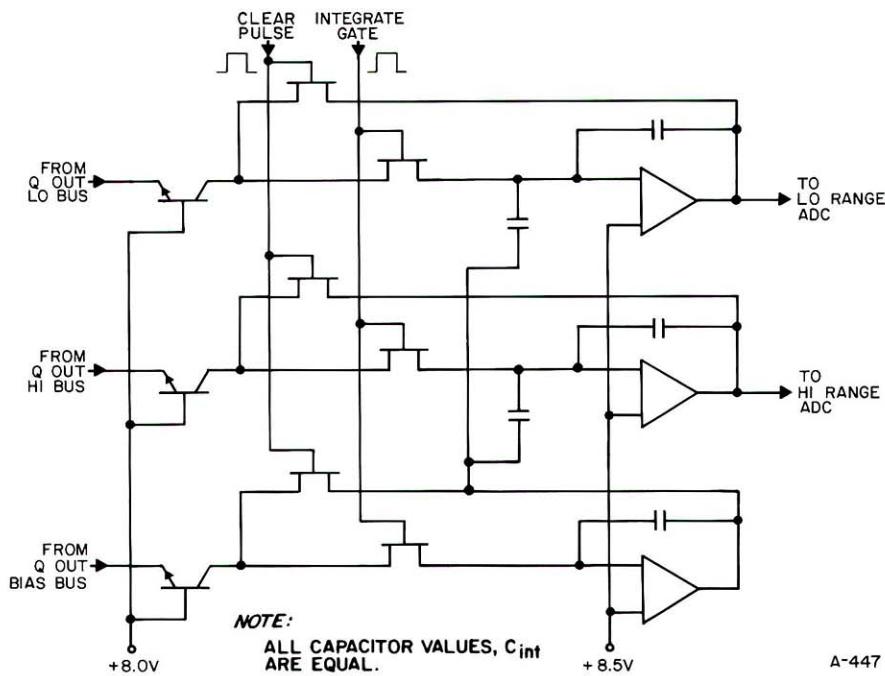


Figure 6
Sample MIQ401 Output Bus Scheme

SPECIFICATIONS

Monolithic Model MIQ401

4 CHANNEL CHARGE MULTIPLEXER – QMUX

MIQ401 PIN OUT SUMMARY

Analog Inputs:

	PIN #	NAME	DESCRIPTION	
	15	IN 0 ⁻	Negative signal input channel 0	
	13	IN 1 ⁻	Negative signal input channel 1	
	11	IN 2 ⁻	Negative signal input channel 2	
	9	IN 3 ⁻	Negative signal input channel 3	
	16	IN 0 ⁺	Positive signal input channel 0	
	14	IN 1 ⁺	Positive signal input channel 1	
	12	IN 2 ⁺	Positive signal input channel 2	
	10	IN 3 ⁺	Positive signal input channel 3	
Input Control:	7	Gate	Gate Input: defines integration interval for the four inputs.	
	6	Gate	Differential ECL	
Analog Outputs:	4	QOUT HI	High-Range charge output (1/10 of integrated input charge)	Channel being read out
	21	QOUT LO	Low-Range charge output (8/10 of integrated input charge)	Selected by STR-Lines.
	18	ISUM	Fast current sum output 1/10 of input current from each channel summed together. Open collector output. $4.5 < V_{col} < 7$ V.	
	22	QOUTB	Strobe bias	
Output Control: (all inputs ECL)	3	CS	Chip select. Enables chip for charge output. Used for multiplexing many chips to same output bus pair.	
	23	STR0	Route charge from channel 0 to output buses	
	24	STR1	Route charge from channel 1 to output buses	
	1	STR2	Route charge from channel 2 to output buses	
	2	STR3	Route charge from channel 3 to output buses	
Supply Voltages:	8	V ⁺⁺	12 V Nominal	
	17	V ⁺⁺	12 V Clean	
	20	V ⁺	4.3 V Nominal	
	5	GND		
	19	V ⁻	– 3 V Nominal	

DC CHARACTERISTICS	PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
	V ⁺⁺ Voltage Requirement	11.5	12	12.5	V	
	V ⁺ Voltage Requirement	4.2	4.3	4.4	V	
	V ⁻ Voltage Requirement	-2.8	-3	-3.2	V	
	V ⁺⁺ Current Requirement	—	10	13	mA	Static condition
	V ⁺ Current Requirement	—	20	25	mA	Static condition
	V ⁻ Current Requirement	—	30	38	mA	Static condition
	Power Dissipation		365		mW	Static condition
AC CHARACTERISTICS	PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
Signal Inputs:	Input Signal Current, Negative	—	—	30	mA	For linear operation
	Input Signal Current, Positive	—	—	100	µA	
	Reference Signal Voltage	-0.5	—	+0.5	V	
	DC Input Impedance	—	—	0.5	Ω	For 0-30 mA
	Input Offset Voltage	-2	0	+2	mV	
	Tempco of Offset Voltage	—	5	—	µV/°C	
Input Integration Gate:	Gate Duration	20	—	2000	nsec	
	Gate Internal Settling Time	—	5	10	nsec	
Charge Transfer:	Droop rate	—	—	100	fC/msec	
	Maximum Holding Charge	180	—	—	pC	
	Low Range (referred to input)					
	Maximum Holding Charge	1800	—	—	pC	
	High Range (referred to input)					
	Low Range Transfer Coefficient	0.75	—	0.8		(Δ Q _{out} LO/Δ Q _{in})
	High Range Transfer Coefficient	0.094	—	0.1		(Δ Q _{out} HI/Δ Q _{in})
	Low Range Charge Transfer Offset	—	—	20	pC	
	High Range Charge Transfer Offset	—	—	20	pC	
	Current Sum Transfer Coefficient	0.096	—	0.1		(Δ I _{isum} /Δ I _{in})
	Non-linearity (Δ Q/Q _{fit})	—	—	±(.25% + 100 fC)		Referred to output
	Clear Time/Readout Time	—	500	600	nsec	Within 50 fC of pedestal
	Noise (rms)	—	—	50	fC	Referred to output
	Interchannel Cross Talk	-60	—	—	dB	
	Temperature Coefficient			<±(50 fC + 0.1% of output Q)/°C		

SPECIFICATIONS SUBJECT TO CHANGE

TECHNICAL DATA

LeCroy

Monolithic Model MLL400 1024 (256 × 4) Bit Static Shift Register

- **High Clocking Rate:** > 250 MHz
- **Very Low Power:** 165 mW, typical
- **Low Capacitance Clock Inputs:** 5 pF, typical
- **CMOS/SOS Technology**
- **Single Power Supply Operation**

General Description

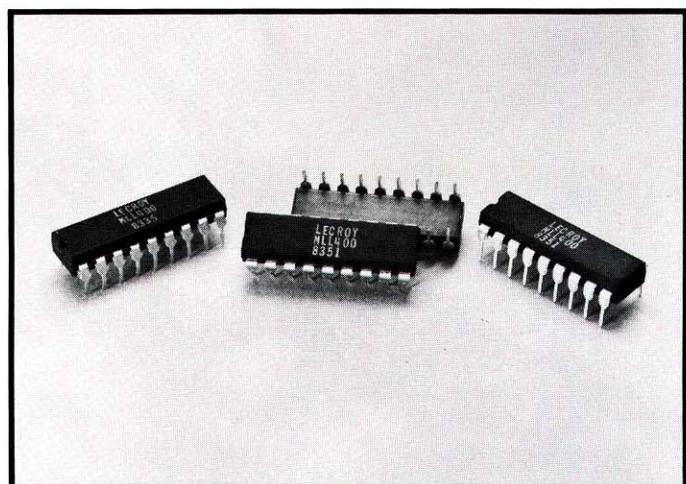
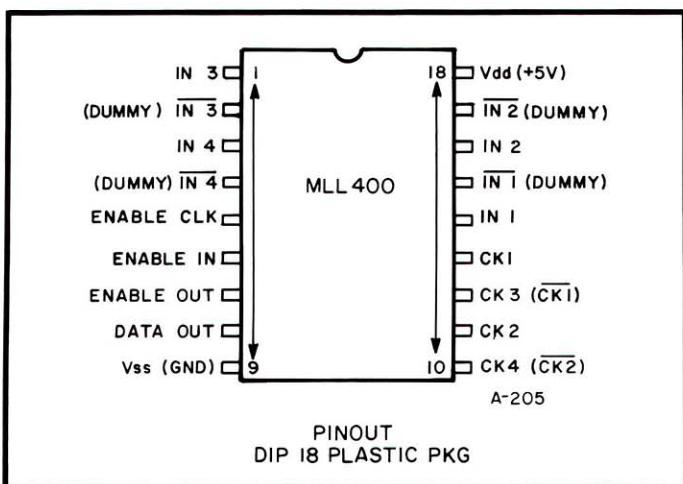
The MLL400 is a digital shift register organized as 4 channels of 256 bits each. It is ideal in applications where data must be sampled at rates to 250 MHz but can be processed at lower rates. When the clocking is stopped, data can be held indefinitely because the device is static. Readout can then occur at rates up to 80 MHz. Applications include time expansion for Time-to-Digital Conversion and as temporary storage of Flash ADC or other data.

Functional Description

The MLL400 has 4 identical channels. Each has an active input and a dummy input. The dummy has no function within the device but may be used to symmetrically load the

differential output stage of the device driving the MLL400. In applications where the MLL400 must be in close proximity to sensitive high gain circuitry, such differential drive can help eliminate feedback from the clock. The four inputs feed the four 256-bit shift registers. See Figure 1.

The shift register is clocked by an externally supplied four-phase clocking scheme. Each phase has a frequency of one fourth of the effective clocking rate. This makes generation of CMOS level clock signals feasible. All four phases are required to operate each of the 4 channels. See Figure 2.



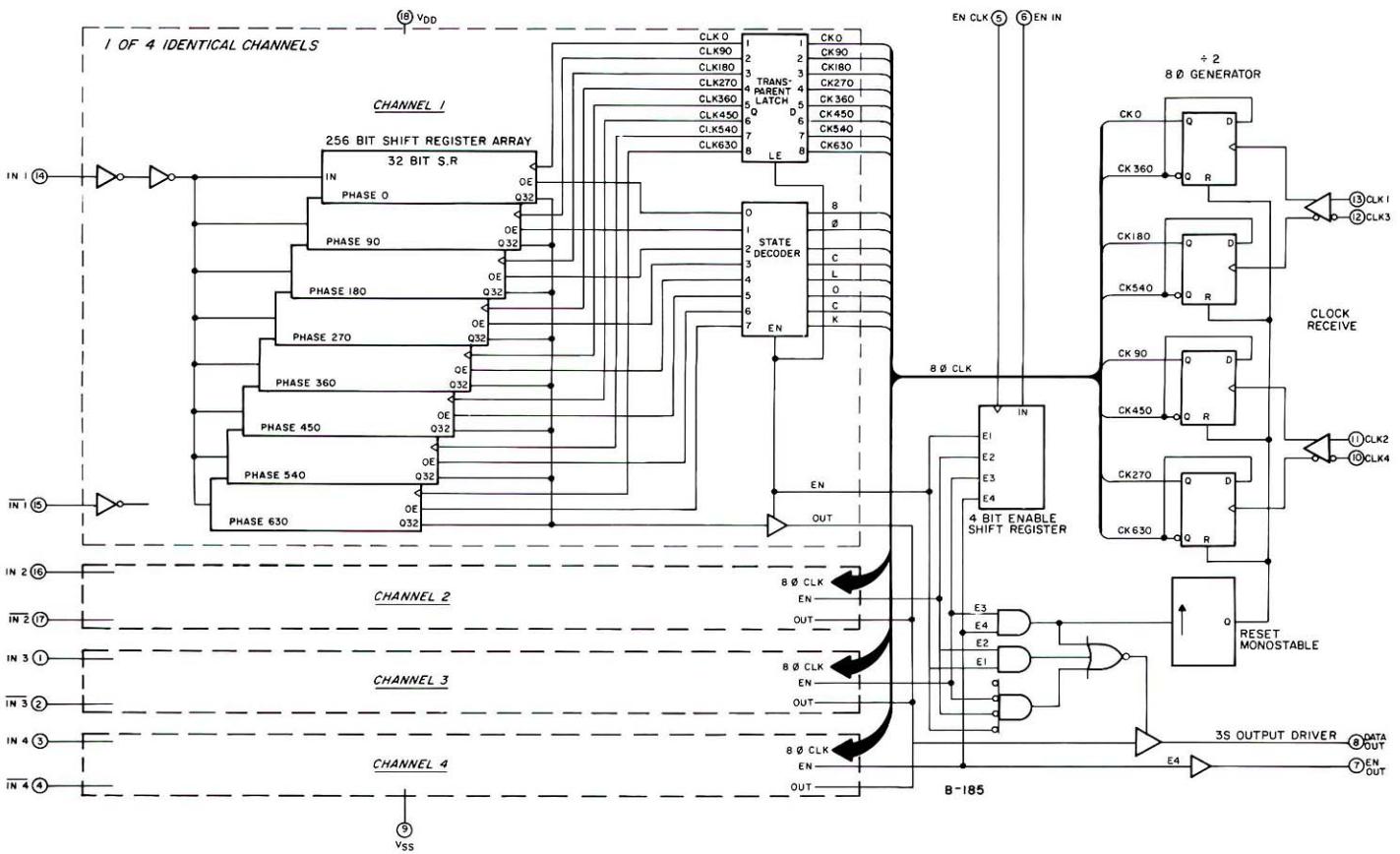


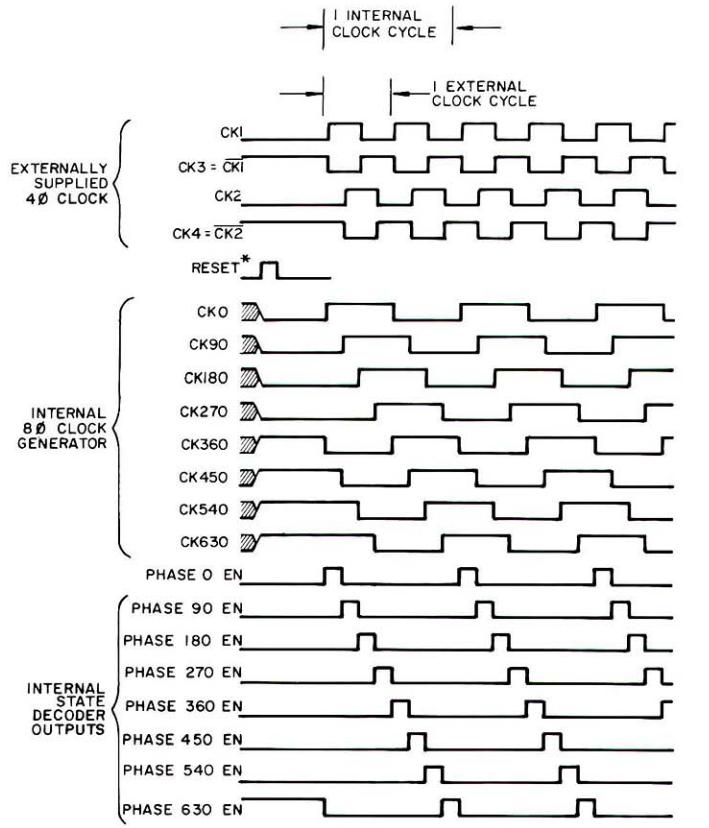
Figure 1. Functional Block Diagram

CK1 and CK3 are complementary inputs (180° out of phase), as are CK2 and CK4. These pairs should be derived from a circuit such as a transistor differential pair so that skewing is minimized. The natural progression of the clocks with respect to rising edges is as follows: CK1, CK2, CK3, CK4, CK1, etc.

The internal outputs of the shift registers are connected to a multiplexer and mode control circuit which controls the single tri-state output driver. The mode control circuit is a 4-bit shift register with its own Enable Clock, Enable-In and Enable-Out connections. These signals can be interconnected with additional MLL400s to a common control circuit to achieve sequential readout of a large array of shift registers. The bit pattern in the Enable Shift Register selects which of the four shift registers is clocked. The pattern also controls the internal multiplexer and enables or disables the output driver.

Technical Discussion

Each of the 256-bit shift register elements is composed of eight 32-bit shift registers clocked in sequence at one eighth the effective clocking rate. The four-phase clock is internally divided by two, creating one rising edge on each of eight internal clock outputs for every two cycles of the input clock. The mode control circuit gates the eight internal shift register clocks to the channels selected for shifting. The mode control circuit also gates the internal shift register clocks to the channels selected for shifting. With this structure during a readout sequence, the four-phase clocks should be held in the same state for each successive Enable Shift Register operation. See



* RESET GENERATED BY OPERATION OF
ENABLE SHIFT REGISTER, NOT SHOWN.

A-215

Figure 2

Figure 3. This state is generally not the same state as the 4 channel initialization state. If this is not done, extraneous clock edges will be generated and the data from the shift registers will not be reassembled properly. Likewise, it is also essential that the clocks be held in a proper state while the Enable Clock is operated.

The matching of propagation delays between the clocking circuits and the data input path have been optimized by insertion of appropriate gate delays in the data input path. Nonetheless, a slightly negative setup time remains. Careful attention to internal layout, a small ten-transistor cell structure and low nodal capacitances attainable with SOS technology allow a sampling accuracy of 0.6 nsec.

The single output driver is enabled or disabled via the pattern shifted into the Enable Shift Register. This facilitates a hardwire connection of the outputs of several MLL400s when used in conjunction with a common readout control circuit. (To achieve high data rates on readout, the output driver is composed of large geometry devices with sink and source capability of >100 mA. The driver is short circuit protected by internal current limiting that reduces the bias to the output drivers within 2 μ sec of detecting an overload. The circuit recovers upon removal of the overload. The output stage has a substantial propagation delay due to the large transistor size). Though the MLL400 can be clocked at an equivalent 80 MHz during readout; the >25 nsec propagation delay causes the output to become asynchronous with the four-phase clock when readout occurs beyond 40 MHz.

The inputs and outputs are similar to other CMOS logic devices operating at 5 V DC. The input threshold is typically 0.5 V_{dd} . Normal input voltage swings should

rise above 3.5 V and fall below 1.5 V. The four-phase clock inputs benefit from greater swings of V_{ss} to V_{dd} or up to 1 V beyond these rails. This is because the four-phase clocks are internally connected to complementary control inputs of transmission gates and the increased voltage swings improve the response time of the clock generation circuitry internal to the IC. Additionally, the skewing of complementary phases of the four-phase clock should be kept to a minimum to achieve maximum speed and avoid data errors, due to internal misclocking. There are input protection devices on all inputs. These clamps begin to conduct if an input is driven above V_{dd} or below V_{ss} by 1.4 V.

Operation and Mode Control

The Enable Shift Register is 4 bits long. See Figure 4. The bit position loaded from Enable-In is called E1 while the end of the register is E4 and logically equal to the level on the Enable-Out pin. The pattern in the shift register enables the internal clocks to shift each channel's shift register, enable the output driver, and reset the internal clock generator. The possible actions are detailed in the function table below.

Typical Operation Sequence

1. Enable for 4 channel shifting:
 - a. Set four-phase clocks to $CK1 = CK2 = L$, $CK3 = CK4 = H$. Hold in this state.
 - b. Using Enable Clock and Enable-In, shift in two 0s, then four 1s.

FUNCTION TABLE

State	Mode	Enable Register				Clocking Enable				Readout Mux				Out	Reset
		E1	E2	E3	E4	Ch1	Ch2	Ch3	Ch4	Ch1	Ch2	Ch3	Ch4	En	
0	Stop	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	Ch1 Readout	1	0	0	0	1	0	0	0	1	0	0	0	1	0
2	Ch2 Readout	0	1	0	0	0	1	0	0	0	1	0	0	1	0
3		1	1	0	0	1	1	0	0	1	1	0	0	0	0
4	Ch3 Readout	0	0	1	0	0	0	1	0	0	0	1	0	1	0
5		1	0	1	0	1	0	1	0	1	0	1	0	1	0
6		0	1	1	0	0	1	1	0	0	1	1	0	1	0
7		1	1	1	0	1	1	1	0	1	1	1	0	0	0
8	Ch4 Readout	0	0	0	1	0	0	0	1	0	0	0	1	0	0
9		1	0	0	1	1	0	0	1	1	0	0	1	1	0
10		0	1	0	1	0	1	0	1	0	1	0	1	1	0
11		1	1	0	1	1	1	0	1	1	1	0	1	0	0
12	Reset	0	0	1	1	0	0	1	1	0	0	1	1	0	1
13		1	0	1	1	1	0	1	1	1	0	1	1	0	0
14		0	1	1	1	0	1	1	1	0	1	1	1	0	0
15	4 Ch Write	1	1	1	1	1	1	1	1	1	1	1	1	0	0

NOTES:

1. In the table above a 0 implies disabled, 1 implies enabled.
2. In states 5, 6, 9 and 10 the positive "OR" of the data in the enabled channels appear at the output.
3. In states 3, 7, 11, 12, 13 and 14 the selected channels can be shifted in the write mode while the other channels act as storage.
4. The reset (state 12) is generated by an internal monostable of about 400 nsec. During this time the four-phase clocks must be in the following states to maintain data within the shift registers: $CK1 = CK2 = L$, $CK3 = CK4 = H$.

Figure 3

This operation resets the clock generator, enables 4 channels for shifting and disables the output driver. A 500 nsec minimum delay should be observed before proceeding to the next step to allow the internal reset monostable to time out.

2. Four-phase clocking:

The four-phase clocks may be operated to clock data into the 4 channels of the MLL400. Since the device is static the clocks may be stopped and restarted as necessary during this mode as long as the natural progression is maintained.

3. Readout enabling:

a. The four-phase clocks must be stopped and held. Note: The state in which the clocks are held must be retained through subsequent operations with the Enable shift register.

b. Using the Enable Clock and Enable-In inputs, shift four 0s and then a 1 into the Enable Shift register. After the shift in of the "1", it is advisable to leave the Enable-In input at a logical 0. The above sequence has disabled the three upper channels and held them in the storage mode and enabled channel 1 for shift and readout. The output driver is also enabled and the data at the output is valid data from the last bit of the Channel 1 shift register.

4. Channel readout:

The four-phased clocks can be advanced in their natural progression and the data output read with due

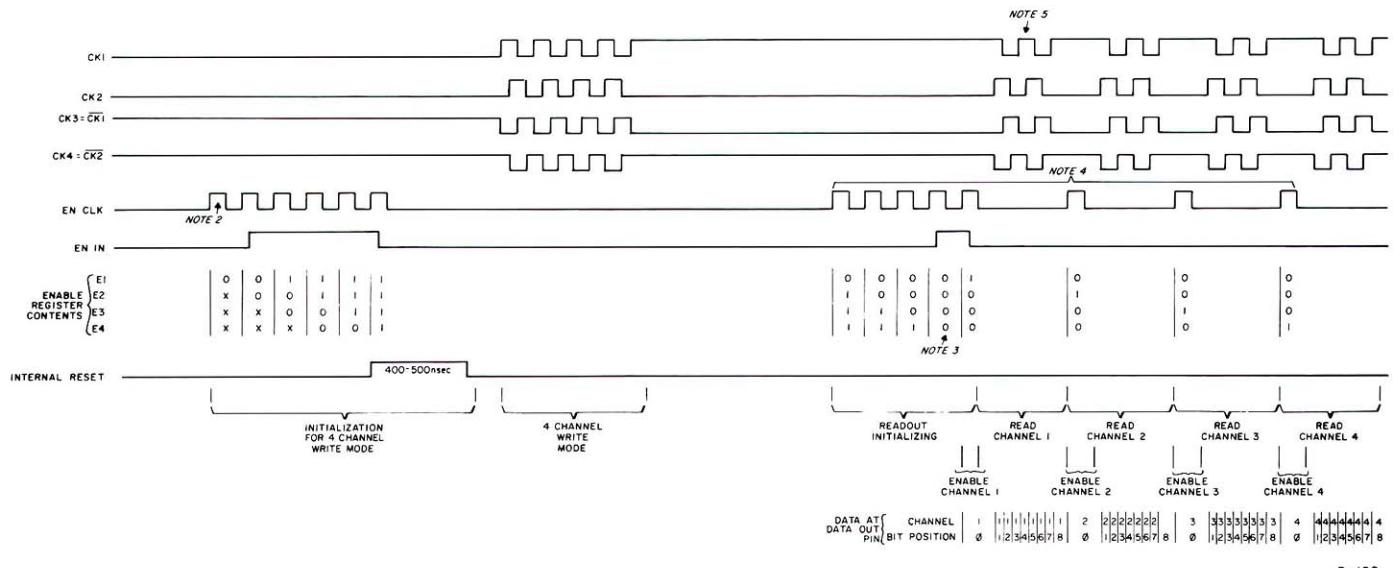
consideration to the propagation delay from the clocks' rising edges. It is important that the number of four-phase clock rising edges generated during this readout be a multiple of eight. This is necessary for the internal clock generator, otherwise, data scrambling will occur. Note: if all 256 bits are to be read out then an extra bit (a 256th bit) must also appear at the output since the first bit was available without generating a four-phase clock rising edge. When all the data of interest from channel 1 has been read out the four-phase clock should be stopped (after having input a multiple of eight rising edges) in the same state as mentioned in Step 3a above.

5. Enabling the next channel for readout:

a. With the four-phase clocks held in the correct state for changes in the Enable Shift Register, shift a 0 into the Enable shift register. This action moves the "1" entered into the Enable Register in step 3b above to the E2 position and enables channel 2 for shifting and readout. Channel 1 has become disabled, the output driver remains enabled and the data at the output is valid data from the last bit of the channel 2 Shift Register.

Readout of channel 2 can be done with the same considerations as in step 4 and then successive channels can be enabled as in step 5.

Note that at any time that the readout process of the MLL400 is to be aborted an immediate jump to step 1 will suffice. However, the previous data in the shift registers is not to be trusted.



NOTES:

- Width of clock pulses not indicative of actual widths.
- The number of φ's shifted in to the enable register must be 1 or more; 2 shown.
- This state can be skipped allowing 1 less EN clock to be generated.
- After the 4 channel write mode is completed all operation of the EN clock occurs while the four φ clocks are in the same state.
- Any multiple of 8 rising edges may be generated; 8 shown in this diagram.

Figure 4. Typical Operation Timing Diagram

SPECIFICATIONS

Model MLL400

STATIC SHIFT REGISTER

Device Ratings

Operating Temperature	0 to 70°C
Normal Operating Supply Voltage (V_{dd})	4.5 to 5.5 V
Absolute Maximum Supply Voltage without damage	-0.8 V to + 7.5 V
Power Supply Current Maximum (any Operating Mode)	65 mA

DC Parameters (at $V_{dd} - V_{ss} = 5.0$ V)	Minimum	Typical	Maximum
Input Current: H or L—Any Input			1 μ A
Input Voltage: High Level—Any Input	3.5 V		
Input Voltage: Low Level—Any Input			1.5 V
Output Voltage: High Level—Any Output	($V_{dd} - 0.5$ V)		
Output Voltage: Low Level—Any Output			0.5 V
En-Out—Low Level Output Current	1.6 mA		
Data Out Output Current; H or L	50 mA	100 mA	

AC Parameters

Four-phase clocks			
— risetime required		2 nsec	10 nsec
— minimum width, H or L	6 nsec	8 nsec	
— allowable skew CK1 to CK2 or CK2 to CK4		1 nsec*	2 nsec
Data-In Setup—Low**	- 3 nsec	- 6 nsec	- 8 nsec
Data-In Setup—High**	- 2 nsec	- 5.5 nsec	- 8 nsec
Data-In Hold—Low**	2 nsec	4 nsec	6 nsec
Data-In Hold—High**	3 nsec	5 nsec	8 nsec
Data-Out propagation delay from four-phase CK edge	25 nsec	30 nsec	40 nsec
Data-Out disable time from En-CK edge			50 nsec
Data-Out enable time from En-CK edge			60 nsec
En-In Setup		10 nsec	5 nsec
En-In Hold		0 nsec	
En-CK minimum width, H or L	15 nsec		
En-Out Propagation Delays from En-CK	3 nsec	12 nsec	20 nsec
Input Capacitance; Any Input		5 pF	10 pF

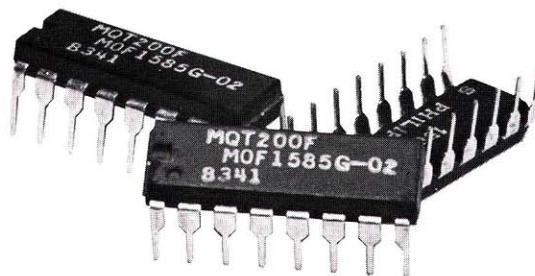
* <1 nsec skew allowed for clocking frequencies >150 MHz.

** Setup and Hold times are measured in the conventional sense. That is moving a single transition of the Data Input with respect to a specific edge of the four-phase clock. When narrow Data Input pulses occur the pulse is generally accepted if the setup time is met.

SPECIFICATIONS SUBJECT TO CHANGE

Monolithic Model MQT200F Charge-to-Time Converter

- Current integrating
- Programmable sensitivity
- Quasi-differential input
- Monolithic design



The LeCroy MQT200F is a monolithic charge-to-time converter circuit. It is intended for use as the front end of a current-integrating Wikenson ADC. It can be used for 10-bit operation with a conversion time of $2.5 \mu\text{sec}$; however, similar performance can be achieved with slower conversion rates. It is ideal for those applications where exceptionally high packaging density is required. The MQT200F offers maximum flexibility while requiring a minimum of support components.

The MQT200F has a direct-coupled virtual-ground (low impedance) input, accepting fast 0 to -30 mA current pulses. A Gate signal enables the input causing it to integrate the analog signal at the input for the duration of the GATE. The charge resulting from this integration is stored on an external capacitor. The time duration required for this charge to be removed by a reference current is proportional to the input charge. A $T^2 L$ Output of this duration is provided. Internal opening and closing time of the Gate is less than 5 nsec with normal gate drive, and recommended gate duration is 25 to 500 nsec. An example of the typical operation sequence is shown in Figure 1.

The full scale output duration may be externally programmed over a wide range with little change in operating characteristics, but the specifications are shown optimized for a full scale output time of $2.5 \mu\text{sec}$.

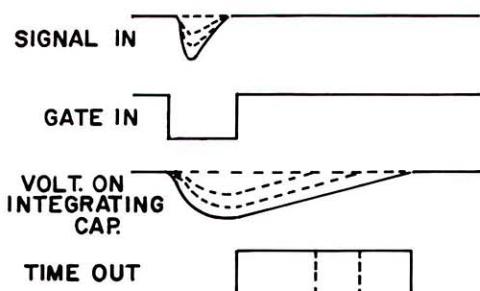


Figure 1

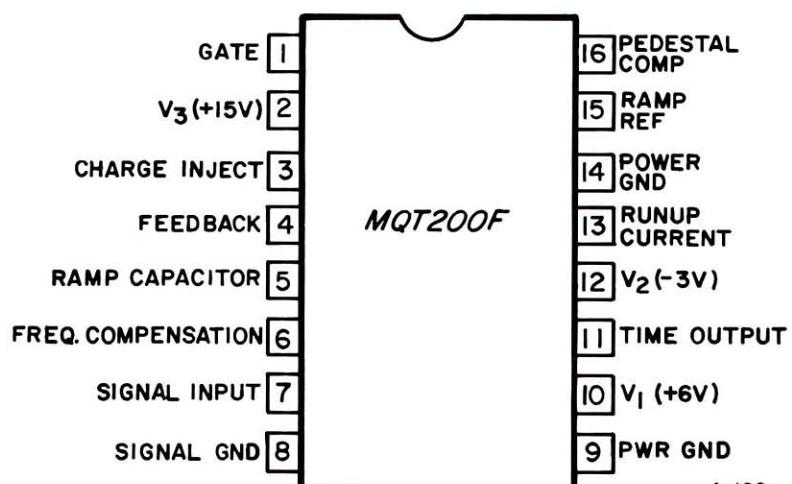


Figure 2

SPECIFICATIONS

Model MQT200F

CHARGE-TO-TIME CONVERTER

DC CHARACTERISTICS

Parameter	Min.	Nom.	Max.	Units	Comments
V ₁ voltage Requirement	+ 5.8	+ 6	+ 6.2	V	
V ₂ Voltage Requirement	- 2.8	- 3.0	- 3.2	V	
V ₃ Voltage Requirement	+ 14.5	+ 15	+ 15.5	V	
V ₁ Current Requirement	—	—	12	mA	Static Condition
V ₂ Current Requirement	—	—	14	mA	Static Condition
V ₃ Current Requirement	—	—	3	mA	Static Condition
Power Dissipation	—	—	166	mW	Static Condition

INPUT REQUIREMENTS AND PERFORMANCE CHARACTERISTICS*

Parameter	Min.	Typ.	Max.	Units	Comments
Input Signal, Negative	—	—	— 30	mA	
Input Signal, Positive	—	—	100	μ A	May be extended (see text)
Input Impedance	—	0.05	0.15	Ω	0 to — 30 mA DC
Input Offset Voltage	— 3	0	+ 3	mV	
Temp. Coefficient of above	—	0.08	0.20	mV/ $^{\circ}$ C	
Full-Scale Charge	—	256	1024	pC	Determined by value of Ramp Capacitor
Gate Duration	25	—	500	nsec	
Gate Amplitude—isolate	7.3	7.5	8.0	V	
Gate Amplitude—integrate	4.8	5.0	5.2	V	
Gate Open/Close Time	—	—	5	nsec	Gate must precede input by at least 5 nsec
Program Current	10	100	250	μ A	(V_G/R_G) See Figure 3
Non-linearity	\pm 0.25 (1 + reading/full scale)			pC	Best straight line
Noise	—	0.075	0.25	pC(rms)	With 50 nsec gate, 100 Ω source (i.e., 50 Ω series termination plus 50 Ω cable)

*At recommended operating voltage and 25 $^{\circ}$ C ambient temperature unless otherwise noted.

SPECIFICATIONS SUBJECT TO CHANGE

PIN ASSIGNMENTS (See Figure 2)

Pin #	Description	Comments
1	Gate Input	Direct-coupled. Input impedance greater than 5 kΩ. Logic States: Isolate 7.3-8.0 V, Integrate 4.8-5.2 V.
2	V ₃	+ 15 V ± 500 mV.
3	Charge Inject	Connect a 3-18 pF capacitor between Pin 1 and Pin 3 to adjust offset. (Dependent on amplitude of gate signal. See Text.)
4	Feedback	Tie to Pin 7 (Provides the required feedback for the input amplifier.)
5	Ramp Capacitor	Requires 33 pF to V ₃ for 256 pC Full Scale (increasing to 200 pF for 1024 pC full scale).
6	Freq. Compensation	Requires 3-18 pF trimmer and series 30 Ω resistor to signal ground. Adjust trimmer for minimum perturbation on Pin 7.
7	Signal Input	Virtual ground. Signal should follow gate opening by more than 5 nsec. Should be series-terminated for proper impedance match. Input impedance 50 mΩ nominal. Higher for slew rates exceeding 2 mA/nsec.
8	Signal Ground	Voltage reference for the input amplifier. Normally connected to printed circuit ground plane, but may be used for quasi-differential input mode (see text).
9	Power Ground	Connect to printed ground plane.
10	V ₁	+ 6 V ± 200 mV.
11	Time output	Open collector T ² L, requires external pull-up resistor. Normally low. (max sink 2.5 mA). Trailing edge response time ≥ 70 nsec (decreases with an increase in programming current).
12	V ₂	- 3 V ± 200 mV.
13	Runup Current	Runup ramp current typically 100 μA (see text).
14	Power Ground	Connect to printed circuit ground plane.
15	Ramp Ref	Used as reference for fast clearing of ramp.
16	Pedestal Compensation	Used to compensate time output dependence on gate width.

APPLICATION HINTS(See Figure 3)

Layout Guidelines

For the purpose of prototyping and evaluation, a test board with a minimum of support circuitry may be needed. Attached is a schematic suggested for a "test board." Continuous ground-plane construction should be used and lead lengths kept to a minimum. The MQT200F is powered by +6, -3, and +15 V supplies. All three power supply voltages and all reference levels should be bypassed to ground with high-frequency capacitors. If multiple channels are used on a circuit board, each supply should be decoupled by a separate series choke with a large value capacitor to ground. In addition, one or more references are employed to program the rundown current. Because of the sensitivity of gain to these voltages, separate supplies should be used.

Programming the Runup Current

The gain (output time vs. input charge) of the MQT200F is determined by the Runup Current. Because the Program Current input (Pin 13) is a 0 V referenced virtual ground, the current is most easily generated by connecting an appropriate stable resistor (R_G) to a stable positive voltage (V_G). The test

and recommended operating conditions, optimized for fast conversion, use a full scale charge of 256 pC and a Program Current of 100 μA. This will provide 2.56 μsec (256 pC/100 μA) of usable output time. Gain therefore is 10 nsec/pC (1 count per pC if a 100 MHz gated digital counter is used). Reducing the Program Current will proportionally increase the full scale output time duration. Note: A 100 MHz clock is used as an example but requires a stable pickoff on the Time Output because of the output trailing edge response time of 70 nsec.

When the value of Runup Current used is in excess of 100 μA, a gate width dependent pedestal will result. This can be cancelled by injecting an equal but negative DC bias current into the Signal Input (Pin 7). This is most easily accomplished by connecting an appropriate stable resistor (R_B) to a negative voltage (V_B) on schematic.

Digital Processing

The time output of the MQT200F is proportional in duration to the total charge input. The beginning of the valid time output occurs after the trailing edge of the gate signal. It is recommended that the time-to-digital conversion begin at approximately 5% of the

full scale time after the leading edge of the gate. The Charge Inject can then be set (with no input signal) to provide a near zero but positive Pedestal. (See Pedestal Adjust below).

Converting the time output to digital form is most easily accomplished by gating a stable oscillator with the MQT200F output, and counting the result with a digital counter. Fast conversion requires a fast counter (e.g., 100 MHz provides 8 bits in 2.54 μ sec) but if speed is not important, a longer full scale conversion time makes the counting circuit simpler. Alternatively, a time-to-digital converter (TDC) may be used.

Pedestal Adjust (Charge Inject and Pedestal Compensation)

Pedestal in the MQT200F may be adjusted by means of an external trimmer capacitor between pins 1 and 3, which injects charge (equal to the value of the trimmer times the gate amplitude) into the ramp capacitor at the leading edge of the gate. Pedestal charge should be just enough to ensure low end linearity. It is normally set at 2% to 5% of full scale charge. It can be digitally subtracted by delaying the clock start time. A gate width dependent pedestal term is also present which can be minimized by proper adjustment of the Pedestal Compensation adjust (Pin 16). Set it (see Figure 3) so there is no change in pedestal for narrow or wide gates. If gates are narrow (< 200 nsec) and fixed width, Pin 16 can be left open.

Gate Input Driver Requirements

The gate input (Pin 1) has a resistance of about 5 k Ω in parallel with 5 pF plus the pedestal adjustment capacitor (up to 8 pF). Gate rise and falltimes should be less than 3 nsec to assure optimum stability of the effective gate width. Gate amplitude should be about 2.5 V and be stable to assure stable injected charge. Sufficiently large and fast input pulses may penetrate the "isolate" gate of the MQT200F and cause spurious outputs. The amplitude level at which this occurs is strongly dependent on the source impedance of the gate driver, the quiescent voltage level of the gate, and the risetime of the input pulse. To minimize punchthrough, the gate should be driven from a low-impedance source such as an emitter follower or (in a system) a low-impedance stripline (50 Ω or less) and the quiescent level of the gate should be set on the high side (+ 7.5 to 8 V). If careful attention is paid to minimizing gate source impedance (including lead inductance), punchthrough should not occur for inputs of greater than 4 nsec risetime up to -3 V amplitude.

Differential Inputs

The MQT200F is basically a single-ended input device. Nevertheless, a quasi-differential input mode is provided that may aid in suppressing low-frequency (<1 kHz) common mode pick-up in some applications. This is accomplished by bringing out the reference pin for the input amplifier separately, so that it may be separately grounded or connected to the shield of the input coaxial cable or the positive side of a twisted pair. The common mode range in this configuration is limited to a few hundred mV. The proper use of this input can be seen in Figure 3.

Input Pulse Shape

The MQT200F is designed for operation with normal photomultiplier anode pulses and pulses of similar shape. Its linear range extends in the negative direction to 30 mA, but in the positive direction to only about 100 μ A. This limitation in the positive direction is imposed by the desire to minimize the front-end standing current, which in turn minimizes output pedestal dependence on gate width. If the input pulse is entirely negative, as is the case with unshaped standard PM pulses, the limited positive range is of no consequence. However, if the input pulse is coupled via a small capacitor or a pulse transformer, the resulting differentiation produces a positive overshoot on the trailing edge of the pulse which may exceed the positive linear range. This will result in a nonlinear response. For best linearity, differentiation of the input pulse should be avoided. Where this is not possible, the linear range in the positive direction can be extended by standing additional current in the input circuit by means of a resistor from the signal input (Pin 7) to a stable negative supply voltage. This additional current is integrated during the gate and will increase both the pedestal and the dependence of pedestal on the gate width. (For example, standing an additional 1 mA will allow linear operation with overshoots up to 50 mV, in a 50 Ω system, but will add 1 pC of pedestal per nsec of gate width which will cause a reduction in the pedestal stability and limits the useful range of the device). Except for extremely fast pulses, the impedance of the signal input is very low. If however, the input pulses have a rise or falltime in excess of 2 mA/nsec, it may be necessary to add about 10pF from the signal input to ground. This will effectively perform a short term integration, holding the change until the input can respond.

Fast Clear

If a fast clear is necessary, an FET can be located across the ramp and ramp reference. It should be held in its low impedance state from the time at which a Clear is asserted to the leading edge of the gate, then released fast and held in its high impedance state until the next clear.

Integrate and Hold

Under limited conditions, the MQT200F can be used as an integrate and hold circuit. This is accomplished by using the fast clear described above and reducing the Ramp Current to 1 μ amp. The ramp voltage (Pin 5) is then monitored with a high impedance (> 10 M Ω), low leakage (< 1 μ A), fast (< 10 μ sec rise and transfer time) voltage buffer or FET. With a total of 200 pF on Pin 1 (1024 pC full scale), the voltage will have a quiescent value of about 11 V and will go negative about 4 mV/pC (approximately 4.1 volts total). The droop will be about 1% per 10 μ sec, depending on the external components used, requiring the next stage to be relatively fast.

Time Output

Under certain loading conditions this output may have a low level oscillation on its baseline. The amplitude of the oscillation is smaller than T²L levels and should not cause a problem. If necessary, some integrating may be used to smooth the falltime. The

70-80 nsec trailing edge will require that a circuit with a stable threshold be used if high accuracy of the time interval is required for high speed conversion.

Power on Sequence

Ideally all three supplies (+ 15 V, + 6 V, - 3 V) should be applied simultaneously. However, due to different

charging times associated with the power supply filter capacitors, it is likely that one supply might lead the other two. This might cause a temporary latch up condition in the MQT200F. The two diodes shown in Figure 3 should prevent this latch up from occurring. For PC boards containing multiple channels, only one pair of diodes is required per board.

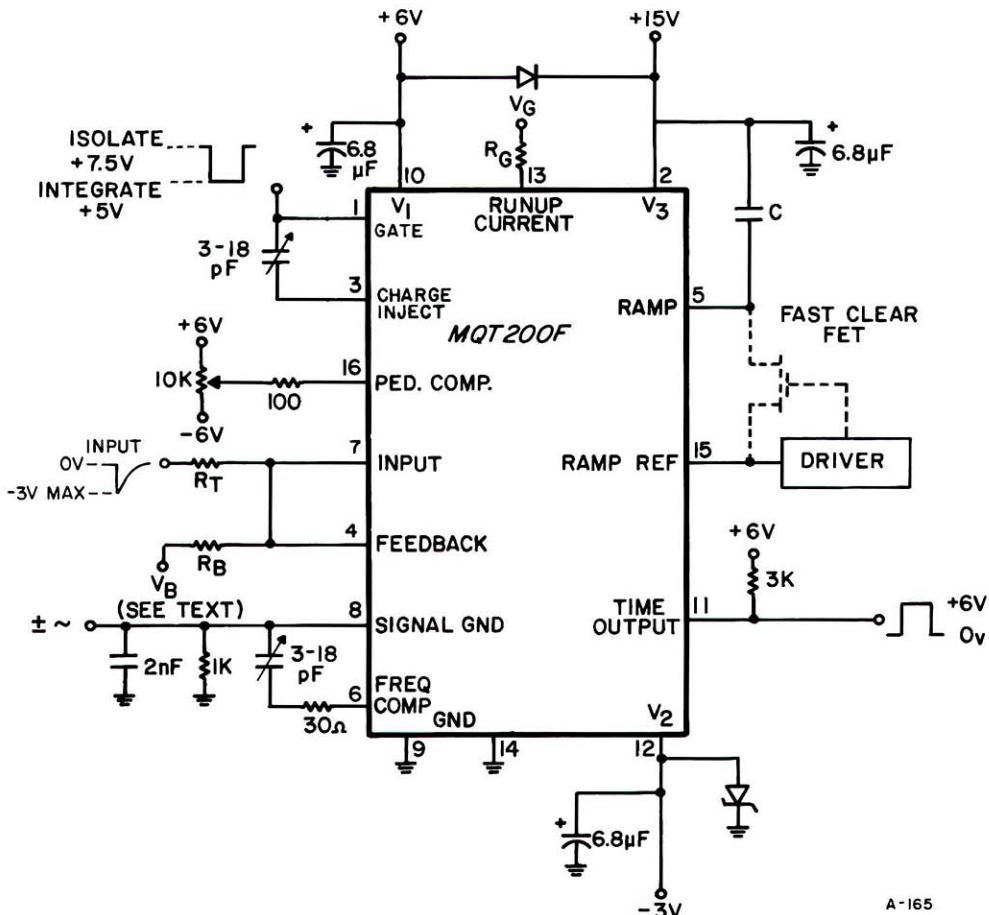


Figure 3

R_T Termination Resistor: $50\ \Omega$ for $50\ \Omega$ cable.

R_B Bias Resistor: R_B selected to cancel Program Current. Omit R_B and V_B for program currents less than $100\ \mu A$.

V_B Bias Voltage: V_B more negative than $-6\ V$.

R_G Gain Resistor: R_G selected to generate Runup Current = V_G/R_G .

V_G Gain Voltage: V_G greater than $+6\ V$.

Omit Pedestal Comp for narrow, fixed gate operation (leave pin 16 open).

Tie pin 8 to ground, omitting 1 kΩ resistor and 2 nF capacitor for non-quasi-differential operation.

Select Ramp Capacitor and program current from table below for optimum full scale charge and full scale output time.

FULL SCALE INPUT Q (pC)	RAMP CAPACITOR (pF)	FULL SCALE OUTPUT TIME (μsec)	PROGRAM CURRENT (μA)
256	33	2.56	100
1024	200	10.24	100
1024	200	102.4	10

TECHNICAL DATA

LeCroy

Monolithic Model MVL407 Quad Ultrafast Voltage Comparator

- Low cost
- 400 MHz operation
- 4 Comparators/DIP
- Less than 1 nsec response time
- 2.5 nsec propagation delay
- Built-in 3.5 mV hysteresis
- 50 Ω line drive capability
- 105 mW/channel typical power dissipation
- Complementary ECL outputs

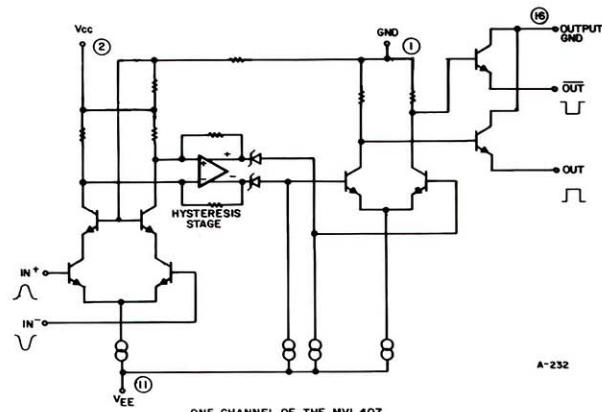
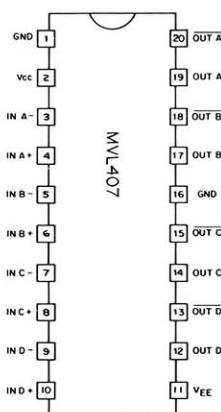
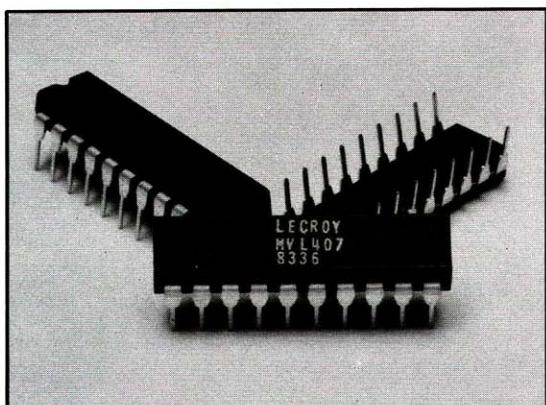
The MVL407 is a quad voltage comparator designed for applications in which ultra high speed and accurate timing are most important. The device is manufactured using a state-of-the-art high speed bipolar process which results in an extremely short (2.5 nsec) propagation delay with operation at speeds in excess of 400 MHz.

Each channel provides differential inputs and complementary outputs compatible with the ECL logic family. The outputs can drive 50 Ω loads or 100 Ω twisted pair directly.

The MVL407 incorporates a unique hysteresis feature for exceptionally clean operation. When the comparator changes state, an internal differential input offset of about 3.5 mV is generated. The positive feedback drives the device quickly through its switching region, greatly reducing the possibility of oscillation or output chatter with small or slowly changing inputs.

The propagation delay is typically 2.5 nsec and changes by only 100 psec for 5 to 100 mV range of overdrive. This very low delay variation makes the MVL407 extremely useful in critical timing applications.

For evaluation and for prototyping purposes, the Model MVL407PK is recommended. It consists of a single MVL407 mounted on a circuit board. Space is provided on the board for user prototyping circuitry. The power and reference voltage are supplied to the MVL407 via a wire pigtail.



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SPECIFICATIONS

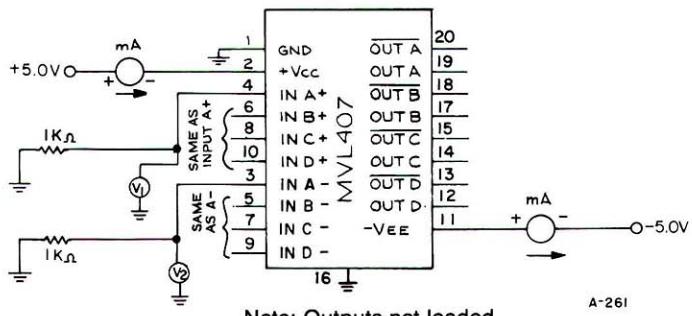
Model MVL407

QUAD ULTRAFAST VOLTAGE COMPARATOR

MAXIMUM RATINGS (See Note 5)	Positive Supply Voltage	+ 6 V					
	Negative Supply Voltage	- 6 V					
	Input Voltage	± 4 V					
	Differential Input Voltage	± 4 V					
	Output Current	30 mA (single output)					
	Power Dissipation	800 mW					
	Operating Temperature	- 20° C to + 70° C					
ELECTRICAL CHARACTERISTICS (See Note 5)	Symbol	Parameter	Min	Typ	Max	Units	Comments
	I_{OS}	Input offset current	- 0.5	± 0.05	+ 0.5	μA	See Fig. 1
	$\Delta I_{OS}/\Delta T$	Average TC of I_{OS}	- 1.5	± 0.5	+ 1.5	$nA/\text{°C}$	
	I_B	Input bias current	2.5	4.0	7.0	μA	See Fig. 1
	$\Delta I_B/\Delta T$	Average TC of I_B	- 20	11	+ 20	$nA/\text{°C}$	
	R_{in}	Input resistance	20	30	-	$K\Omega$	
	C_{in}	Input capacitance	1.2	1.6	2.1	pF	
	V_{cm}	Input voltage range	- 2.0		1.7	V	See Figs. 2, 14
	V_{T+}	Threshold for $\bar{OUT} \rightarrow OUT$	- 3.0	+ 1.0	+ 5.0	mV	
	V_{T-}	Threshold for $OUT \rightarrow \bar{OUT}$	- 6.6	- 2.6	- 1.4	mV	
	$\Delta V_{T\pm}/\Delta T$	Average TC of $V_{T\pm}$	- 10	± 5	10	$\mu V/\text{°C}$	See Fig. 4, Note 4
	V_H	Hysteresis voltage	3.4	3.6	4.0	mV	
	V_{OL}	Output low level	- 1.7	- 1.62	- 1.52	V	
	V_{OH}	Output high level	- 0.85	- 0.78	- 0.75	V	
	$\Delta V_{OH}/\Delta T$	Average TC of V_{OH}	-	1.5	-	$mV/\text{°C}$	
	$\Delta V_{OL}/\Delta T$	Average TC of V_{OL}	-	0.6	-	$mV/\text{°C}$	
SWITCHING CHARACTERISTICS (See Note 5)	I^+	Positive supply current	-	43	60	mA	4 channels Without output pulldown resistors See Fig. 1
	I^-	Negative supply current	-	41	60	mA	
	PD	Power dissipation	-	420	520	mW	
INTERCHANNEL MATCHING (See Note 5)	Symbol	Parameter	Min	Typ	Max	Unit	Comments
	ΔV_H	Hysteresis		± 0.25		mV	
	$\Delta V_{T\pm}$	Threshold voltage		± 1.25		mV	
	ΔI_{OS}	Input offset current		± 50		nA	
	Δt_{pd}	Propagation delay		± 125		psec	
		Cross talk—any channel	-	-	-	dB	Unobservable Note 1

Interchannel matching refers to the variation between the channels on any single chip.

- NOTES:**
1. Cross talk is measured at a threshold of 2 mV.
 2. Propagation delays are defined to be the delays between a positive going input and an output transition of either polarity. The input overdrive is 50 mV with the threshold set at 0 mV.
 3. Double pulse resolution is defined as the minimum pulse pair spacing at which the MVL407 responds to the second pulse of the pair. The output levels of the second pulse must cross V_{OH} and V_{OL} . See Figure 5.
 4. See Application Hints.
 5. All measurements at 25° C, $V_{cc} = + 5.0$ V, $V_{EE} = - 5.0$ V.



$$I_B = \frac{1}{2} \frac{V_1 + V_2}{1 \text{ K}\Omega} \quad I_{OS} = \frac{V_1 - V_2}{1 \text{ K}\Omega}$$

Figure 1

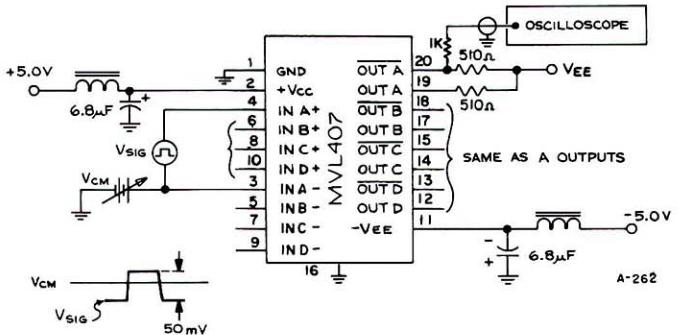
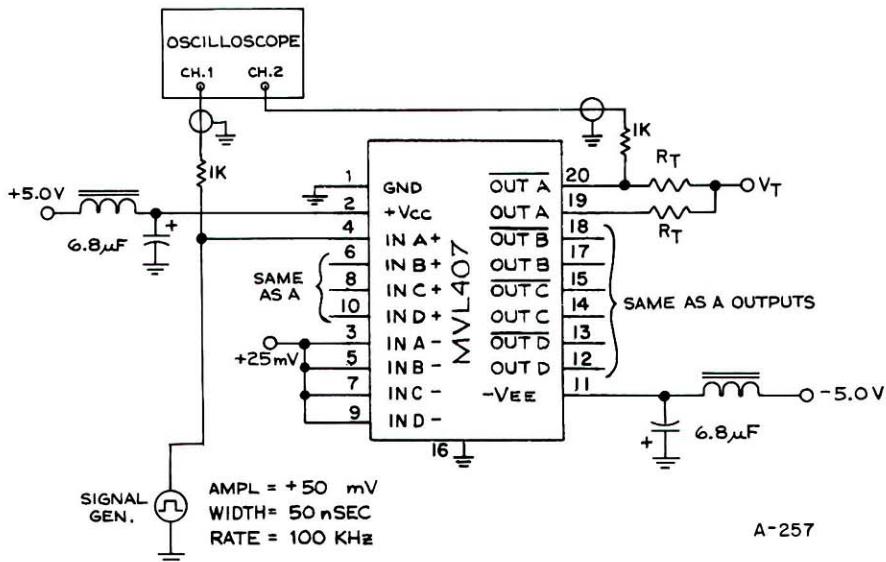
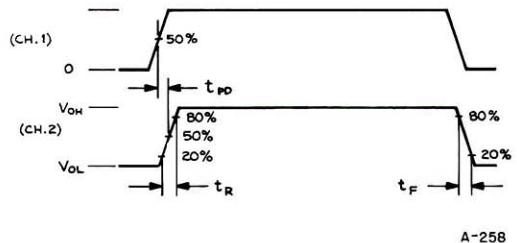


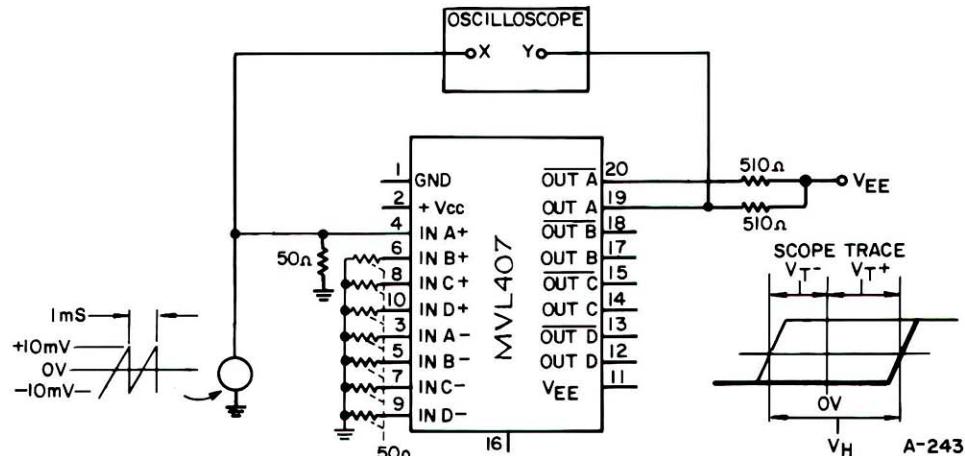
Figure 2



A-257



A-258



A-243

Figure 4

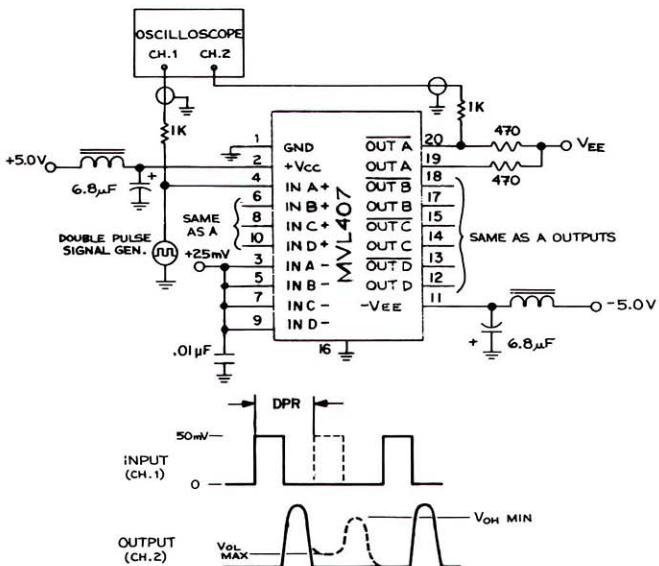
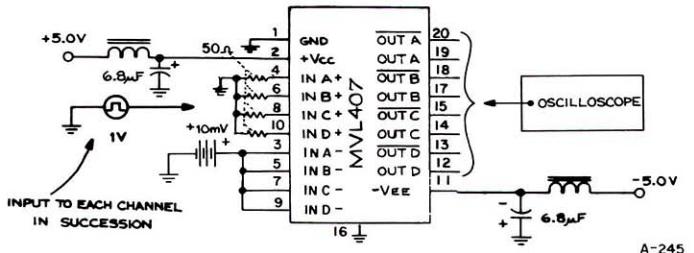


Figure 5

Note: All outputs loaded with 510 ohms to V_{EE}.



Drive one channel only. If any other channel triggers, cross talk spec is not met.

Figure 6

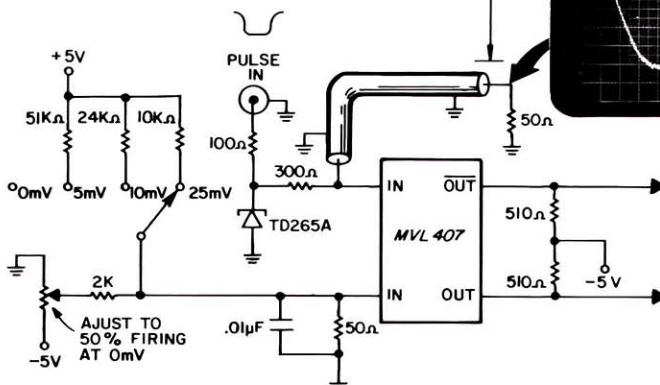


Figure 7

APPLICATION HINTS

Interconnection Techniques

To achieve optimum performance, high speed circuits require some special layout precautions. For a good low inductance ground current return path, a ground plane must be used. The input impedance should be as low as is practical and lead lengths should be as short as possible. The MVL407 should be soldered into the printed circuit board instead of using a socket. To minimize ringing, output lead lengths of 2 cm or less are recommended. If longer lengths are required, use micro-strip transmission line, miniature coaxial cable, or twisted pair. Reflections will occur unless the line is properly terminated. Termination resistors typically go to -2.0 V. Low impedance lines are better for driving capacitive loads. Supply voltages should be well decoupled with good RF capacitors connected to the ground plane as close to the MVL407 supply pins as practical.

Measurement of Propagation Delay

The ability of a voltage comparator to perform an accurate timing function is determined by the constancy of its propagation delay with overdrive. Because the input risetime and the comparator's slew time add in quadrature to produce the observed propagation delay, it is necessary to employ a very fast input pulse to accurately measure propagation delay variances of the device. A slow input would give optimistically low results.

In order to produce a sufficiently fast and clean input pulse, a tunnel diode based pulse generator was employed. It pro-

duced a very clean pulse with a risetime (10% to 90%) of approximately 0.1 nsec. See Figures 7 and 17.

Measurement of Double Pulse Resolution

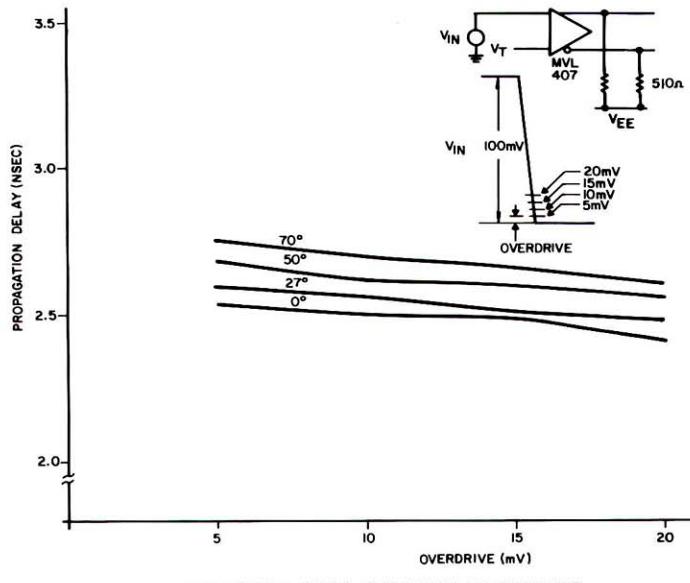
The width of input pulses is adjusted to the minimum which will provide a full amplitude output. Delay of second pulse is reduced until a degradation of output amplitude is noted. The closest spacing of the input pulse pair which will produce a second pulse of full output amplitude is the double pulse resolution (Figure 5).

Hysteresis

The MVL407 incorporates about 3.5 mV of internal hysteresis, and therefore has two thresholds separated by about 3.5 mV. One threshold (V_{T+}) applies for input signals that cause a low-to-high transition on the normally low output (e.g., a positive-going signal applied to the IN⁺ input, or a negative-going signal applied to the IN⁻ input). The other (V_{T-}) applies for input signals that cause a high-to-low transition on the normally low output. The hysteresis voltage (V_H) is the difference between these two thresholds. V_{T+} , V_{T-} , and V_H are measured as shown in Figure 4.

The presence of this hysteresis helps assure that the outputs of the MVL407 are always in a defined state, even for small or very slowly changing inputs. Comparators without hysteresis show a pronounced tendency to oscillate when biased near threshold. In spite of its higher speed, the MVL407 gives much cleaner operation than other comparators.

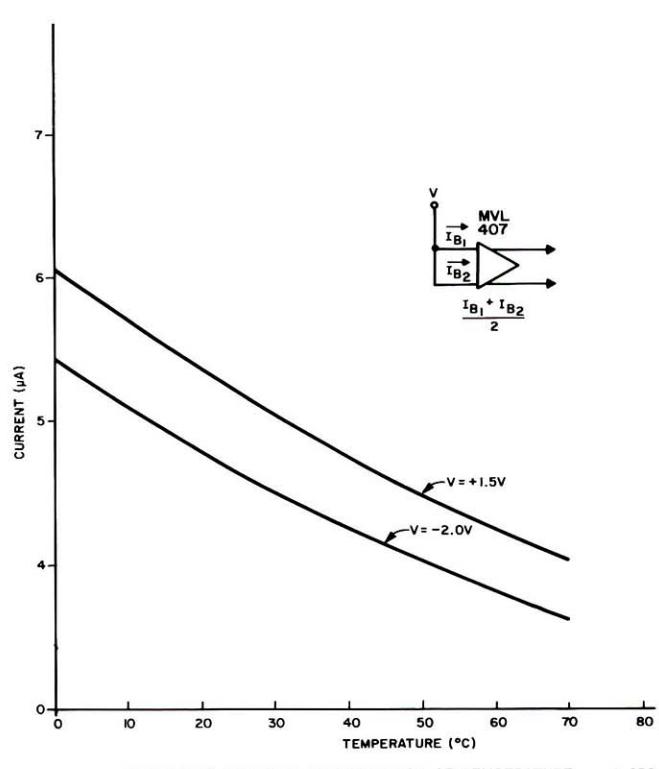
TYPICAL PERFORMANCE CURVES



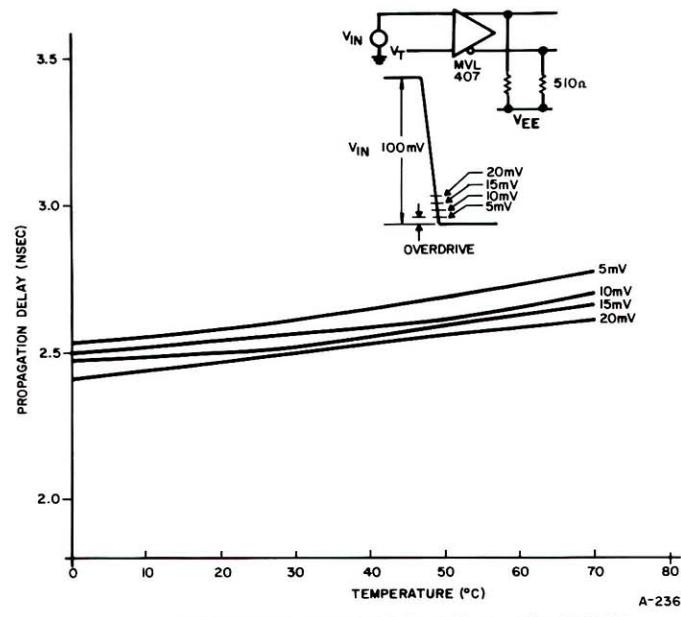
A-235

PROPAGATION DELAY AS FUNCTION OF OVERDRIVE

Figure 8

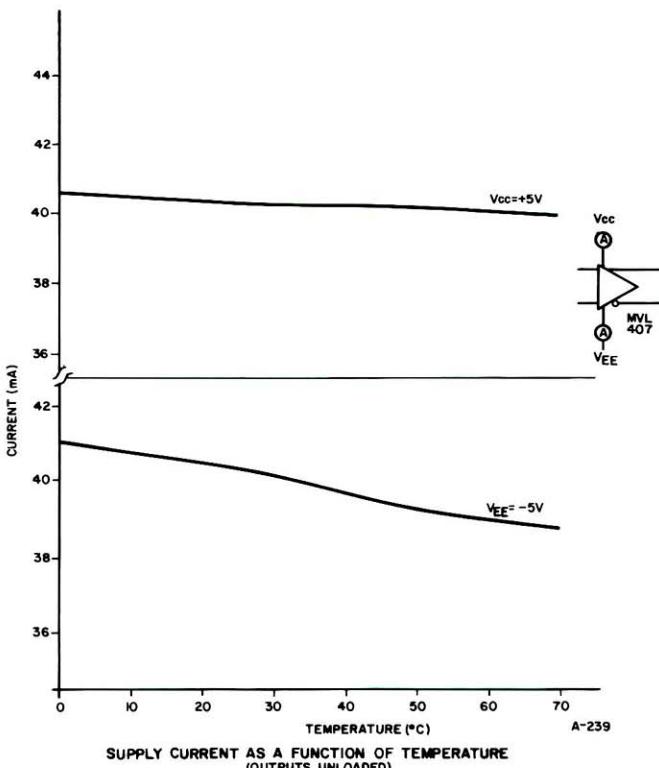


A-238



PROPAGATION DELAY AS A FUNCTION OF TEMPERATURE

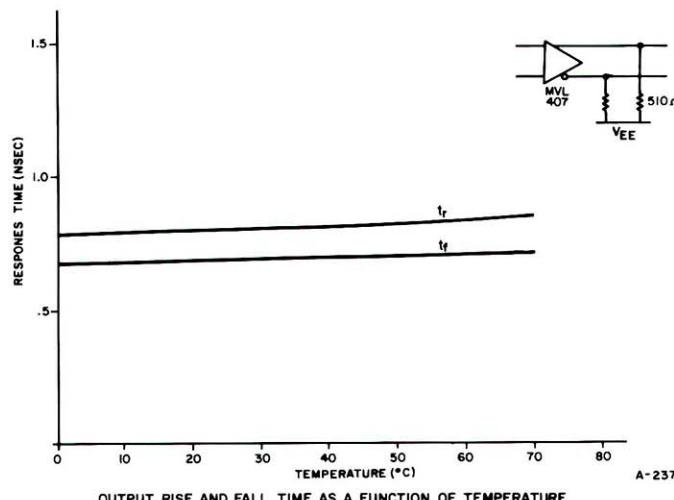
Figure 9



A-239

SUPPLY CURRENT AS A FUNCTION OF TEMPERATURE
(OUTPUTS UNLOADED)

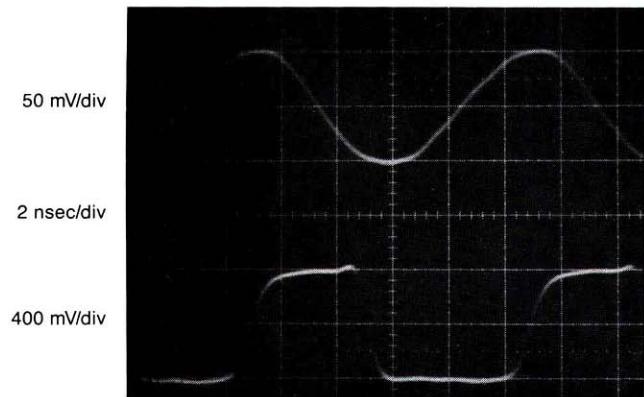
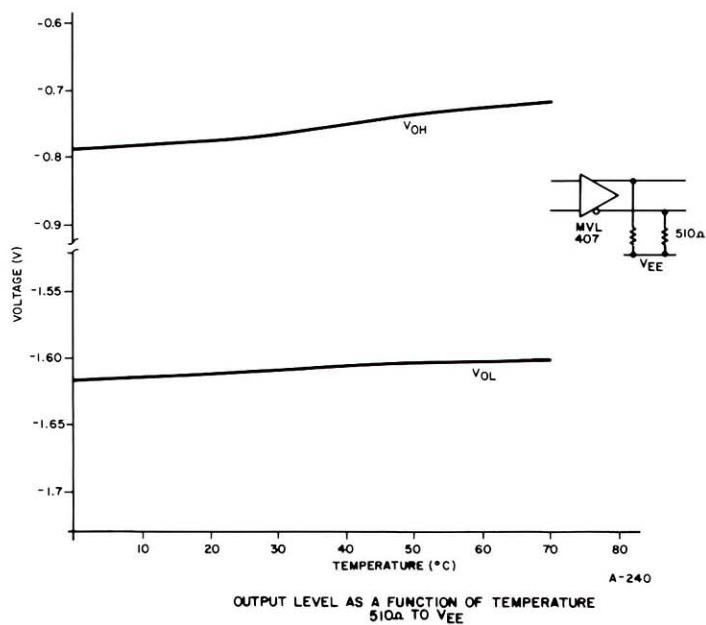
Figure 12



OUTPUT RISE AND FALL TIME AS A FUNCTION OF TEMPERATURE

Figure 10

TYPICAL PERFORMANCE TRACES



Response to 100 MHz sine wave.

Figure 15

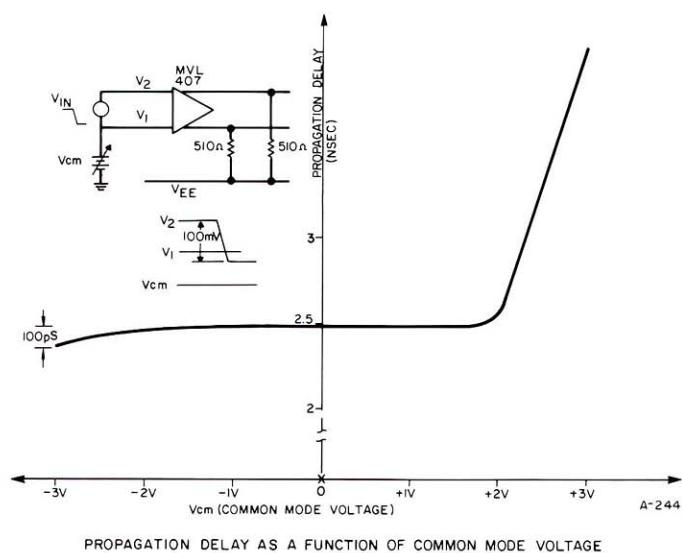
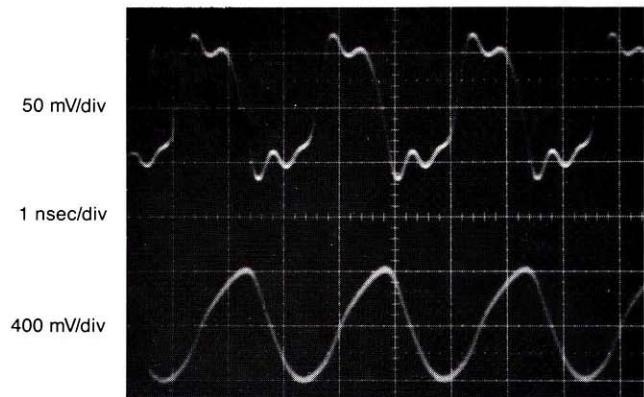
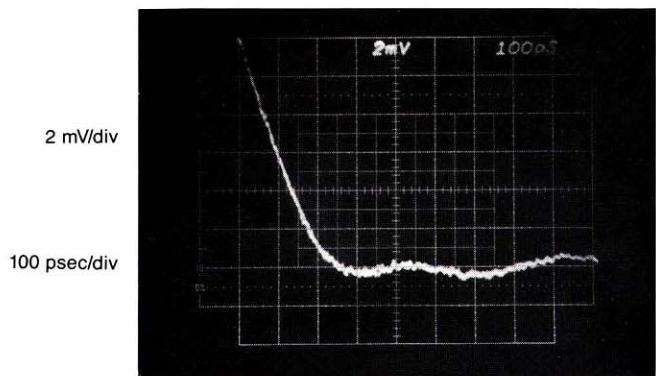


Figure 14



Response to 400 MHz input.

Figure 16



Fast timing pulse. See Figure 7.

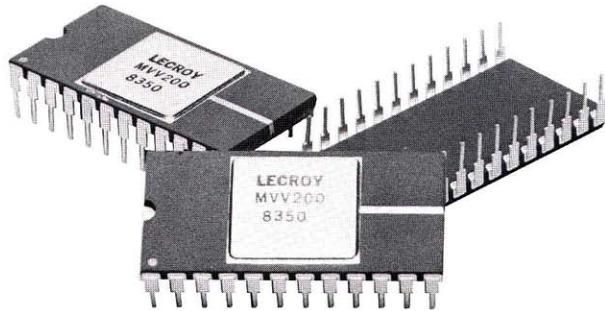
Figure 17

TECHNICAL DATA

LeCroy

Monolithic Model MVV200 320/640-Cell Analog Shift Register

- **High Sampling Rate:** >40 MHz (>80 MHz—2 channels multiplexed)
- **High Dynamic Range:** >10 bits
- **Extremely Small Spatial Noise:** <0.1%
- **Low Power Consumption:** MOS technology
- **Excellent Thermal Stability:** Using compensated reference
- **Negligible Droop Rate:** 0.1%/msec
- **Charge Coupled**

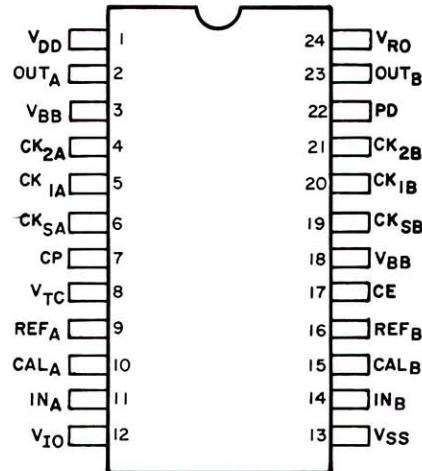


GENERAL DESCRIPTION

The MVV200 is a high accuracy analog shift register optimized for use where analog signals must be accepted (written) at a high clock rate but utilized (read) at a lower rate. The geometry of the CCD has been designed to optimize the dynamic range response and device speed (both input slewing and clock speed). The MVV200 consists of two 320-cell analog shift registers, each with its own voltage input, transport clock and output port, allowing the device to be used as two 320-cell or one 640-cell analog shift register. Although the device utilizes charge in its shift register, the input is a voltage sampling device and the output is a voltage source. The MVV200 can be used in applications requiring time base expansion in which analog channels require high speed sampling and temporary storage, allowing later conversion to digital by a lower speed low cost ADC. In particular, applications include Time Projection Chambers (TPC's), Jet Chambers and other imaging detectors.

PIN DESIGNATION (CHANNELS A & B)

IN_A, IN_B Signal Voltage Inputs
CAL_A, CAL_B Calibrate Voltage Inputs
REF_A, REF_B Reference Voltage Inputs
CE Calibrate Enable Input
CP Clamp Pulse Input
V_{TC} Thermal Compensation Bias Voltage
V_{IO} Input Offset Voltage Input
CK_{SA}, CK_{SB} Sample Clocks
CK_{1A}, CK_{1B} Phase 1 Transport Clocks
CK_{2A}, CK_{2B} Phase 2 Transport Clocks
OUT_A, OUT_B Signal Voltage Outputs
PD Power Down Input
V_{RO} Reset Output Voltage Input
V_{DD} Drain (Positive Supply) Voltage
V_{BB} Substrate (Negative Bias) Voltage
V_{SS} Ground



FUNCTIONAL DESCRIPTION

A block diagram of the MVV200 is shown in Figure 1. It indicates the major subsections of the device, each of which will be described below. For the purpose of simplicity, only channel A is described. Channel B is identical.

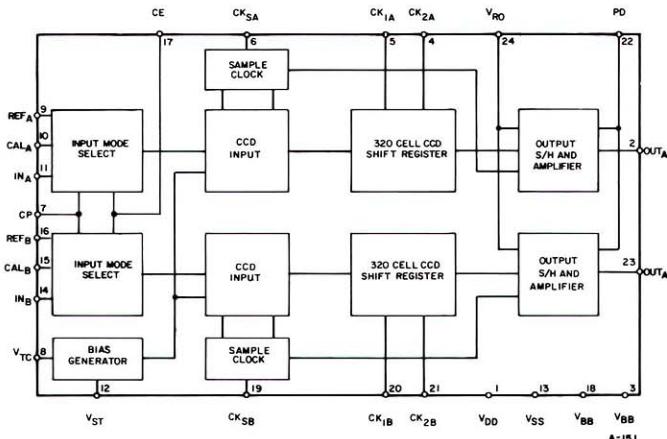


Figure 1
MVV200 Block Diagram

Input Circuit

The front end of the MVV200 includes analog switching for input selection. See Figure 2. One of two analog inputs may be selected. These are called IN_A , the normal input, and CAL_A , intended for calibration purposes. The CE signal, common to both channels, selects the CAL_A/IN_A input when high/low.

Also connected to the internal input node is an analog switch operated by the clamp pulse, CP (common to both channels). When enabled, this connects the REF_A input to the node and to the analog input selected as described above. This circuit allows baseline restoration of a capacitively coupled input stage. The selected input is clamped to REF_A by asserting CP high.

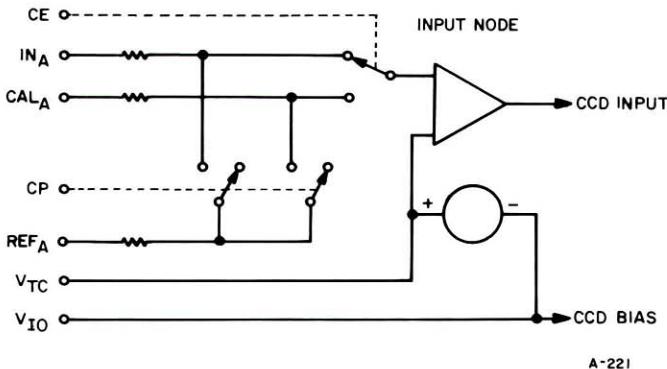


Figure 2
Resistors $\approx 1 \text{ k}\Omega$
Input Equivalent Circuit

The input signal voltage is the voltage difference between the input node voltage and V_{TC} . See Figure 2. Here V_{TC} is a reference voltage common to both channels, intended to bias external input conditioning circuitry.

To provide the greatest flexibility, it is possible to offset the input operating range of the MVV200. The V_{IO} input provides the function of input offset adjustment. If $V_{IO} = V_{SS} = 0 \text{ V}$, the operating range is approximately $+3.5 \text{ V}$ to $+6.5 \text{ V}$. In this case, $V_{TC} = 3 \text{ V}$. If V_{IO} is set to $+3 \text{ V}$, then the operating range is approximately $+6.5 \text{ V}$ to $+9.5 \text{ V}$ and $V_{TC} \approx 6 \text{ V}$. See Figure 3.

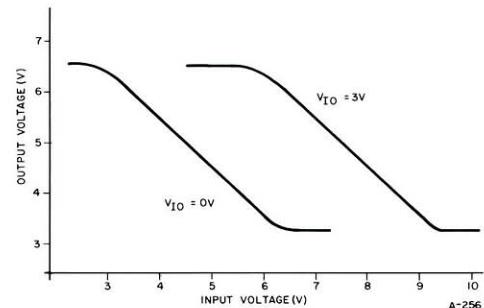


Figure 3
The Operating Range

CCD Input

The CCD Input includes a track-and-hold circuit which samples when the sample clock, CK_{SA} , is high and holds when CK_{SA} is low. This section also includes a charge injector which applies a charge to the first cell of the CCD shift register and is clocked by the falling edge of CK_{SA} .

320-Cell Analog Shift Register

The CCD register transports the charge packets from cell to cell. For this purpose, two transport clock signals, CK_{1A} and CK_{2A} , are required. In order to transfer all charge packets forward by one cell, it is necessary to raise and lower CK_{1A} and CK_{2A} in turn. See Figure 4. The simplest possible circuit has $CK_{2A} = CK_{1A}$. Note that while the sample clock requires a fast falling edge, all four edges of the transport clocks are less critical.

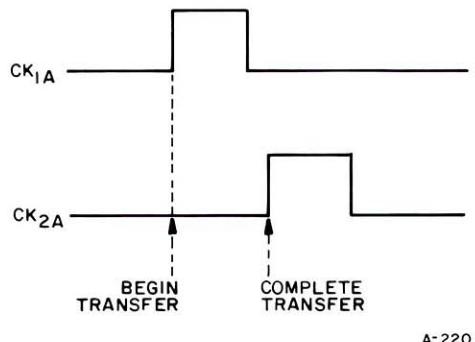


Figure 4
One Transfer Cycle

Output Stage

In normal operation, reading the MVV200 consists of successively shifting charge packets to the end of the CCD shift register and applying a corresponding voltage to the output pin OUT_A . Due to the high impedance of the output buffer circuit, it is also necessary to provide a discharge path for the last cell before shifting another charge packet to it. A circuit is included to minimize output swing due to the discharge operation. See Figure 5.

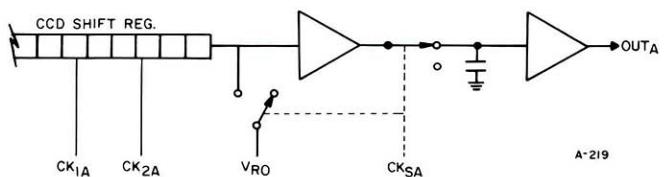


Figure 5
The Output Stage

For extremely critical applications where low chip temperatures are required, it is possible to defeat the output stage, saving 50 mW during the write cycle. This pin, called PD, is set to V_{SS} to enable the output amplifier and to V_{DD} to disable it.

In order to minimize the timing constraints placed upon read clocking, an internal timing generator operates the output stage strobes. This circuit is controlled by CK_{SA} and is sensitive to the phase of CK_{2A} . Three constraints must be met for proper read operation:

1. The minimum high width of CK_{SA} must be 80 nsec.
2. The clock CK_{2A} must be low for at least 20 nsec before the falling edge of CK_{SA} .
3. The clocks CK_{1A} and CK_{2A} must make as many transitions as CK_{SA} and must spend >10 nsec in opposite states. See Figure 4. For the purpose of convenience, $CK_{1A} = CK_{SA}$, $CK_{2A} = \bar{CK}_{SA}$ may be implemented.

Data are valid beginning within 170 nsec of the falling edge of CK_{SA} and remain stable until the rising edge of the next CK_{SA} pulse. See Figure 6.

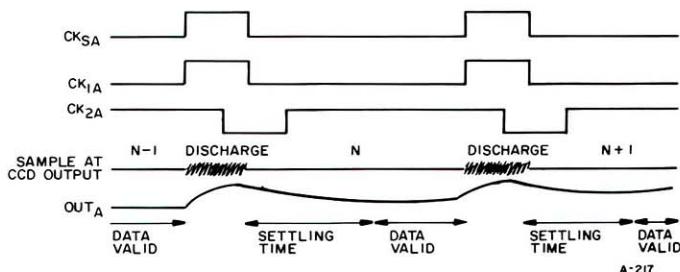


Figure 6
Clocking the Output

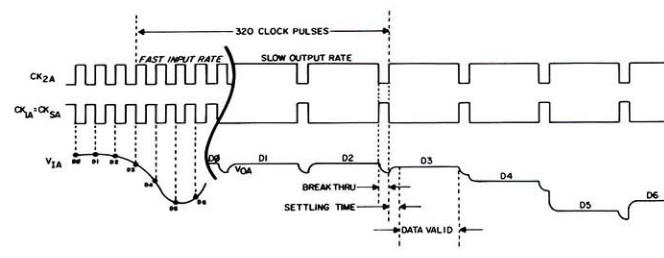
A parameter associated with the output stage is Rate of Signal Droop (RSD). The output has an integral sample-and-hold amplifier, and when the output is in the "hold" state ($CK_S = \text{low}$) the output will droop at the specified rate.

The impedance of the output amplifier is approximately 400Ω . The output circuit has a rail to rail swing from approximately $+3.5$ V to $+7$ V when enabled. Note that the overall transfer function of the MVV200 is inverting.

MODES OF OPERATION

320-Cell Time Expansion

Each of the two analog shift registers can be used to independently acquire and store up to 320 analog samples at high clock rates (<1 to >40 MHz), then read out at slower rates (0.5 to 5 MHz). The waveforms required to operate shift register A are shown in Figure 7. To write into the register, the output may be disabled (PD high) and the input voltage, referenced to V_{TC} , is applied to IN_A . The voltage on the input at the time of the falling edge of CK_{SA} causes a proportional amount of charge to be injected into the first cell of register A. The charge is then shifted from cell to cell by the shift clocks CK_{1A} and CK_{2A} . In general, a CK_{1A} pulse is followed by a CK_{2A} pulse. The simplest way to achieve this is to make CK_{2A} the complement of CK_{1A} , and for CK_{SA} to be equal to CK_{1A} . Note, however, that the V_{DD} current is about ten times higher with CK_{SA} high, so it may be advisable to minimize this clock width. At the end of the desired sampling period, the clocks should be stopped with CK_{1A} and CK_{SA} low. CK_{2A} can be either left high, or also brought low after its last pulse. With the output enabled (PD low), a readout clock sequence can be begun. CK_{1A} and CK_{SA} should again be operated with the minimum required width (80 nsec in the read mode) for minimum power. Allowing about 150 nsec for settling after CK_{SA} goes low, the "held" analog data can be read at the OUT_A terminal, during the period of valid data indicated in Figure 7.

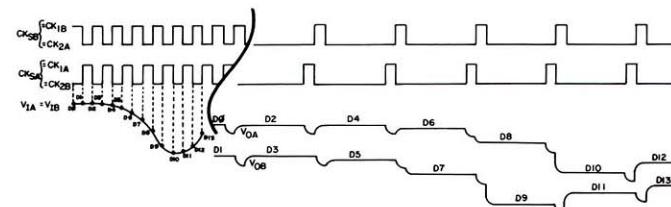


Note: Output Inversion Not Shown

Figure 7
Timing Diagram
One 320-Cell Register

640-Cell Time Expansion

If more than 320 samples are required, or if faster sampling rates are required, the two analog shift register inputs can be tied in parallel and the clocks tied in cross-phase. See Figure 8. This will provide 640 cells of analog storage, and will operate at an effective sample rate that is twice the clock frequency. Because CK_{1A} and CK_{SA} are now the complements of CK_{1B} and CK_{SB} , data is sampled and shifted on each edge of the original clock. It is necessary that the clocks are symmetrical to provide uniformly spaced sample times. It will also be necessary during readout to use care to start the clocks from the same phase they were stopped. Also, if power dissipation is of concern, it is necessary that CK_{1A} , CK_{SA} , CK_{1B} and CK_{SB} all be left in the low state after each shift sequence.



Note: Output Inversion Not Shown

Figure 8
Timing Diagram
Two Multiplexed 320-Cell Registers
(640-Cell Analog Shift Register)

ANALOG PERFORMANCE

The limits to the analog performance of the MVV200 are noise and leakage. These parameters as well as the operating range specify the signal to noise ratio achievable with the device. Measurements of typical room temperature performance are presented and discussed below as a guide for the designer.

Dynamic Range

Figure 9 shows a plot of the transfer characteristics of the device. The MVV200 is an inverting device with a gain of very nearly unity. The operating range spans a 3 V interval. An analysis of the data indicates that the linearity of the device is $\pm 0.2\%$ over a 2 V range. Typical linearity data is shown in Figure 10. The width of the curve includes random noise.

Random Noise

The random noise of the device was determined by repeated measurement of the response to a DC input. A noise histogram

is shown in Figure 11. The measurement excluded effects due to Spatial Noise by measuring the output of one bucket only. The FWHM of the noise distribution was found to be 0.5 mV.

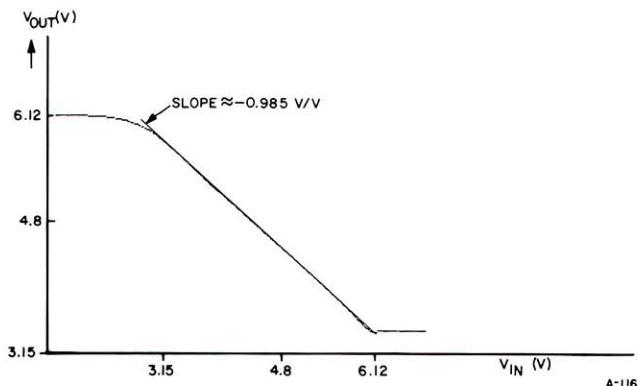


Figure 9
Measured Transfer Characteristic

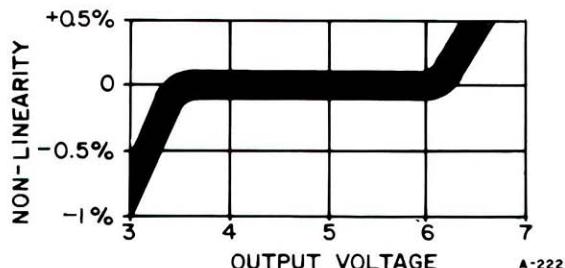


Figure 10
Linearity Plot

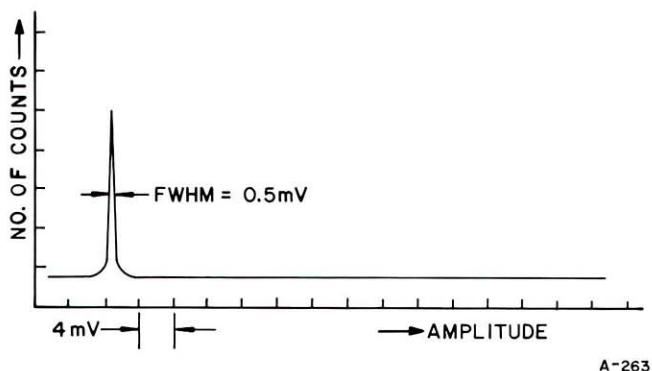


Figure 11
Random Noise Spectrum

Spatial Noise and RSO

Both of these effects are a result of charge leakage in the CCD shift register. The Rate of Signal Offset (RSO) is a droop of the baseline which is linear with storage time. The output of an MVV200 channel moves towards V_{SS} as the storage time increases. This is noticeable in Figure 12.

Two observations are shown. The upper figure has a 1.3 msec pause between the write and read intervals. In the lower figure this interval was 13 msec. The difference between vertical intercepts of these two observations is 5.2 mV. This corresponds to an RSO of approximately 0.5 mV/msec. Note also that the slopes of these two figures are due to RSO drift during the readout time.

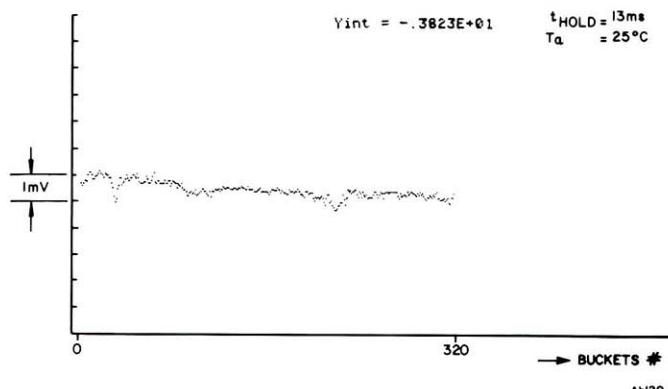
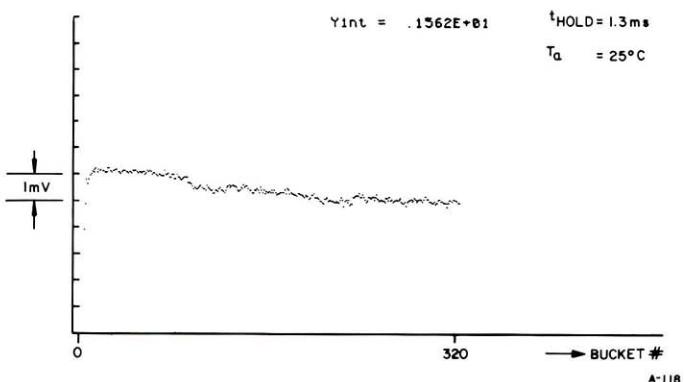


Figure 12
Signal Droop and Spatial Noise

The Spatial Noise (SN) is a consequence of cell to cell variations of RSO: It is a result of geometrical factors in the chip layout. Typical results of Spatial Noise measurements are shown in Figure 12. These are the response of the MVV200 for a DC level input. Here SN is the deviation from the "ideal RSO straight line". Note that the SN is more prominent in the upper figure when determining the response of the MVV200. SN is also affected by temperature. A good rule of thumb is that SN doubles for each 10°C increase.

Interchannel Isolation

It is essential that each channel of the MVV200 be unaffected by operations taking place in the other channel. Such inter-channel cross talk was tested first by driving channel A with a square wave signal while the input of channel B was connected to ground via $50\ \Omega$. The write clock frequency was 55 MHz. The results, shown in Figure 13, indicate that inter-channel isolation is excellent (>60 dB). Note that channel B is displayed with 5 times the sensitivity of channel A.

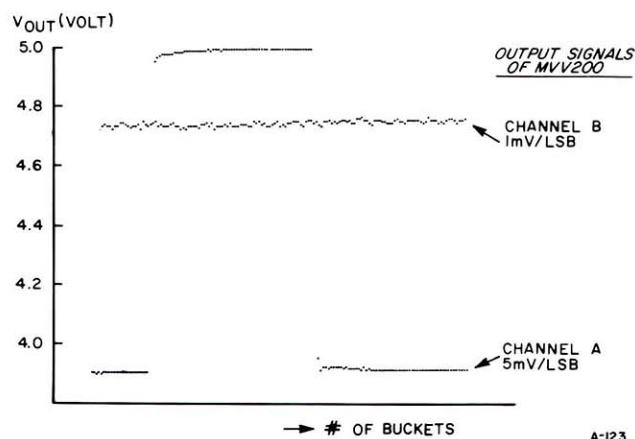


Figure 13
Interchannel Isolation

Pulse Response

Figures 14 and 15 show the response of the MVV200 to various inputs. In Figure 14, the MVV200's response to a step function is shown. The write clock frequency was 20 MHz and the MVV200's output signal was digitized with an 8-bit ADC. Note that the 0 to 100% response time is less than one time bucket. In Figure 15, the MVV200 was used in 2 channel interleaved mode to track a double pulse with risetimes on the order of 10 nsec. This figure demonstrates the viability of an

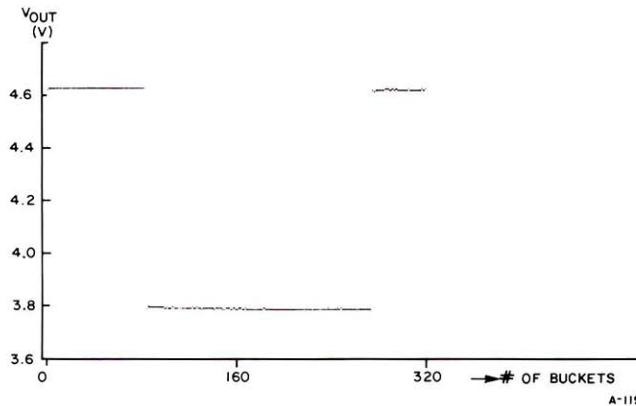
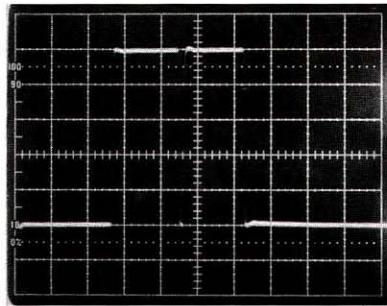
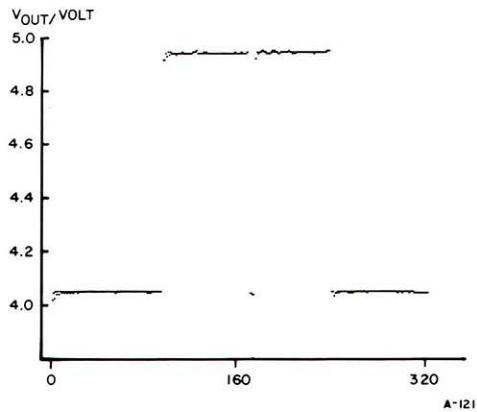


Figure 14
Step Response, Non-interleaved Mode
X: 50 nsec/bucket
Y: 5 mV/LSB, 200 mV/div.



a. Input signal to MVV200.
Two channels interleaved.
Y: 200 mV/div.
X: 400 nsec/div.



b. Output signal of MVV200.
Y: 5 mV/LSB
X: 10 nsec/bucket
First 320 buckets shown

interleaving technique to achieve high sampling rates. Again, the output signal was digitized by an 8-bit ADC.

DESIGN CONSIDERATIONS

Clock Drivers

Figure 16 shows the equivalent input for the clock inputs to one channel of the MVV200. Capacitance values shown are typical. Resistor R_C decouples the relatively high capacitance inputs of the shift clock (pins 4 and 5) from the driver circuit. Typical values for R_C are 10 to 100 Ω , depending on the clock frequency used. For good aperture time, the sample clock input (pin 6) is connected directly to the ϕ_1 driver output stage, maintaining short transition times.

Note that the clock drivers must be capable of delivering sufficient voltage swing, which may be difficult at high frequencies. The energy stored in the total effective clock input capacitance is roughly $1.5 \cdot 10^{-8}$ J, so at 50 MHz, the clock driver will supply approximately 1.5 VA per channel (= 30 mVA per MHz). To reduce the clock driver peak current the clocks can be operated by alternately pulsing each independently while keeping the other at V_{SS} (compare Figure 4). To reduce the clock driver power requirements, the capacitive current to the clock inputs can be partially or completely compensated with inductors.

A simple clock driver for use with the MVV200 is shown in Figure 17. Reliable operation is achieved up to a clock frequency of 40 MHz. At lower frequencies, one driver can supply the clock pulses for many MVV200s tied with the corresponding clock inputs in parallel.

Power Down Mode

Asserting the PD input disables the output circuitry and reduces the total power consumption of the MVV200. PD may be asserted during write mode but it must be de-asserted (i.e., grounded) during read mode. See the Clock and Control Input Characteristics section below.

MVV 200 CLOCK LINE DRIVERS

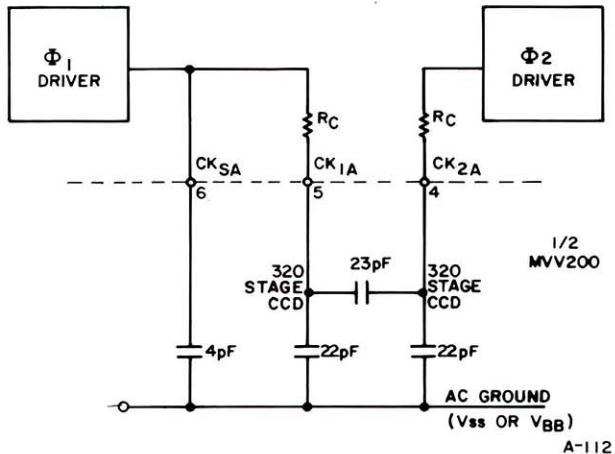


Figure 16
Clock Inputs Equivalent Circuit

THERMAL COMPENSATION

AC Coupled Inputs

Figure 18 shows the simplest method of connecting the MVV200 inputs when AC coupling is being employed. R_1 and R_2 together with V_{TC} define the DC input voltage of the MVV200. R_3 should be selected to set the input RC time constant.

CP, the Clamp Pulse input, is used to re-stabilize the input capacitors during read mode. CP should not be asserted during write mode. A suggested circuit for thermally compensating the MVV200 (using the Clamp Pulse) with AC coupled inputs is shown in Figure 19. If V_{IO} is not ground, it must have an appropriate DC voltage level applied to it.

The Clamp Pulse (CP input) is asserted at some time other than during write operations in order to re-stabilize the input capacitors. CP must be asserted for several RC time constants to assure baseline restoration of the input. The clamp pulse should be released about 100 nsec before write operations begin. (R = resistance of input source plus 1 k Ω ; C = coupling capacitance = C_A or C_B .)

Divider resistors must be chosen so that the total current at V_{TC} is approximately 100 μ A. The voltage level at V_{TC} in Figure 19 is the lowest possible input voltage. Resistors R_A and R_B should be chosen so that the voltage at points REF_A and REF_B in Figure 19 are at AC ground for the channel A and B inputs, respectively.

For best DC stability, the output signals OUT_A and OUT_B can be thermally compensated as in Figure 20.

DC Coupled

Thermal compensation for DC coupled inputs is achieved by the circuit shown in Figure 20. This circuit functions similarly to the circuit shown in Figure 19 except that the input signal conditioning amplifiers are referenced to REF_A and REF_B and the CP input is grounded.

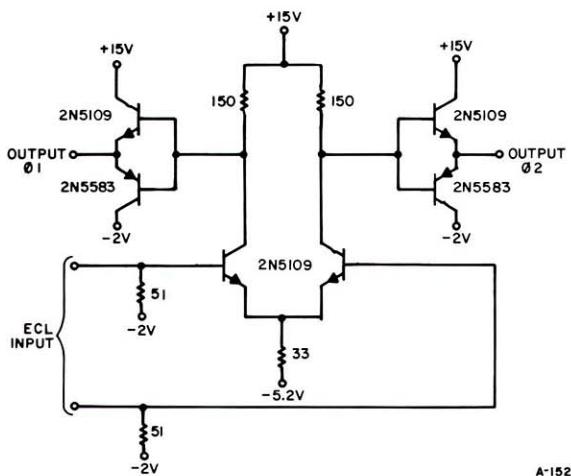
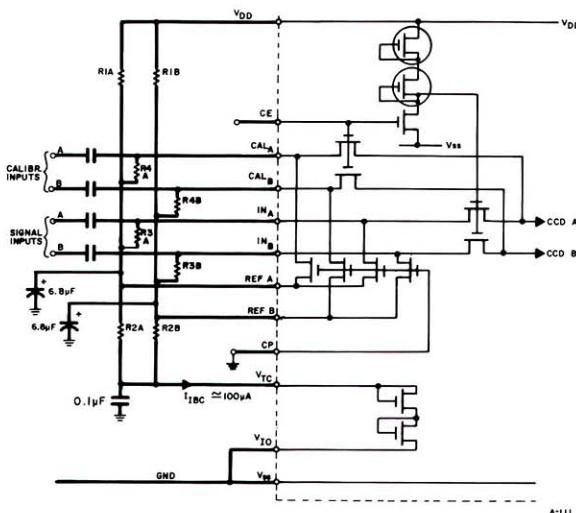


Figure 17
A Clock Driver Circuit



I_{BC} Input Bias Chain Current
V_{DD} Drain Supply
V_{SS} Ground
CE Calibration Input Select
CALA, CALB Calibration Input

Figure 18
A Sample AC Coupled Circuit

A Typical Circuit

The basic circuit needed to operate the MVV200 as a 2 channel, 320 bucket analog shift register is shown in Figure 21. Input and output can be DC coupled. However, a proper DC offset has to be used for linear operation. This can be done either by offsetting the inputs and outputs with a suitable DC voltage or by offsetting the power supply voltages as assumed in Figure 21. Input clamping is disabled by tying it to V_{SS} .

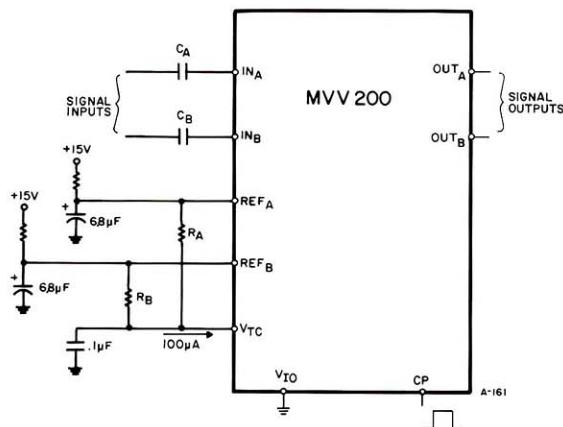


Figure 19
Using the Input Clamp

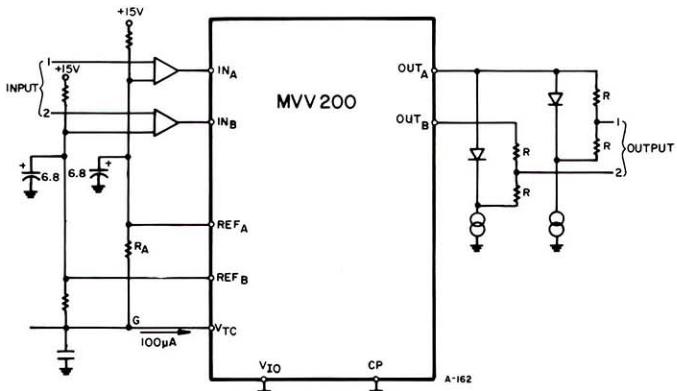


Figure 20
DC Coupling and Output Compensation

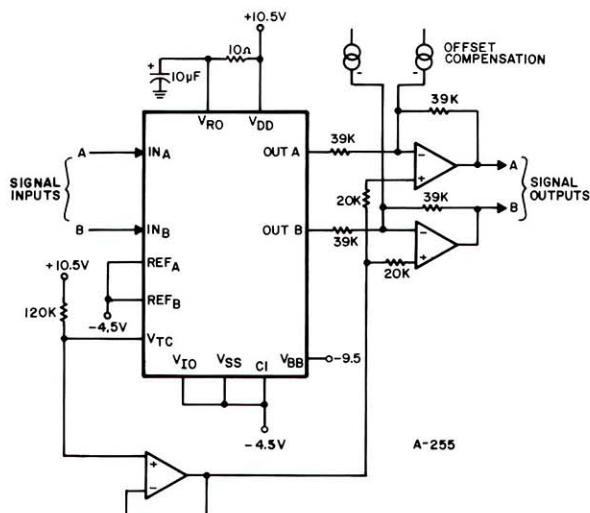


Figure 21
A Typical Circuit

SPECIFICATIONS

Monolithic Model MVV200

320/640-CELL ANALOG SHIFT REGISTER

DC CHARACTERISTICS (See Note 1)

Symbol	Characteristic	Range				Condition
		Min	Typ	Max	Units	
V _{DD}	Supply (Drain) Voltage	14.5	15	15.5	V	
I _{DD}	Supply (Drain) Current					
(I _{DD1})	PD	L	—	0.9	mA	Note 2
(I _{DD2})		H	—	13	mA	Note 2
(I _{DD3})		L	—	5	mA	Note 2
(I _{DD4})		L	H	18	mA	Note 2
V _{SS}	Ground	—0	0	0	V	
V _{BB}	Substrate Bias	—6	—5	—4	V	
I _{BB}	Substrate Current	—	—	50	μA	
REF _A , REF _B	Reference Input Voltage	0	3.5	10	V	For use with CP
I _{IN}	Input Leakage Current	—	0.1	12	nA	
C _{IN}	Signal Input Capacitance	—	4	7	pF	
C _{CK1} , C _{CK2}	Register Clock Capacitance	—	23	30	pF	Phase to Phase
		—	22	31	pF	Phase to Ground
C _{CKS}	Sample Clock Capacitance	2	4	7	pF	Phase to Ground
C _{CP}	Clamp Pulse Capacitance	2	4	7	pF	
R _C	Clamp On Resistance	—	1	2	kΩ	Notes 14 and 15
R _{OUT}	AC Output Resistance	—	400	—	Ω	
V _{TC}	Temperature Compensated Voltage	2.3	3	3.7	V	
V _{IO}	Input Offset Voltage	0	—	3	V	

CLOCK AND CONTROL INPUT CHARACTERISTICS: (See Note 1)

Symbol	Characteristic	Range				Condition
		Min	Typ	Max	Units	
CK _{1L} , CK _{2L}	Register Clocks Low	—1	0	0.8	V	Both A and B
CK _{1H} , CK _{2H}	Register Clocks High	13.5	14.5	15.5	V	Both A and B
CK _{SL}	Sample Clocks Low	—1	0	0.8	V	Both A and B
CK _{SH}	Sample Clocks High	13.5	14.5	15.5	V	Both A and B
CP _L	Clamp Pulse Low	—1	0	0.8	V	
CP _H	Clamp Pulse High	(V _{REFM} + 4.0)	—	15.5	V	Note 14
CE _L	Calibrate Enable Low	—1	0	0.8	V	
CE _H	Calibrate Enable High	(V _{CALM} + 4.0)	—	15.5	V	Note 13
PD _L	Power Down Low	—1	0	0.8	V	Read Mode
PD _H	Power Down High	4.5	—	15.5	V	Write Only Mode
f _w	Write Frequency (max)	40	50	—	MHz	Note 18
f _r	Read Frequency (max)	5	10	—	MHz	Note 18

ASSOCIATED CHARACTERISTICS: (See Note 1)

Symbol	Characteristic	Range				Condition
		Min	Typ	Max	Units	
G	Small Signal Gain	—.8	—1	—1.25		Note 4
DG	Differential Gain	—	0.3	1	%	Note 5
SN	Spatial Noise	—	0.7	2	mV p-p	Notes 7, 8, 9, 18
RN	Random Noise	—	0.5	0.8	mV rms	Notes 6, 7
V _{IN}	Signal Range—normal input and calibrate input	1.5	3	—	V	Note 10
V _{ODC}	DC Output Voltage	5.5	6.1	7.25	V	Note 16
R _{out}	AC Output Resistance	—	400	—	Ω	
RSO	Output Signal Offset Droop Rate	—	0.7	2	mV/msec	Note 9
RSD	Output Signal Droop Rate	—	1.5	12	mV/msec	Note 11

t_s	Output Settling Time	—	80	170	nsec	Note 17
$f_c(\text{min})$	Min Clock Freq for $V_{IN} = 1 \text{ V}$	3	0.4	—	kHz	Note 10
SRE	Step Response Error for $f_w =$					
	12.5 MHz	—	2	3	%	
	25.0 MHz	—	3	4	%	Notes 3, 7
V_{TC}	Thermal Compensation Bias Voltage	2.3	3	3.7	V	$V_{IO} = 0$
O_{VDC}	Output DC mismatch between					
	A and B register		± 100	—	mV	
O_{VAC}	Output AC mismatch between					
	A and B register		± 1	—	%	
TC	Temperature Coefficient of DC					
	Output Voltage, uncompensated		— 1.8	—	mV/ $^{\circ}\text{C}$	
	Input compensated with V_{TC}		— 1	—	mV/ $^{\circ}\text{C}$	
	Input and Output compensated with V_{TC}		± 0.2	—	mV/ $^{\circ}\text{C}$	

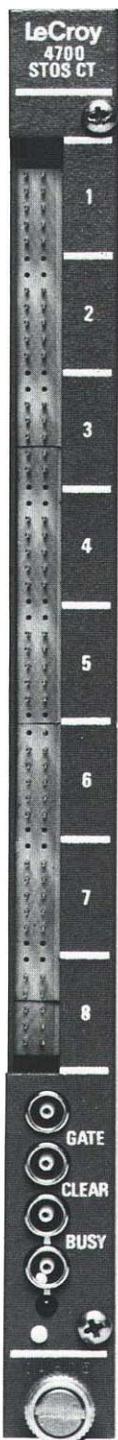
NOTES

- Unless otherwise stated, values are per register, with nominal supply voltages 25°C. Voltages measured with respect to V_{SS} unless otherwise stated.
- Average current = $I_{DD1} + D(I_{DD2} - I_{DD1})$ for the case when PD is high and $I_{DD3} + D(I_{DD4} - I_{DD3})$ when PD is low. D is the duty cycle of CK_S . Figures relate to CE = L. For CE = H add 1 mA typically.
- SRE is measured with synchronized square wave signal of fundamental frequency $f \leq f_{\text{write}}/8$, and amplitude at CCD input of 1 V. SRE is the error in the amplitude of the first signal sample following each signal transition.
- Small signal gain = V_o/V_{in} at $V_{in} = 500 \text{ mV}$ peak to peak, $f_s = 100 \text{ kHz}$. The output signal is inverted with respect to the input signal.
- Differential Gain = $(G_1 - G) \times 100\%$ where G = gain at 1.3 V p-p input signal, G_1 is the small signal gain at 500 mV p-p input, $f_s = 100 \text{ kHz}$.
- RN is rms random noise of an individual bucket measured at a read clock frequency of 500 kHz and an integration time constant of 200 nsec.
- Parameter measured at output, and referred to input by dividing by gain (G). All quoted figures are input referred.
- SN is the p-p variation in output voltage when the clocks have been stopped (CK_{SL} , CK_{1L} , CK_{2H}) for 1 msec. RSO is the variation in DC offset at the output. PD = H for hold period and low for read. Read is achieved by a train of 320 clock cycles at a rate $f = 2 \text{ MHz}$. The SN specification excludes the performance of the 2 storage buckets adjacent to the CCD output and the one storage bucket adjacent to the CCD input.
- SN and RSO are a function of the stopped clock period and typically double for each 10°C temperature increment.
- Maximum signal consistent with $\Delta G < 3\%$.
- RSD is the rate of change of output voltage when the clocks are stopped ($CK_S = CK_{SL}$, $CK_1 = CK_{1L}$, $CK_2 = CK_{2H}$).
- Input bias chain current (I_{IBC}) = 100 μA .
- V_{CALM} is the most positive voltage appearing on either CAL input.
- V_{REFM} is the most positive voltage appearing on either REF input.
- Clamp pulse high level $CP_H = V_{REFM} + 4.0 \text{ V}$.
- $V_{IO} = 0 \text{ V}$, $V_{IN} = V_{TC} + 0.5 \text{ V}$.
- Output settling to 1% of final value after one volt excursion with $R = 100 \text{ k}\Omega$ and $C_L = 30 \text{ pF}$.
- Minimum read and write frequencies are set by RSO and SN considerations.

SPECIFICATIONS SUBJECT TO CHANGE

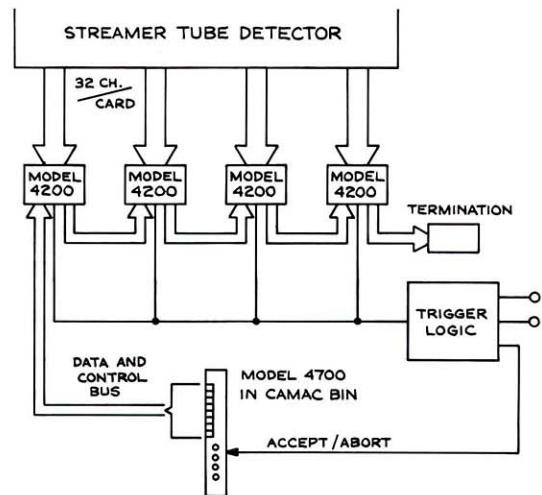
TECHNICAL DATA

LeCroy



STOS 1 Streamer Tube Operating System

- Low minimum threshold, adjustable from ± 30 to $\pm 300 \mu\text{A}$
- 50Ω current inputs, diode protected
- Prompt "OR" output from each Model 4200 Card for trigger logic uses
- Memory built into the 4700 Controller, minimizing computer readout time

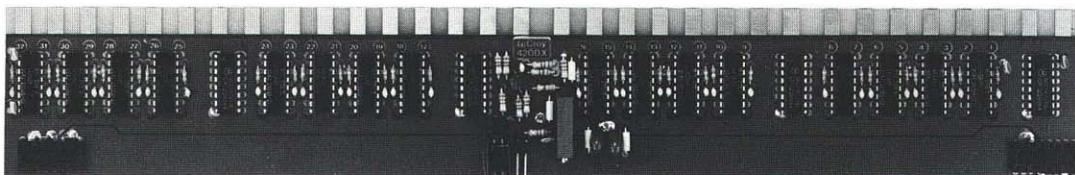


The LeCroy STOS I is a detector-mounted system for encoding Streamer Tube events. The basic system consists of a front end amplifier, discriminator, and temporary event-storage card (Model 4200) and a CAMAC 4700 Controller.

The 32 channel Model 4200 Streamer Tube Card makes its stored signals promptly available (in user-determined groups) for use in trigger logic decisions while awaiting address encoding by the 4700 Controller. Accepted events, acknowledged by the final trigger, are encoded and stored by the Controller. Each Controller directs the operation of up to 256 detector cards for a total of 8192 tubes.

The System achieves remarkably low costs and high reliability through the use of the custom monolithic type MIL200 Dual Amplifier/Discriminator/Monostable, 16 of which comprise the bulk of the 4200 Card.

The STOS I System is mechanically compatible with 10 or 12 mm Streamer Tube spacing, or closer spacing if the cards are "stacked" or placed on both ends of the detector.



Model 4200

December 1982

TECHNICAL DATA

LeCroy

Monolithic Model TRA402 Quad Transresistance Chamber Amplifier

- **Low Cost**
- **High Gain:** 25 mV/ μ A
- **Fast Response:** <3 nsec typical risetime
- **Low Input Noise:** <65 nA rms typical
- **High Density:** 4 channels/22-pin DIP
- **Low Power:** 65 mW per channel typical

The TRA402 is a monolithic four channel, fast, low-noise preamplifier. Its principal application is amplification of wire chamber signals for time-resolved measurements. Its high density makes it a practical solution, especially if space at the detector is at a premium, yet chamber mounting is a necessity.

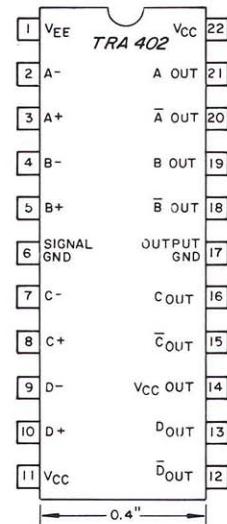
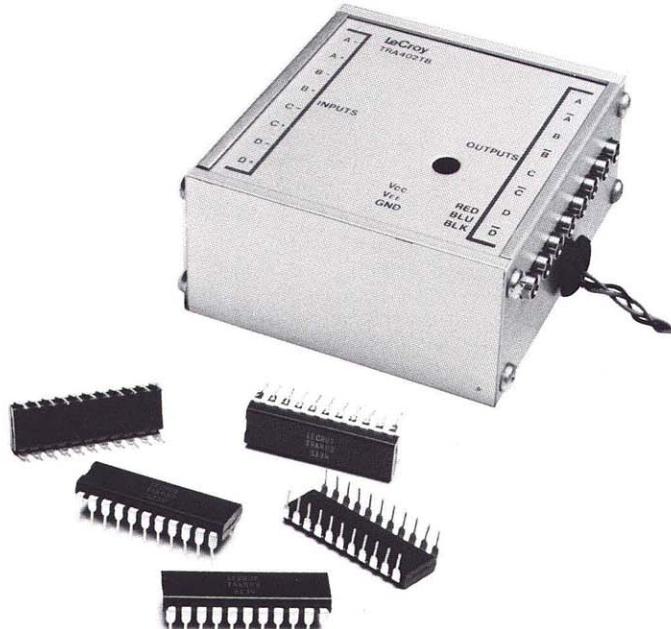
The amplifier provides a gain of 25 mV/ μ A with a risetime of 3 nsec. The low input impedance of <100 Ω and low noise of <100 nA rms is ideally suited to chamber applications, providing little integration of the current pulses. The special input geometry of the TRA402 makes it useful even with high capacitance detectors such as liquid argon calorimeters and wire chamber strips and pads. Because the risetime of the wire input is maintained by the TRA402, the user has greater freedom in selecting the RC coupling to the subsequent circuitry, allowing the risetime/noise trade-off to be optimized.

The TRA402 provides both inverting and non-inverting inputs for all four channels. This allows use of the amplifier with both positive and negative inputs provided by the cathodes and anodes of a wire chamber respectively.

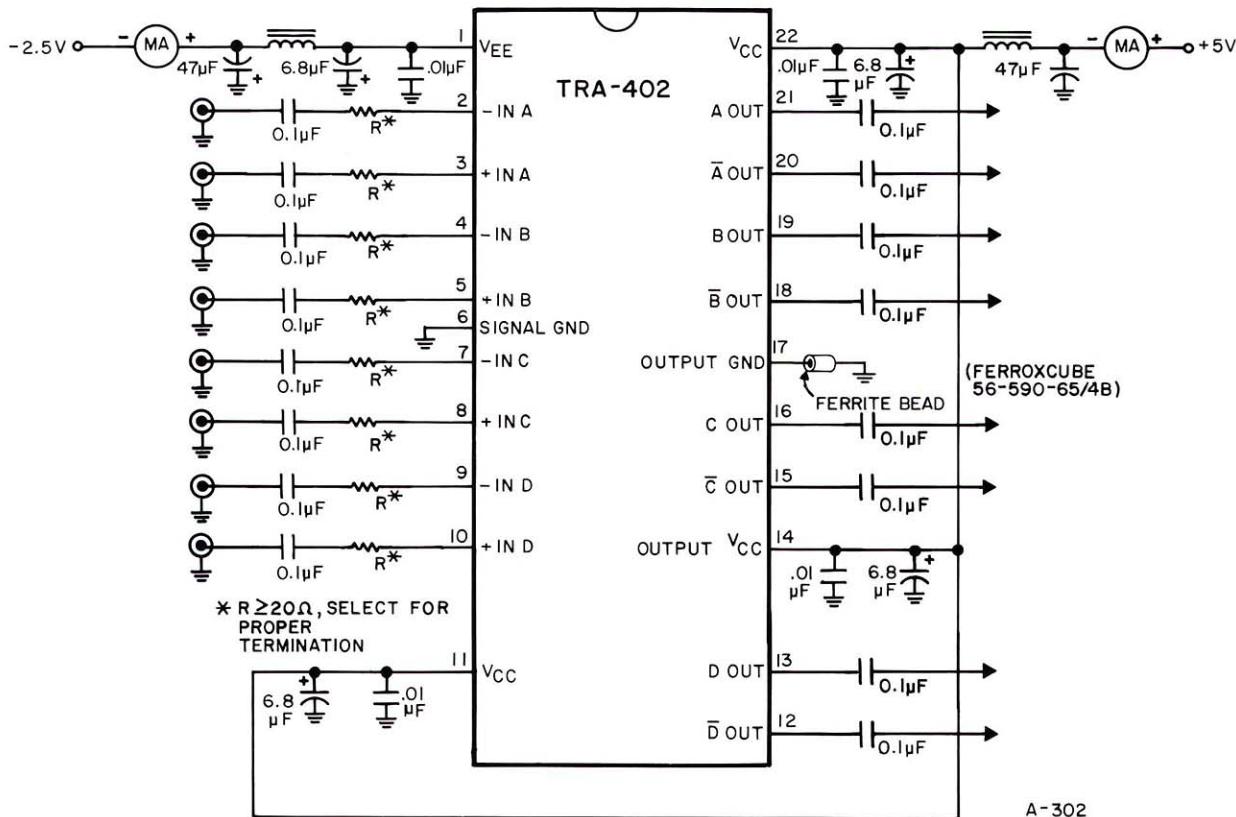
The amplifier has been designed to offer exceptional dynamic range and high gain. It employs two operating voltages, + 5.0 V and - 2.5 V. The circuit has a power dissipation typically 65 mW per channel.

For evaluation purposes, the Model TRA402TB evaluation kit is available. It is recommended for prototyping and testing.

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A-149



TEST CIRCUIT FOR TRA 402

Figure 1

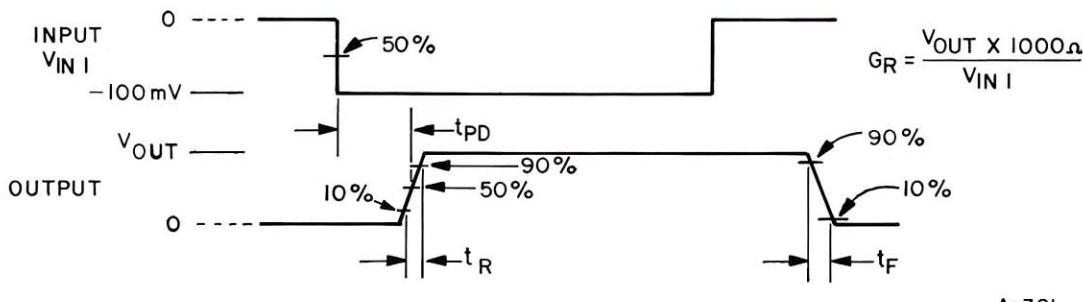


Figure 2

APPLICATION HINTS

The TRA402 is a high gain, high bandwidth device. Thus, good high frequency printed circuit layout techniques are required. Supply voltages must be properly decoupled and input and output trace routings must be well separated and kept to minimum lengths. Lead inductance is a potential feedback mechanism which can cause oscillations. One common cause of this effect is introduced by conventional IC sockets. These may **not** be used with the TRA402. Either insertion pins such as Berg Minisert pins (75060-12), or direct soldering into the board is a necessity. Only with attention to these matters can stable operation with minimum interchannel cross talk be achieved. For most applications, a small inductor (bead) such as a Ferroxcube 56-590-65/4B (LeCroy 300-010-001) or a 10 Ω resistor should be used in series with the output ground. See Figure 3.

POWER SUPPLIES

Two supply voltages are required by the TRA402. By virtue of the design of the amplifier, the voltage range listed above must be observed to achieve the electrical characteristics intrinsic to the device. Bypass of both supplies is required. Capacitors with good high frequency characteristics must be used. Monolithic capacitors of at least .01 μF are recommended. In order to minimize the possibility of oscillation, the positive supply voltage for the amplifier (pins 11 and 22) and the output emitter follower (pin 14) are separately pinned out of the chip. These pins should be tied common on the circuit board. See Figure 3.

DEPENDENCE UPON SUPPLY VOLTAGES

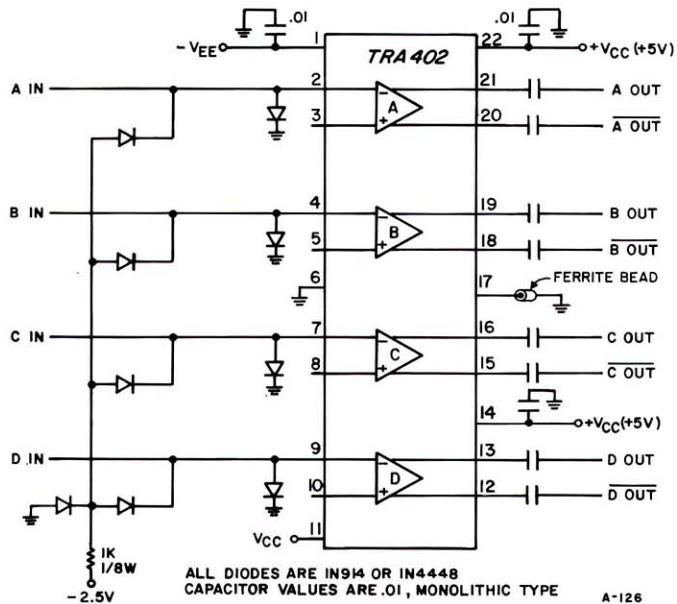
The bandwidth, output swing, conversion gain and noise performance of the TRA402 are affected by the supply voltages. See Figures 4-8. In general, lower

supply voltages give better noise performance at the expense of output swing, gain and response time. The optimum performance must be selected on a case by case basis.

THE INPUTS

The front end of the TRA402 is a differential current amplifier. Both inputs are biased to approximately -0.7 V . Thus, any DC path to ground, resulting in an input current, must be avoided. Unless an extremely high impedance source (e.g. a proportional chamber wire) is employed, the inputs must be capacitively coupled. To protect the inputs against large transients, two diodes should be installed at the input. Use a fast high conductance diode such as 1N914 or 1N4448. See Figure 3.

Each input of the TRA402 consists of a common base stage with the base connected to DC ground. The emitter standing current is set to 0.34 mA and is supplied by an internal current source per input. This



results in a typical input DC offset voltage of -0.65 V and an input impedance of 85 Ω .

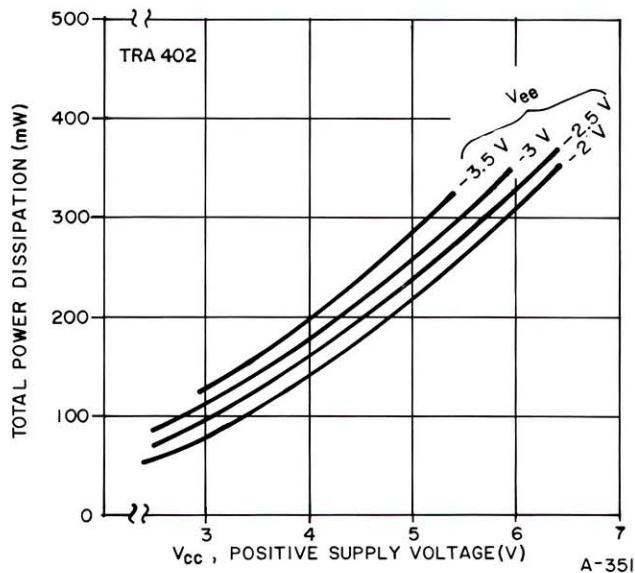
All inputs are protected against positive over voltage with internally connected protection diodes to ground. For negative over voltage, the emitter to base diode of the input transistor acts as a protection diode.

THE OUTPUT

Since the quiescent output level is not at 0 V , the output of the TRA402 must be capacitively coupled as shown in Figure 3 and Figure 9. An output network that serves as DC blocking may also be used to achieve RC shaping. If the amplifier and its load are to be separated, pickup and noise considerations recommend that the shaping be located at the load. The output can drive 50 Ω , making it suitable for use with coax cable. With the TRA402 driving a low impedance load, the amplitude will be attenuated due to its non-zero output impedance. Noise, cross talk and

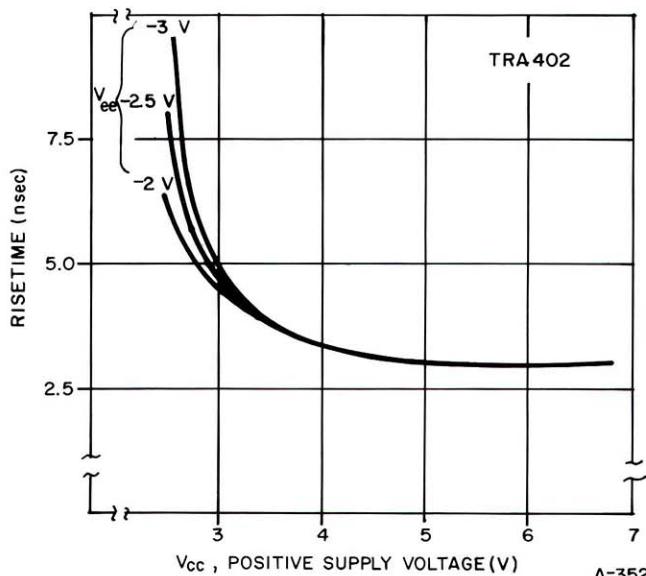
pickup will set an upper limit on the length of cable that can be driven. For long cable runs, shielded twisted-pair cable is recommended.

The maximum positive output voltage swing of the TRA402 is typically $>1\text{ V}$ across 50 Ω and is sufficiently high in most applications. The maximum negative output voltage swing, however, is much smaller and given by the DC standing current in the output emitter followers of the device. The standing current is typically 1.4 mA . This allows driving a 50 Ω load with a maximum negative voltage swing of $1.4\text{ mA} \cdot 50\text{ Ω} = 70\text{ mV}$. In cases where this voltage swing is too small, the user may increase the DC standing current in the output emitter follower. This is



Power dissipation versus V_{cc} and for V_{ee} between -2 V and -3.5 V . The data were taken with no external pulldown resistors.

Figure 4



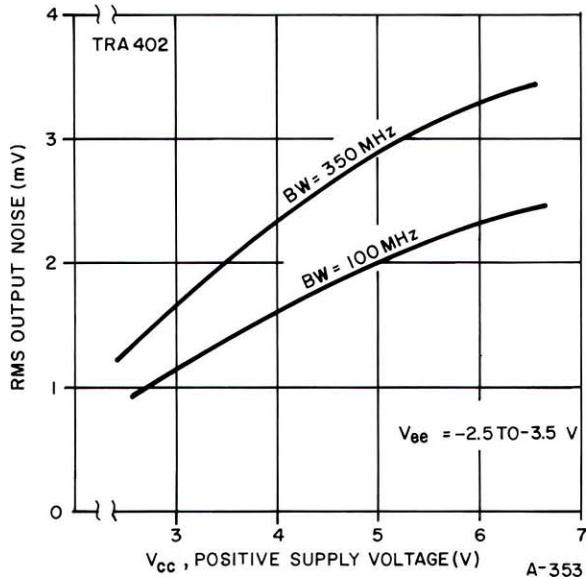
Output signal risetime versus V_{cc} for three different values of V_{ee} with the outputs terminated into 50 Ω .

Figure 5

accomplished by adding an external pulldown resistor per output to a negative voltage. The negative voltage to which the pulldown resistors are connected can either be V_{EE} or a separate, more negative voltage than V_{EE} which results in somewhat better linearity. The value for the pulldown resistors can be calculated by the formulas given in Figure 4. These

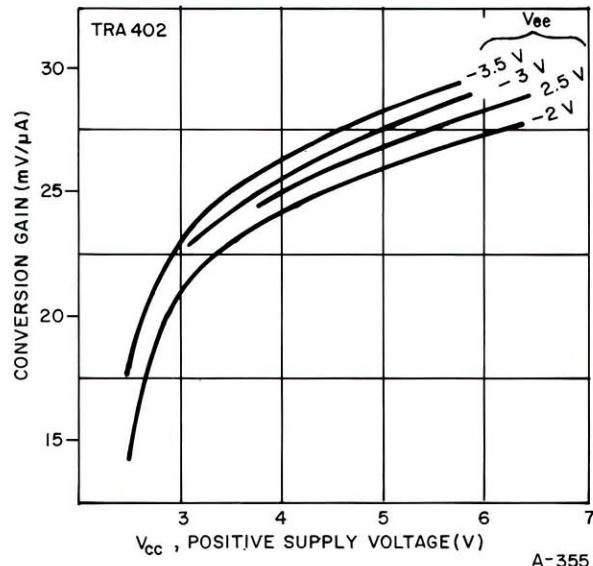
formulas allow for a residual DC standing current of 0.4 mA in the output emitter follower for good linearity.

The output of each TRA402 channel is a differential driver. For single ended applications, the unused output should be terminated symmetrically to the used output for stable operation.



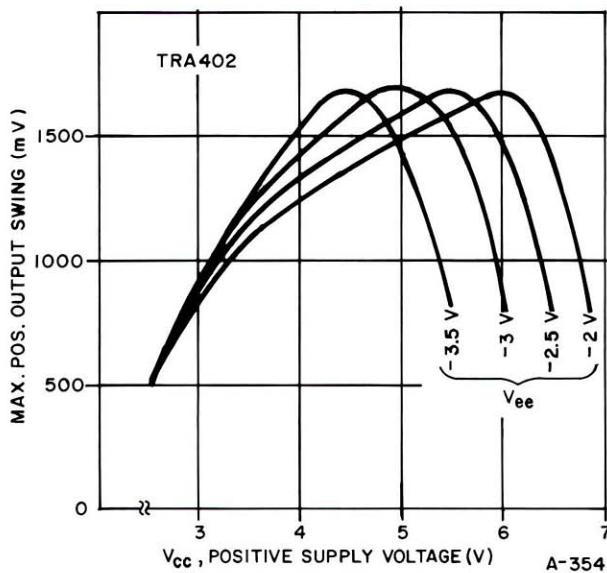
RMS output voltage noise versus V_{cc} . V_{ee} is not critical and can be set anywhere between -2.5 V and -3.5 V . The upper trace shows the noise when measured with a 350 MHz bandwidth, the lower trace was taken with 100 MHz bandwidth.

Figure 6



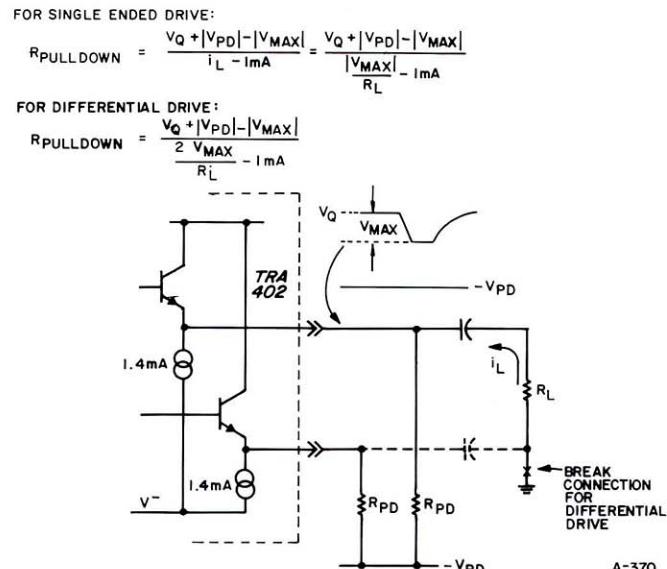
Conversion gain versus V_{cc} for values of V_{ee} between -2 V and -3.5 V . Data were taken with output terminated into 50Ω .

Figure 8



Maximum positive output voltage swing (into a 50Ω load) of TRA402 versus V_{cc} . The graph shows signal swing for various values of V_{ee} .

Figure 7



The Output

Figure 9

SPECIFICATIONS

Model TRA402

QUAD TRANSRESISTANCE CHAMBER AMPLIFIER

ABSOLUTE MAXIMUM RATINGS (above which useful life may be impaired)

Positive Supply Voltage	7 V
Negative Supply Voltage	− 4 V
Current at Amplifier Input	± 10 mA
Differential Input Current	± 10 mA
Maximum Continuous Power Dissipation (at 50°C still air)	0.75 W
Storage Temperature	− 65 to + 150°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	Symbol	Min.	Max.	Unit
Positive Supply Voltage	V_{CC}	3	6	V
Negative Supply Voltage	V_{EE}	− 2	− 3.5	V
Operating Temperature (still air)	T_A		50	°C
Operating Temperature (Air Flow 500 LFM)	T_{FA}		75	°C
Output Signal Current	I_{max}		20	mA

ELECTRICAL CHARACTERISTICS

Measured at $T = 25^\circ\text{C}$, $V_{CC} = + 5.0$ V, $V_{EE} = - 2.5$ V with AC-coupled outputs and a load of 50Ω paralleled by 5 pF unless otherwise specified. Note 1. See test setup (Figure 1).

PARAMETERS	Symbol	Min.	Typical	Max.	Units
Positive Supply Current	I_{CC}		40	50	mA
Negative Supply Current	I_{EE}		− 25	30	mA
Quiescent Input Voltage	V_{QI}	− 0.85	− 0.65	− 0.55	V
Input Noise (Note 2)	I_N		65	100	nA
Input Resistance	R_I	65	85	100	Ω
Input Resistance Stability	ΔR_I		0.3	0.45	%/ $^\circ\text{C}$
Input Capacitance	C_I		4	6	pF
Input Protection (50 pF, 2 kV)	E	1×10^{-4}			J
Gain (Note 3)	G	20	25	30	$\text{mV}/\mu\text{A}$
Gain Stability	ΔG		0.08	0.15	$\text{mV}/\mu\text{A}$
Quiescent Output Voltage	V_{QO}	0	0.5	1	V
Maximum Positive Output Swing	V_{max+}	1	1.5		V
Maximum Negative Output Swing	V_{max-}	75	150		mV
Integral Non Linearity (Note 5)	L		0.5	1.5	%
Output Resistance	R_O	20	30	40	Ω
Propagation Delay	T_{PD}	3	5	7	nsec
Risetime	t_R	—	3	6	nsec
Falltime	t_F	—	5	7	nsec

Note 1. For a package thermal resistance of $90^\circ\text{C}/\text{W}$.

Note 2. Noise with no external capacitance at input and with the typical noise bandwidth of 100 MHz.

Note 3. Gain measured with a $10 \mu\text{A}$ input signal.

Note 4. Without external pulldown resistor. Can be extended by the use of a pulldown resistor.

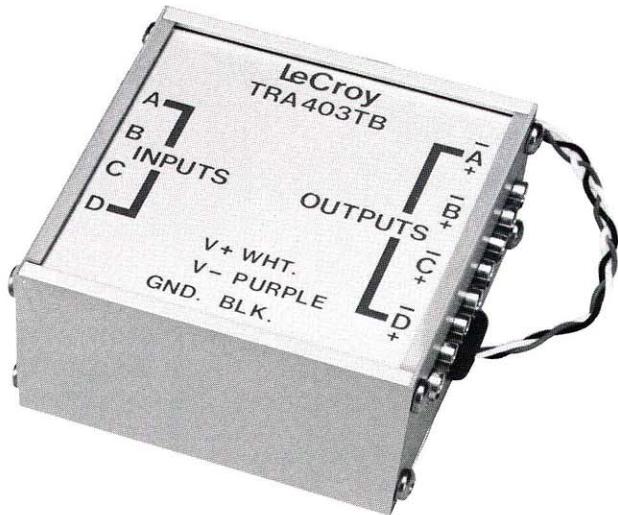
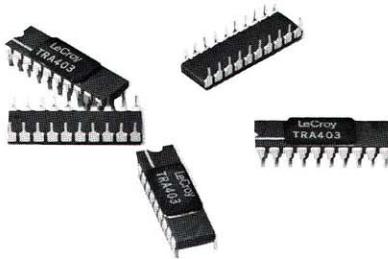
Note 5. For positive output voltage swing of 1 V with a load of $\geq 50 \Omega$.

TECHNICAL DATA

LeCroy

Model TRA403 Quad Micro Amplifier

- Silicon strip detectors
- RICH
- Drift chambers
- MWPC
- Low power
- High density
- Low noise



The LeCroy Model TRA403 four channel monolithic preamplifier is an extremely compact, wide band, low noise transimpedance amplifier. It is ideally suited for fast current pulse inputs obtained from a low shunt capacitance source. It can be used wherever total output charge is the key parameter. Signals in the fC regime can be processed by the device. Resolutions of $3-5 \times 10^{-16}$ C can be achieved for most applications. It requires a minimum of support components making it extremely compact in practical applications.

The TRA403 has been designed with low power as an important parameter. The device dissipates < 25 mW per channel. The circuit achieves low noise for applications where low shunt capacitance (<< 100 pF) is possible. A consequence of this constraint is that the device must be located in close proximity to the detector so that input stray capacitance is minimized. The TRA403 has differential outputs, allowing use of a balanced transmission line. Pulldown resistors are required on the outputs when driving a transmission line or other low impedance load. These would normally be located at the receiving end of the transmission line to further reduce power dissipation at the detector.

For the purposes of evaluation and prototyping, the TRA403 DIP is available mounted on a printed circuit board. The device, Model TRA403TB, is strongly recommended for this purpose. Inputs and outputs are provided via Lemo connectors. The board is contained in an aluminum enclosure, providing RF shielding for the device.

SPECIFICATIONS

Model TRA403

QUAD MICRO AMPLIFIER

Note: Unless otherwise stated, all specifications at $T = 25^\circ\text{C}$, $V^+ = +3.2\text{ V}$, $V^- = -1.5\text{ V}$, $R_L > 1\text{ k}\Omega$, $C_L < 10\text{ pF}$.

Channels:	Four
Inputs:	One per channel; accepts negative and positive current signals. Quiescent level 0.7 V, nominal.
Input Impedance:	Typically $300\ \Omega$ DC. Intended to be driven from a current source.
Outputs:	Two per channel; differential. Quiescent level +1.4 nominal. Output impedance, $10\ \Omega$ typical. Output swing, $\pm 0.5\text{ V}$ for linear operation. Output source current, 12 mA typical. Output sink current, -0.6 mA* typical.
Overload Recovery:	< 100 nsec for a $20\ \mu\text{A}$ input pulse.
Interchannel Cross Talk:	3% typical
Linear Range:	$> \pm 0.5\text{ V}$, each output
Gain:	$330\text{ mV}/\mu\text{A} \pm 15\%$ per output, $660\text{ mV}/\mu\text{A}$ differentially. ($Q_{\text{out}}/Q_{\text{out}} = 3000$ with $R_L = 100\ \Omega$)
Power:	25 mA at +3.2 V, nominal 12.5 mA at -1.5 V, nominal Total power < 25 mW per channel (static).
Rise and Falltimes:	7 nsec typical (9.5 nsec max.) for $C_S < 10\text{ pF}$.
Noise (Wideband):	< 25 nA rms for $C_S = 5\text{ pF}$. < 35 nA rms for $C_S = 10\text{ pF}$. 1900 electrons for 20 nsec gate, $C_S = 2\text{ pF}$. See Figure 1.
Packaging:	20-pin DIP

*Low impedance loads may require additional output sink current, achieved by adding a pulldown resistor on each output (see Application Notes).

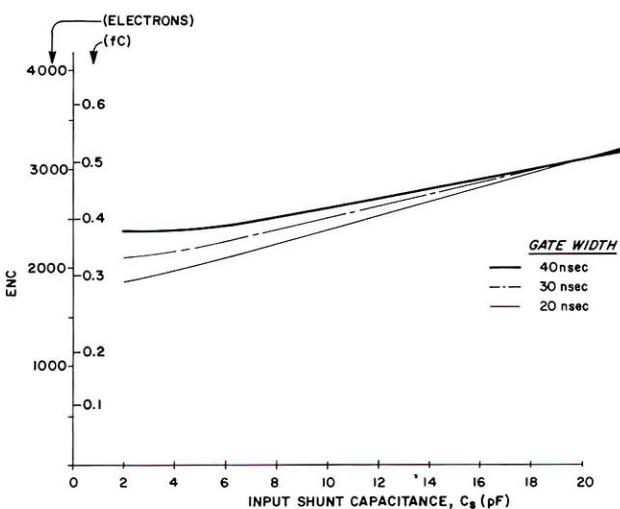
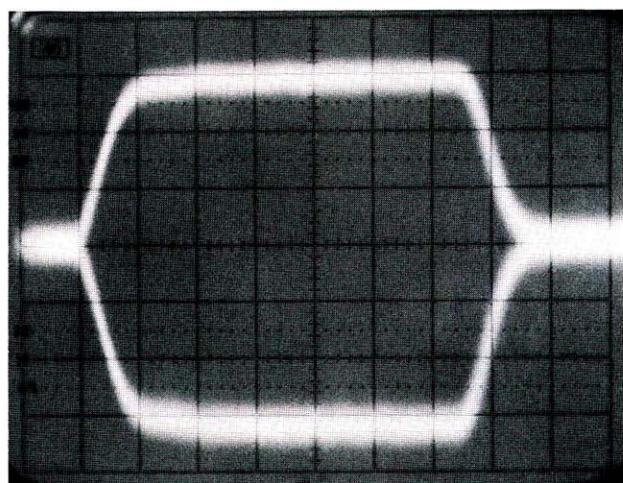


Figure 1



Output Wave Shape

Typical differential output signals of a TRA403 driven with a square wave input signal of $0.5\ \mu\text{A}$ in amplitude and with fast transition times.

Scale: Horizontal 10 nsec/div.
Vertical 50 mV/div.

Figure 2

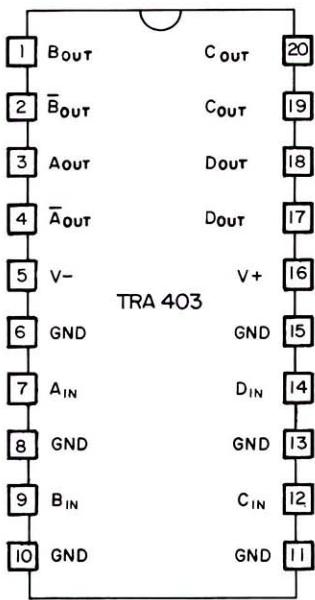
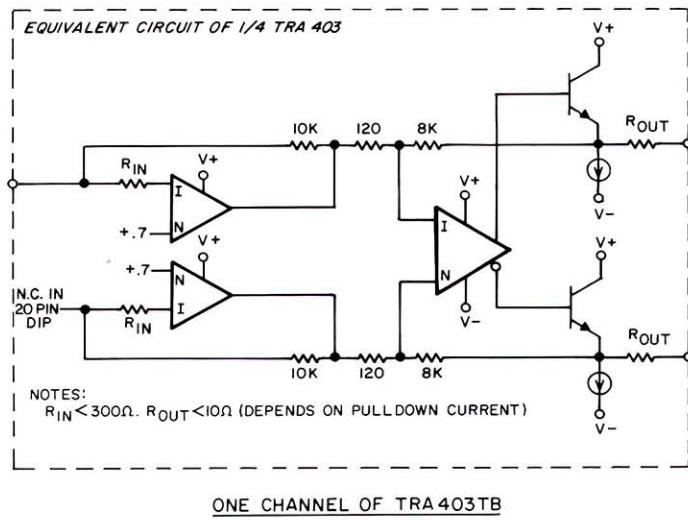


Figure 3



ONE CHANNEL OF TRA 403TB

Figure 4

APPLICATION NOTES

Layout

Good high frequency layout techniques are essential. The circuit should be built with continuous ground plane on one side and as much ground as possible on the reverse. Input connections should be as short as possible with ground between the input traces to minimize cross talk. The power supply buses and bypass capacitors must be kept as far from the input signal as possible. The power supply buses must be bypassed carefully, preferably using $.01 \mu F$ chip capacitors with good high frequency response placed as close to the package pins as possible. Also use of an appropriate series inductor and large value tantalum capacitor to ground are recommended to provide good rejection of power supply transients. When used in magnetic fields, the inductor should be replaced by a resistor of several ohms. If socketing of the chip is required, insertion pins such as Berg Minisert pins 75060-12 are recommended. Sockets, connectors, and cables all add shunt capacitance and can seriously degrade the noise performance if not minimized or avoided. Typical shunt capacitances are: 1 pF per Berg pin, 1 pF per Lemo connector, 2 pF from DIP package, 0.3 pF/inch in micro strip, 30 pF/ft of coaxial cable and 1 pF shunting resistor leads.

Inputs

The input impedance is a function of V^+ . At + 3 V it is roughly 300Ω (DC).

The quiescent level of the input is approximately 0.7 V. To avoid a DC current which might saturate the amplifier, the input should be AC coupled or should have a large DC resistance ($> 20 M\Omega$) to ground.

Input Protection

For applications involving detectors with high voltages, input protection is recommended. A fast diode such as a 1N4448 connected from the input to ground, cathode to input, can be employed. This will add 2-3 pF of shunt capacitance to the input, resulting in some degradation of the noise performance.

Outputs

The output of the TRA403 rests quiescently at + 1.4 V. The differential outputs are driven by emitter followers which can drive up to 10 mA positive and $600 \mu A$ negative. For linear operation, the outputs should not be allowed to saturate. As a practical consequence in most applications, external pulldown resistors will be required unless the load is of high impedance ($> 500 \Omega$). See Figure 5.

If pulldown resistors are employed, they should be installed on both outputs to preserve symmetry which plays a major role in the stability of the device. The resistors can be connected to V^- (- 1.5 V). The value required for the pulldown resistors can be calculated by using the following equations or determined from the graphs supplied.

Note that the quiescent output voltage, V_Q , and the standing current, I_S , as given are nominal values which will be process dependent as well as load dependent. The values given above are more accurate for large ($> 500 \Omega$) R_L .

To drive loads $< 500 \Omega$ requires R_{PD} to be small to obtain sufficient voltage swing. For example, if a 100Ω load is to be differentially driven to a 500 mV maximum amplitude (negative excursion of 250 mV), then

$$V_{\max} = 250 \text{ mV}$$

$$R_L = 50 \Omega$$

$$R_{PD} = 275 \Omega$$

If a low load impedance ($< 100 \Omega$) is being driven, both of the differential output legs must have the same impedance or the circuit may oscillate. See Figures 6 and 7.

General

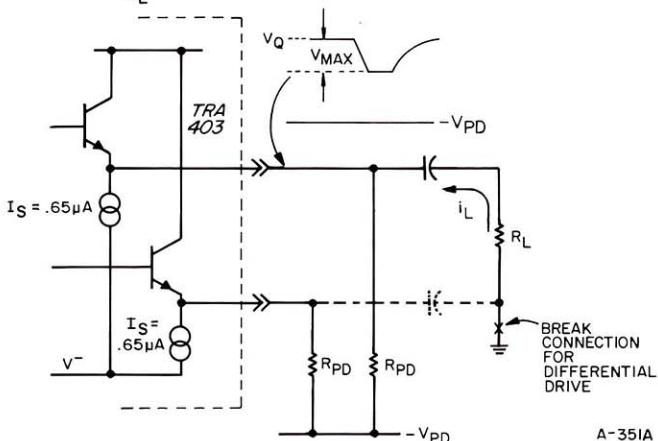
The linearity and input noise of the amplifier have been measured using a gated integrating ADC with a 20 nsec gate and no shaping. The unit is linear to 1% and the noise measurements indicate a sigma of 0.33 fC referred to the input. The noise increases both with source capacitance and with gate width. See Figure 1.

FOR SINGLE ENDED DRIVE:

$$R_{PULLDOWN} = \frac{V_Q + |V_{PD}| - |V_{MAX}|}{i_L - 0.3 \text{ mA}} = \frac{V_Q + |V_{PD}| - |V_{MAX}|}{\frac{|V_{MAX}| - 0.3 \text{ mA}}{R_L}}$$

FOR DIFFERENTIAL DRIVE:

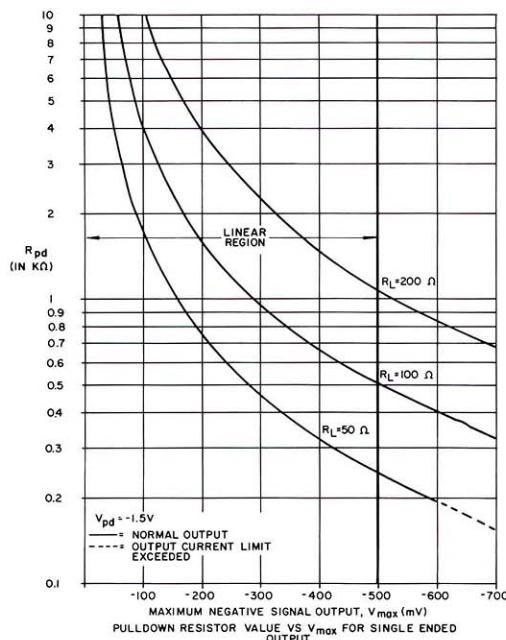
$$R_{PULLDOWN} = \frac{\frac{V_Q + |V_{PD}| - |V_{MAX}|}{2}}{\frac{|V_{MAX}| - 0.3 \text{ mA}}{R_L}}$$



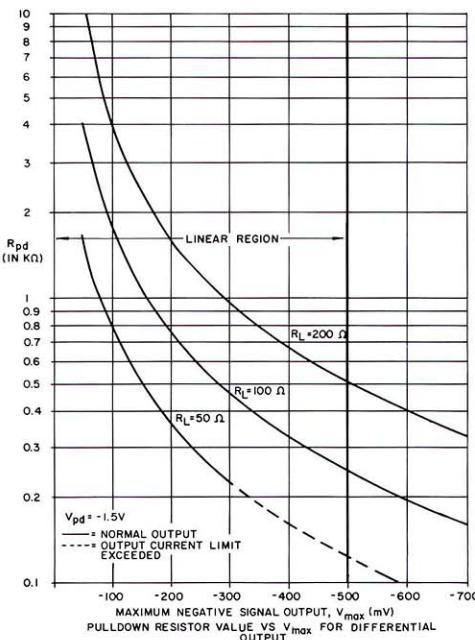
A-35IA

- Notes:**
1. For single ended output drive the unused output requires a pulldown resistor (equal in value to the used outputs' pulldown).
 2. The calculated value for the pulldown resistors in the above equation allows for a minimum current of 0.35 mA standing in each output emitter follower.

Figure 5
Output Driver Considerations



B-403



B-404

Figure 6

Figure 7

TECHNICAL DATA

LeCroy

Monolithic Circuit/Type TRA1000 Charge/Current Pulse Preamplifier

FEATURES

- Low noise
- Low cost
- Low power dissipation
- Versatile configuration flexibility
- Very wide dynamic range
- Monolithic
- Excellent linearity
- >5000 open-loop voltage gain
- Current or charge input modes
- Inverting and non-inverting outputs
- Directly drives twisted pair or 50 Ω cable

Ideal for Wire Chamber Linear Measurements

The LeCroy Model TRA1000 monolithic preamplifier is a versatile, economical, low-noise device which can be used either as a current-to-voltage preamplifier or as a charge-to-voltage preamplifier. The device has been designed for use with negative input signals; however, it may also be configured for operation with positive inputs. The various options are selected through the use of external components.

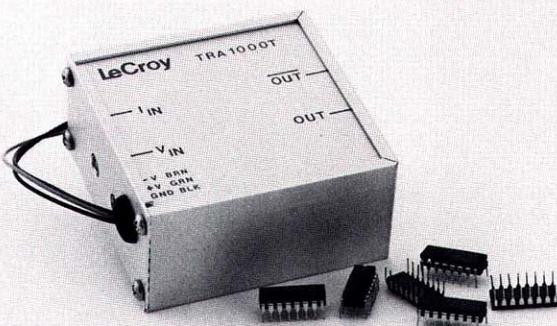
The TRA1000 has been designed for direct connection to a variety of detectors. Its low noise and low input impedance make it ideal for use with proportional wire chambers even when resistive wire is used for position measurements. The device also finds application with photomultipliers when the economy of low-gain tubes is a factor or dynamic range considerations are important. When used in conjunction with both the last dynode and the anode signals, exceptional dynamic range can be achieved by selecting different gains for the two devices. In this way high- and low-sensitivity channels are configured.

The linearity of the preamplifier is excellent for a wide range of input risetimes and selected gains. The linear range of output is 0

to 1 V, even for 50 Ω loads. In the applications discussed below typical linearity has been measured in conjunction with a LeCroy 2280-Series 12-bit ADC. The result is typically <0.5% of reading, with proper compensation.

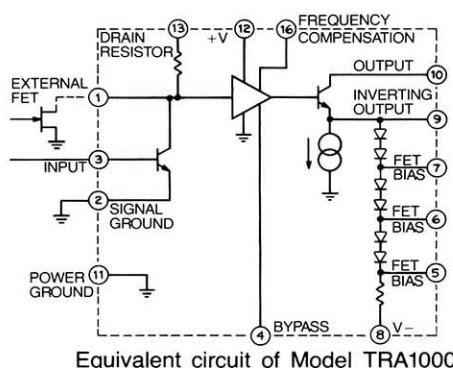
The equivalent input noise of the preamplifier is as low as $2 \text{ pA}/\sqrt{\text{Hz}}$ in some configurations. In the applications documented below noise measurements are quoted in rms pC, referred to the preamplifier input. The LeCroy 2280-Series current-integrating ADC's, employing a 500 nsec wide gate, were used to characterize the current-to-voltage configurations. For the charge-to-voltage configurations a peak-sensing 2280-Series ADC was used. The output noise in rms mV is also given for each case below.

The low price, compact packaging, and low power dissipation of the Model TRA1000 make it an ideal choice for use in large-scale systems applications. It is particularly suited for use as a current-sensitive preamplifier for MWPC analog position measurements. The Model TRA1000 is a low-cost, high-performance answer to a wide range of charge-sensitive and current-sensitive preamplifier needs.



Model TRA1000T is a printed circuit card allowing prototyping and evaluation of the TRA1000.

LOGIC DIAGRAM (TOP VIEW)



SPECIFICATIONS*

MONOLITHIC CIRCUIT/TYPe TRA1000

CHARGE/CURRENT PULSE PREAMPLIFIER

Gain:	>5000 open-loop voltage gain into 50 Ω load. Current-mode and charge-mode gains are determined by external feedback elements.
Linearity:	<±0.5% integral, into 50 Ω load.
Rated Output:	1.0 V into 50 Ω load.
Output Impedance:	Inverted output: 1.8 mA sink current; 20 mA source current. Non-inverted output: 20 mA sink current; 1.8 mA source current.
Risetime:	<1 Ω, with $R_F = 2.7 \text{ k}\Omega$; see specifications below.
Falltime:	See specifications below.
Input Noise:	See specifications below.
Input Bias Current:	See specifications below.
Input Voltage:	<7 μA.
Temperature Range:	Quiescently 700 mV. 0°C to 70°C.
Power Supply Requirements:	Standard operation: +12 V @ 6 mA. Two-voltage operation (for FET input stage or with buffered output): +12 V @ 6 mA + FET drain current (~10 mA) and buffer current (~26 mA); -12 V @ -2 mA + buffer current (~26 mA).
Rated Voltage, Quiescent Current	16-pin plastic DIP.
Package:	

*All specifications are typical at 25°C and the rated supply voltages. Currents flowing into the amplifier are considered to be positive.

ALL SPECIFICATIONS SUBJECT TO CHANGE

APPLICATION NOTES

The TRA1000 input consists of a special geometry low-noise common emitter transistor as part of a cascode stage. The emitter connection is isolated from the power ground and is brought out on pin 2. This input ground must be externally referenced to power ground by the user. A frequency compensation point on the output of the cascode stage is available on pin 16. Compensation may not be required for the highest gain operation. Compensation for each of the example circuits shown in the accompanying schematics is presented only as a guide. Precise component values will depend upon details of the layout, the input source characteristics, etc. Compensation values should be selected to avoid oscillation and to minimize overshoot of the output.

The output stage consists of a single transistor having both collector and emitter external connections, allowing either differential or single-ended outputs to be used. The collector (pin 10) provides the non-inverting output and the emitter (pin 9) provides the inverting output. Due to quiescent DC levels, the outputs must be capacitively coupled. For proper operation the outputs must be loaded symmetrically.

The TRA1000 can operate from a single power supply, as shown in Fig. 1. Pin 8 is connected to the chip substrate and must always be connected to the most negative power supply used. When an input FET or an output buffer is used, two power supplies are required. Power supply ripple should be below 3 mV (peak-to-peak) for low-noise performance. A series inductor of 1 μH with a 6.8 μF capacitor to ground provides excellent rejection of power supply transients. For highest gain operation a π network should be used. The isolation of input ground and power ground allows for protection against possible noise due to ground loops or pickup which could feed through to the input stage. For most applications the input ground at Pin 2 can be tied directly to the circuit board ground plane. The power ground, Pin 11, should be tied to the ground plane. A bypass capacitor from Pin 4 to ground is required for all circuit configurations. In many cases a value as small as 0.01 μF may be used. For critical low noise applications use 6.8 μF.

For optimum performance good wiring techniques are essential. The circuit must be built on a printed circuit board having a continuous ground plane on one side. The input and feedback connections must be kept as short as possible to minimize stray capacitance. If a DIP socket is desired, a low-profile version should be used, and insertion pins are preferable.

The gain of the TRA1000 is determined by the feedback element selected. See Figures 1, 2, and 3. If a resistor is employed, the TRA1000 becomes a transresistance amplifier; i.e., a current-to-voltage device. The transfer gain will be determined by the value of the resistor. For example, a 10 kΩ resistor offers 10 mV/μA gain. When used in this mode, the TRA1000 should be driven from a current source such as a photomultiplier anode or an ionization chamber. When driven from a voltage source, such as an amplifier, a series input resistor is required by the TRA1000. In this case the voltage gain of the TRA1000 is

When the TRA1000 employs a capacitor as its feedback element, it operates as a current-integrating or charge-sensitive amplifier. Its gain is determined by the value of the capacitor. For example, with 2 pF as the feedback element, the

TRA1000 has a gain of 0.5 V/pC. In this mode it is necessary to employ a resistor in parallel to the feedback capacitor in order to provide a discharge path for the capacitor and thereby determine the falltime of the amplifier and also maintain necessary DC feedback for proper biasing of the input.

Applications requiring a faster risetime than specified in the cases on the following pages may be accommodated by supplying more current to the TRA1000 input stage. This may be accomplished by inserting a 1.5 KΩ resistor between pins 12 and 13 (labeled points 28 and 29 on the TRA1000TB). This decreased risetime will be gained at the sacrifice of increased noise. For example, if Case 7 is modified by addition of this 1.5 KΩ resistor then a risetime of 15 nsec may be achieved but the typical noise performance will be about 0.8 fC (HWHM) rather than 0.4 fC.

The input voltage of the TRA1000 is quiescently +700 mV. When used with an input FET, the quiescent input voltage will be different but also non-zero. As a result, it is often necessary to AC-couple the input, eliminating a DC path to ground. For many applications direct coupling may be possible. When used in conjunction with an ideal current source such as an ionization chamber, a proportional chamber, or a photomultiplier anode, direct coupling may be used as long as any resistance to ground is large compared to the feedback resistance.

The input to the TRA1000 is a virtual ground. In the applications listed below the input impedance is given. In most cases it is less than 20 Ω. As a result, when driven from a transmission line, proper termination requires a series resistance. Choose a value so that when added to the input impedance, proper termination is obtained. For fast edges an RC from the input to ground may be required. Some common mode noise rejection may be achieved if the ground return of the input is tied only to pin 2 rather than to chassis ground. In this case the ground reference of the TRA1000 circuit and the ground of the source must be tied common. Although the input circuit provides some protection against chamber breakdown, it is suggested that the clamp circuit shown in Figure 1 be employed.

The inverting output can swing >1 V in the positive direction. Since this point is used for feedback, the TRA1000 is ideally suited for negative inputs. For use with positive inputs, an external pnp transistor should be used as a buffer. See Figure 3. A pnp transistor with $f_T \geq 850 \text{ MHz}$ should be used.

The input bias current of the TRA1000 is approximately 5 μA. This value sets an upper limit on the magnitude of the feedback resistance ($R \leq 100 \text{ k}\Omega$). For applications requiring high transimpedance gain or current-integrating operation with a large time constant, it is necessary to replace the input transistor with a FET. See Figure 2. Note that pins 2 and 3 are connected to ground. A junction-type n channel FET is recommended. The T1575 or 2N5485 are common in this application.

The output of the TRA1000 can be used to drive 100 Ω twisted-pair cable. A typical drive circuit is shown in Figure 4. When only the inverting output is to be used, the pull-up resistor and AC coupling capacitor on the noninverting output may be eliminated. In this case, pin 10 should be connected to +12 V.

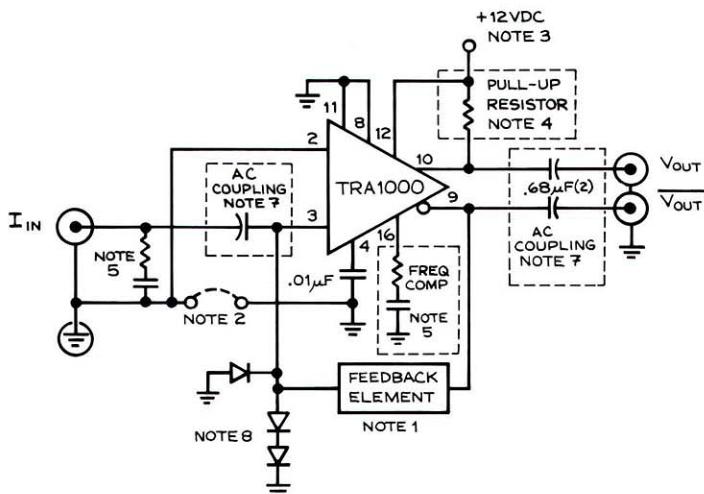


FIGURE 1 TYPICAL CONFIGURATION

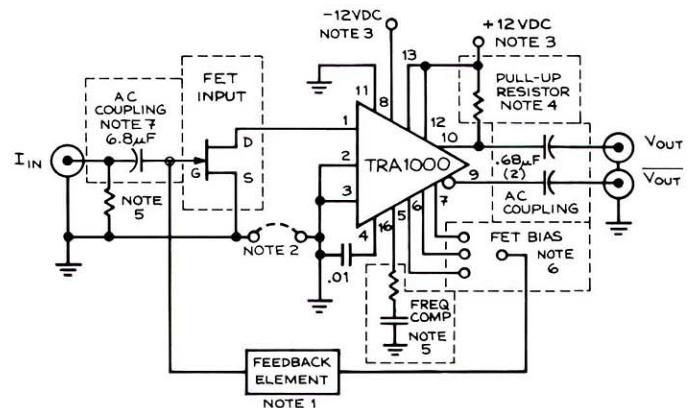


FIGURE 2 FET INPUT CONFIGURATION

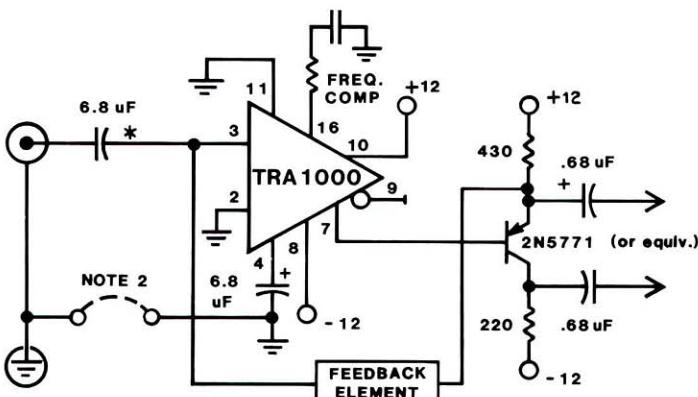


FIGURE 3 BUFFERED OUTPUT CONFIGURATION

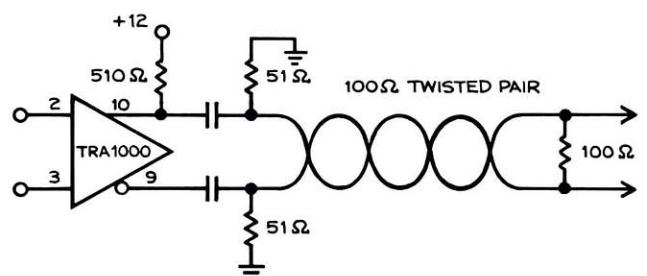


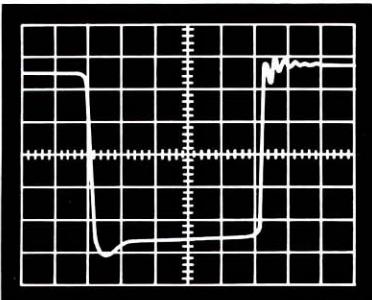
FIGURE 4 TWISTED-PAIR OUTPUT

NOTES:

- For a current-to-voltage amplifier, the gain is determined by a feedback resistor, where $V_{OUT} = I_{IN} \cdot R_F$. For a charge-to-voltage amplifier the gain is determined by a feedback capacitor, where $V_{OUT} = Q_{IN}/C_F$.
- Wire jumper between "clean" ground (⏚) and "power" ground (⏚).
- All voltage power supplies should be decoupled with a series 100 μH inductor and a 6.8 μF bypass capacitor to ground.
- Open collector output. A 510 Ω pull up resistor was used for device tests.
- Compensation networks.
- Selected with jumper to match FET V_{GS} (off) characteristic.
- Polarity of input capacitor depends on D.C. level on input.
- External protection (for chamber breakdown).

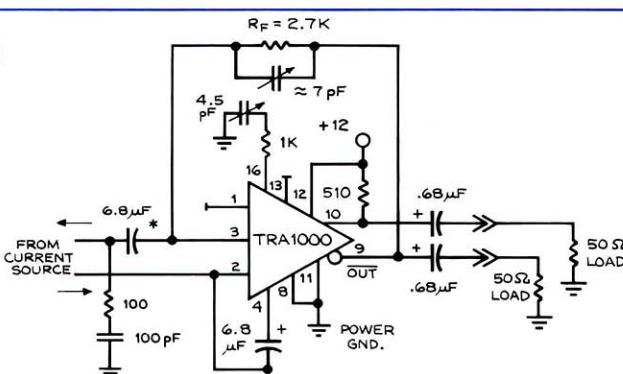
CASE 1 For low-gain (2.7 mV/μA) applications with negative inputs.

RESPONSE TO RECTANGULAR INPUT

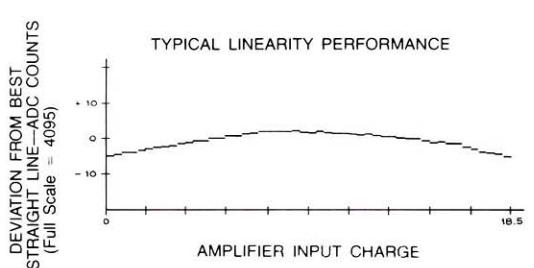
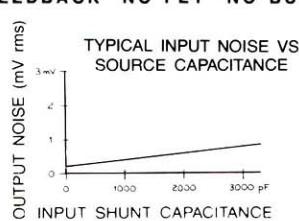


100 nsec/Horizontal Division
200 mV/Vertical Division

Risetime: 25 nsec (10% to 90%)
Falltime: 16 nsec (10% to 90%)
Propagation Delay: 22 nsec
Output Noise: 370 μV rms typical (≥ 175 MHz Bandwidth)
Input Impedance: 0.4 Ω

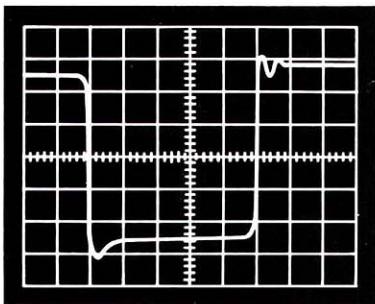


2.7 K FEEDBACK NO FET NO BUFFER

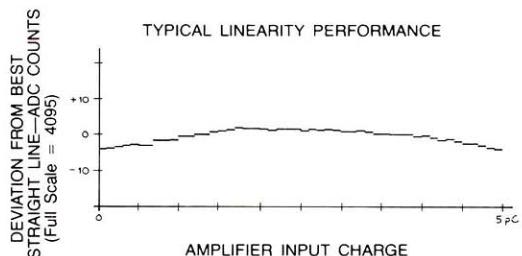
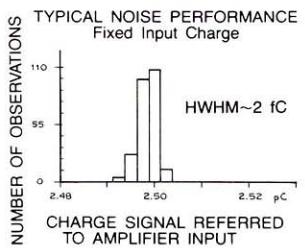
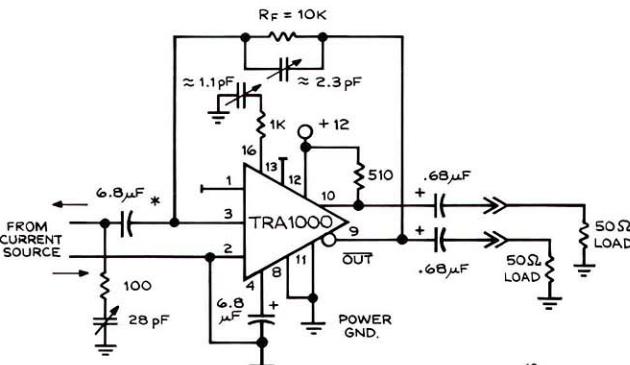


CASE 2 For intermediate-gain (10 mV/ μ A) applications with negative inputs.

RESPONSE TO RECTANGULAR INPUT

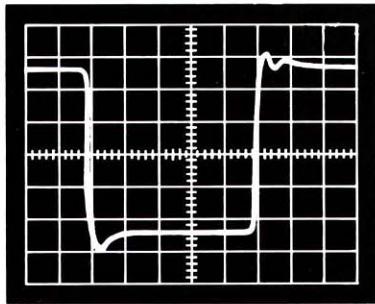


Risetime: 24 nsec (10% to 90%)
Falltime: 18 nsec (10% to 90%)
Propagation Delay: 24 nsec
Output Noise: 340 μ V rms typical (≥ 175 MHz Bandwidth)
Input Impedance: 1.5 Ω

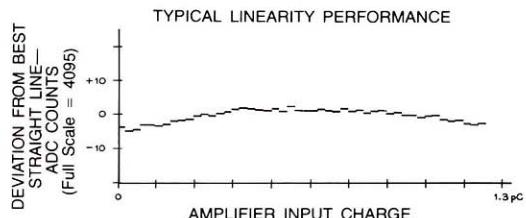
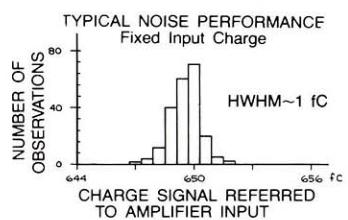
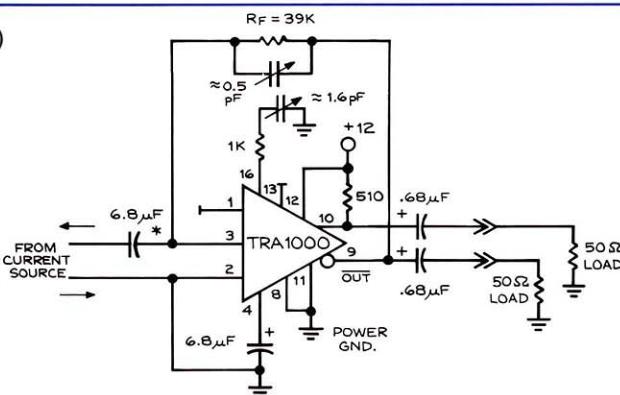


CASE 3 For high-gain (39 mV/ μ A) applications with negative inputs.

RESPONSE TO RECTANGULAR INPUT

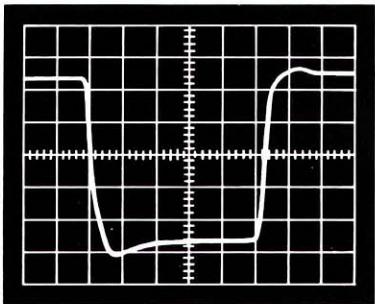


Risetime: 26 nsec (10% to 90%)
Falltime: 24 nsec (10% to 90%)
Propagation Delay: 28 nsec
Output Noise: 360 μ V rms typical (≥ 175 MHz Bandwidth)
Input Impedance: 5 Ω

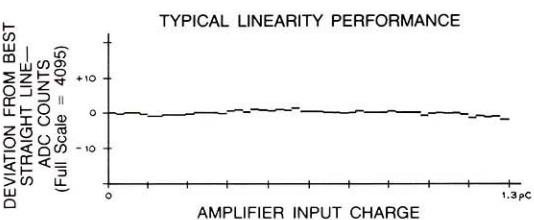
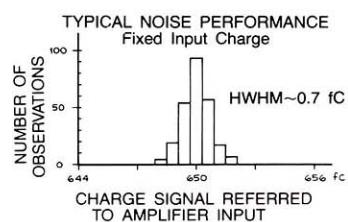
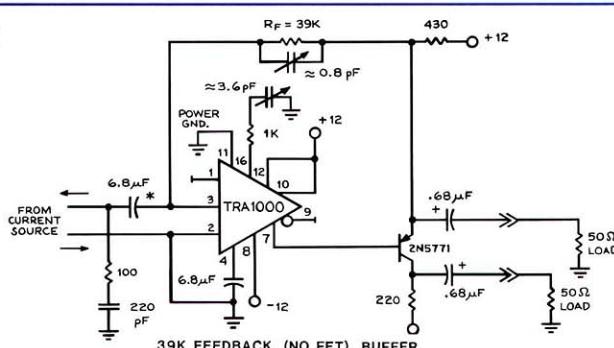


CASE 4 For high-gain (39 mV/ μ A) applications with either negative or positive inputs.*

RESPONSE TO RECTANGULAR INPUT



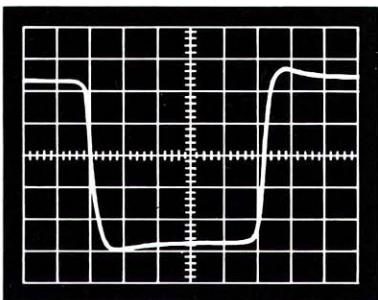
Risetime: 36 nsec (10% to 90%)
Falltime: 32 nsec (10% to 90%)
Propagation Delay: 28 nsec
Output Noise: 460 μ V rms typical (≥ 175 MHz Bandwidth)
Input Impedance: 8 Ω



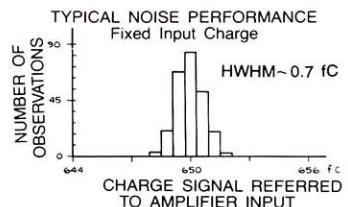
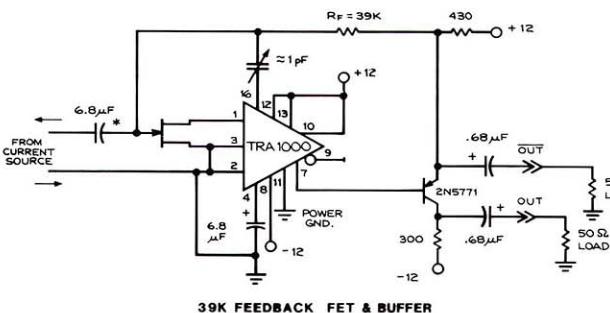
*For positive inputs select either Pin 5, 6, or 7. (By measuring Pin 16, the tap that provides a voltage (at Pin 16) closest to +9 V should be used.)

CASE 5 For high-gain ($39 \text{ mV}/\mu\text{A}$), low-noise applications with either negative or positive inputs.*

RESPONSE TO RECTANGULAR INPUT

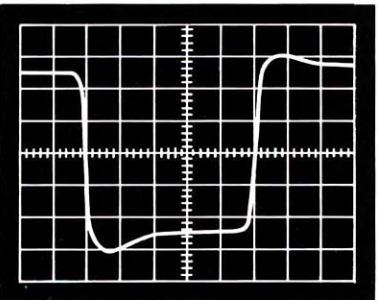


Risetime: 36 nsec (10% to 90%)
Falltime: 40 nsec (10% to 90%)
Propagation Delay: 30 nsec
Output Noise: 300 μV rms typical ($\geq 175 \text{ MHz}$ Bandwidth)
Input Impedance: 10 Ω

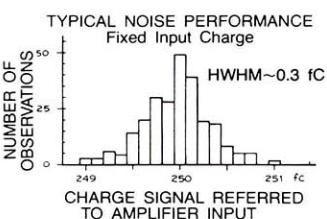
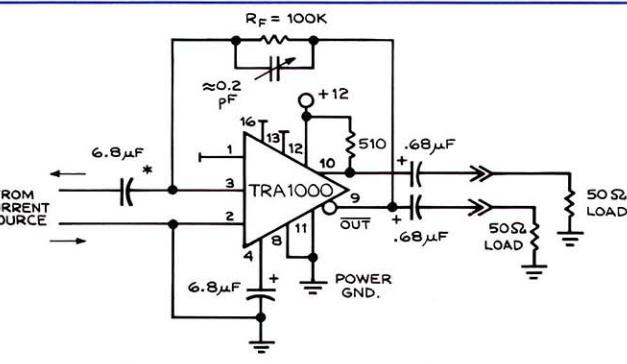


CASE 6 For very-high-gain ($100 \text{ mV}/\mu\text{A}$) applications with negative inputs.

RESPONSE TO RECTANGULAR INPUT

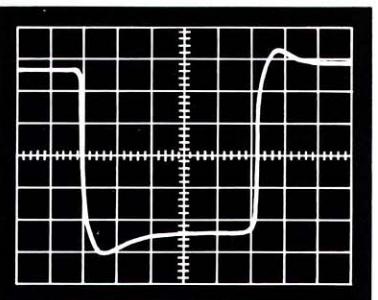


Risetime: 38 nsec (10% to 90%)
Falltime: 36 nsec (10% to 90%)
Propagation Delay: 32 nsec
Output Noise: 460 μV rms typical ($\geq 175 \text{ MHz}$ Bandwidth)
Input Impedance: 20 Ω

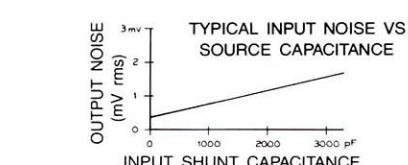
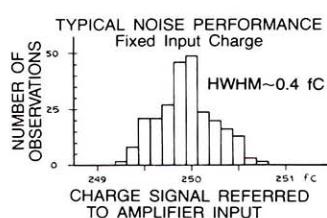
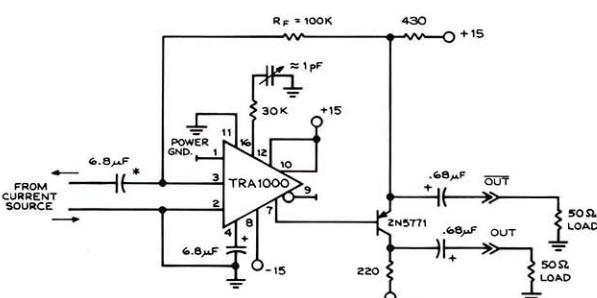


CASE 7 For very-high-gain ($100 \text{ mV}/\mu\text{A}$) applications with either negative or positive inputs.*

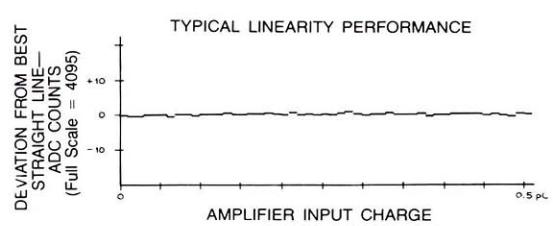
RESPONSE TO RECTANGULAR INPUT



Risetime: 36 nsec (10% to 90%)
Falltime: 34 nsec (10% to 90%)
Propagation Delay: 32 nsec
Output Noise: 590 μV rms typical ($\geq 175 \text{ MHz}$ Bandwidth)
Input Impedance: 20 Ω

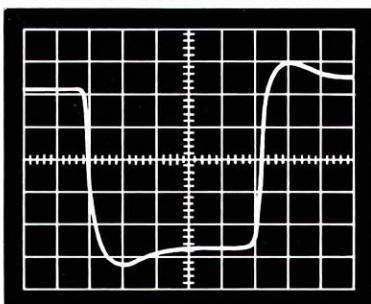


*For positive inputs select either Pin 5, 6, or 7. (By measuring Pin 16, the tap that provides a voltage (at Pin 16) closest to +9 V should be used.)

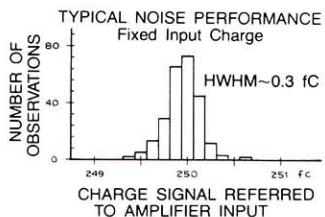
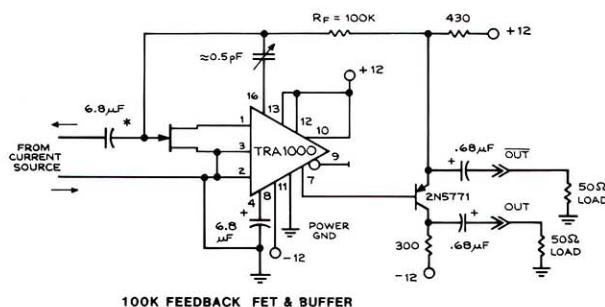


CASE 8 For very-high-gain (100 mV/ μ A), low-noise applications with either negative or positive inputs.*

RESPONSE TO RECTANGULAR INPUT

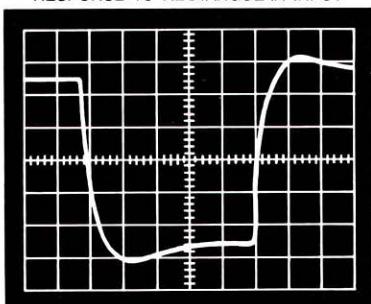


Risetime: 52 nsec (10% to 90%)
Falltime: 52 nsec (10% to 90%)
Propagation Delay: 40 nsec
Output Noise: 380 μ V rms typical
(\geq 175 MHz Bandwidth)
Input Impedance: 20 Ω

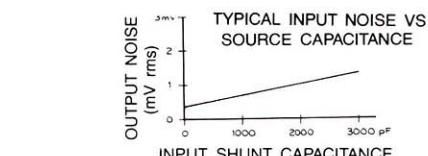


CASE 9 For extremely-high-gain (270 mV/ μ A) applications with either negative or positive inputs.*

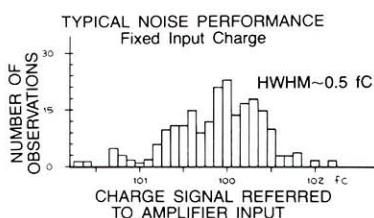
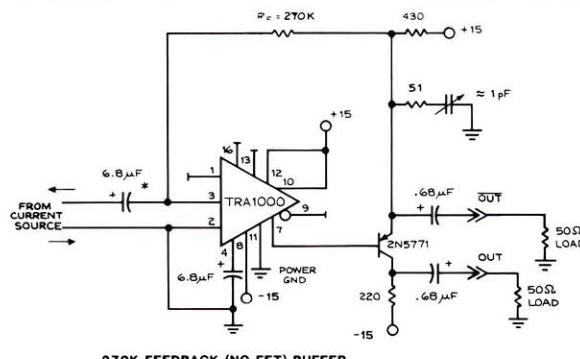
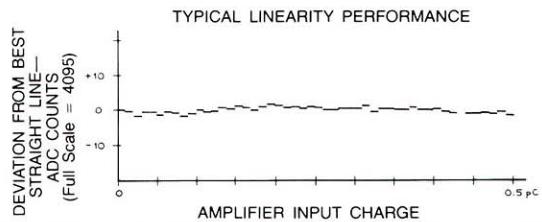
RESPONSE TO RECTANGULAR INPUT



Risetime: 64 nsec (10% to 90%)
Falltime: 62 nsec (10% to 90%)
Propagation Delay: 40 nsec
Output Noise: 840 μ V rms typical
(\geq 175 MHz Bandwidth)
Input Impedance: 30 Ω

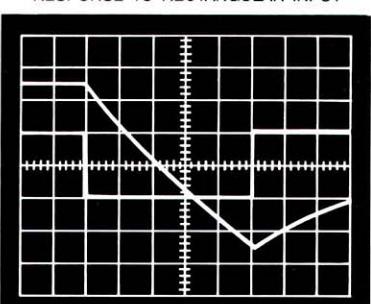


*For positive inputs select either Pin 5, 6, or 7. (By measuring Pin 16, the tap that provides a voltage (at Pin 16) closest to +9 V should be used.)

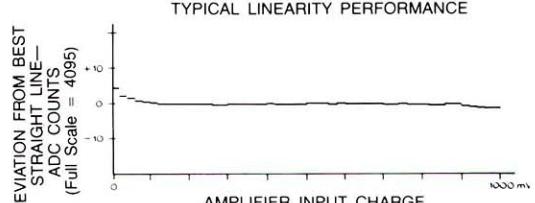
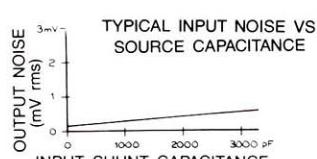
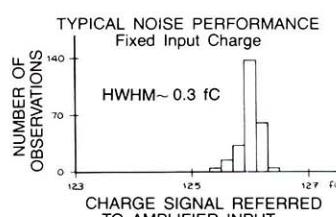
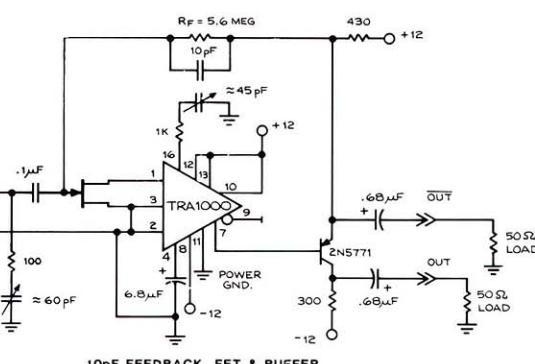


CASE 10 For low charge-to-voltage gain (0.1 V/pC).

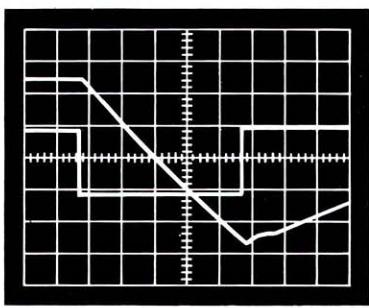
RESPONSE TO RECTANGULAR INPUT



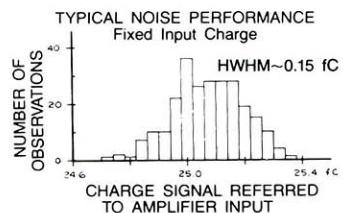
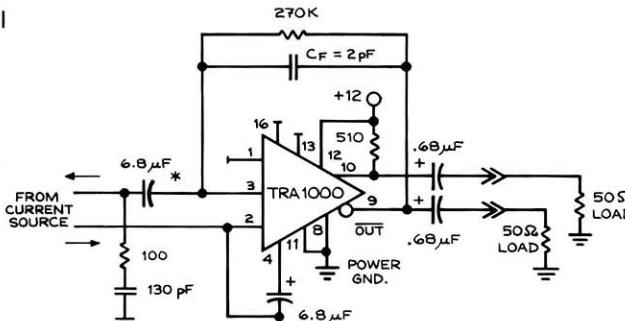
Output Noise: 285 μ V rms typical (\geq 175 MHz Bandwidth)
Input Impedance: 400 Ω



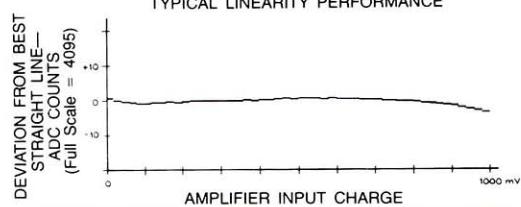
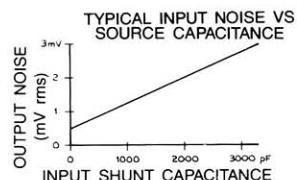
CASE 11 For high charge-to-voltage gain (0.5 V/pC) with fast tail (500 nsec.)



50 nsec/Horizontal Division
200 mV/Vertical Division

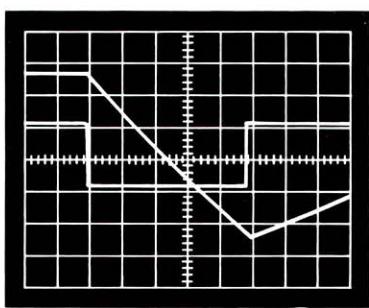


270K - 2pF FEEDBACK NO FET NO BUFFER

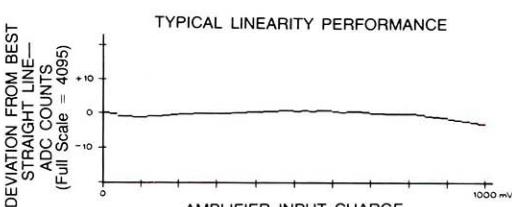
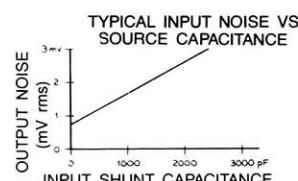
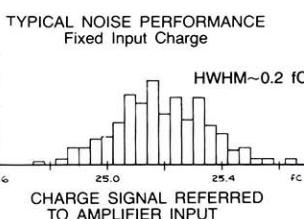
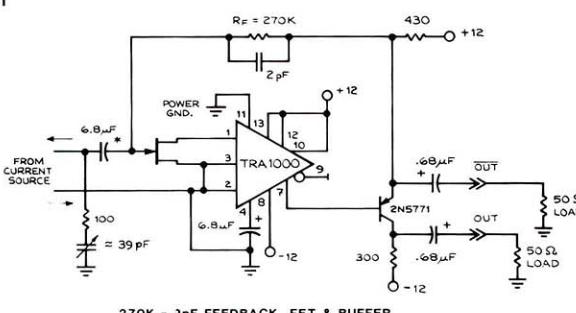


Output Noise: 400 μ V rms typical (≥ 175 MHz Bandwidth)
Input Impedance: 100 Ω

CASE 12 For high charge-to-voltage gain (0.5 V/pC) with fast tail (500 nsec.)

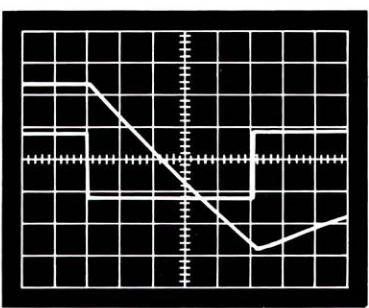


50 nsec/Horizontal Division
200 mV/Vertical Division

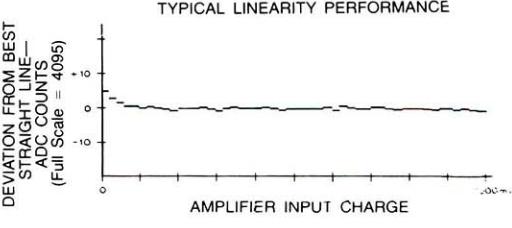
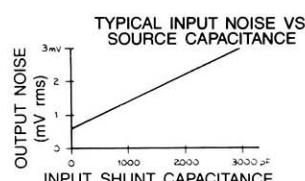
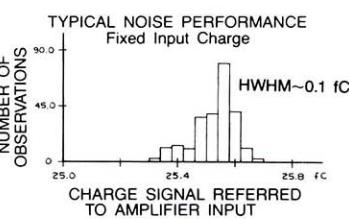
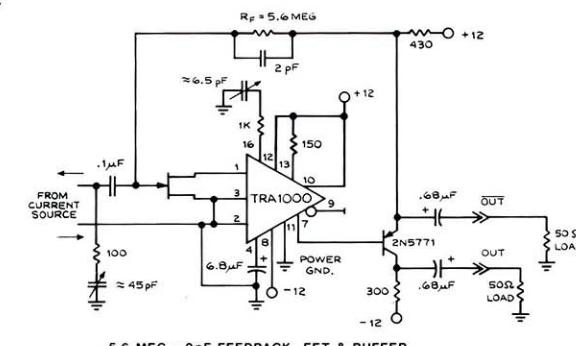


Output Noise: 560 μ V rms typical (≥ 175 MHz Bandwidth)
Input Impedance: 40 Ω

CASE 13 For high charge-to-voltage gain with slow tail (10 μ sec.).



500 nsec/Horizontal Division
200 mV/Vertical Division



Output Noise: 310 μ V rms typical (≥ 175 MHz Bandwidth)
Input Impedance: 320 Ω

TECHNICAL DATA

LeCroy

Model VV100B Hybrid Circuit Wideband Pulse Amplifier

- **WIDE BANDWIDTH** risetime: <2 nsec
- **DIRECT-COUPLED DESIGN** permits high rate application without baseline shifts.
- **10 \times GAIN, CASCADABLE** to 1000 \times for direct compatibility with a wide range of input amplitude applications.
- **EXCELLENT DC STABILITY** (<1 mV long term) assures optimum performance in DC coupled applications.

The LeCroy Model VV100B is a wide bandwidth, gain-of-10 pulse amplifier packaged as a standard 16-pin DIP hybrid circuit. Representing a major advance in fast amplifier bandwidth, stability, dynamic range, and general utility, the VV100B provides unprecedented performance in demanding direct-coupled, high-duty-cycle applications.

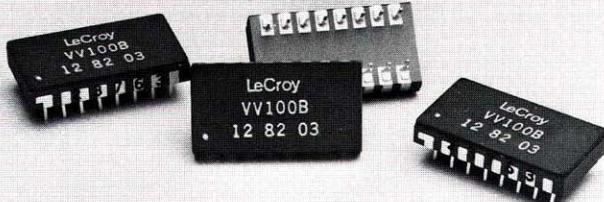
A new high speed amplifier circuit design makes the performance of the VV100B virtually independent of external variables such as supply voltages or temperature.

- **$\pm 0.2\%$, INTEGRAL LINEARITY** to outputs of -3 V.
- **LOW IMPEDANCE OUTPUT** designed to drive two 50 Ω loads, allowing the amplified signal to be used directly for both logic and analog functions.
- **COMPACT PACKAGING** permits the complete amplifier to be mounted near the pulse source in a standard 16-pin DIP socket, thereby reducing amplification of extraneous noise.

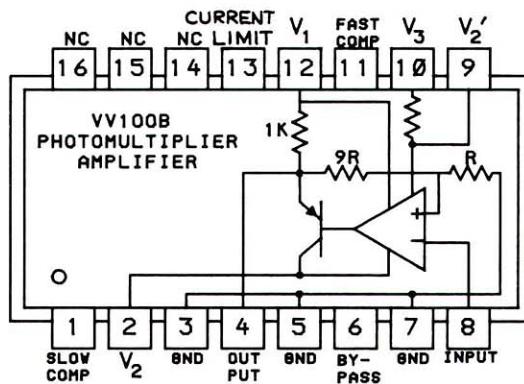
Shifts in the DC output level remain negligibly small even when the amplifier is subjected to extremes of operating temperature or variations in power supplied. There is virtually no warmup drift at turn-on.

An ideal "transparent gain" element would simply magnify the input signal without significant distortion of operating constraints. The VV100B performance is very close to this ideal by virtue of its extraordinary stability, speed, linearity, and noise characteristics.

PACKAGING



LOGIC DIAGRAM (TOP VIEW)



SPECIFICATIONS

Hybrid Circuit Model WV100B

WIDEBAND PULSE AMPLIFIER

Gain:	10 FIXED, $\pm 5\%$ tolerance, non-inverting, long term stability $\pm 1\%$
Linearity:	$\pm 0.2\%$ integral (0 to -3 V)
Maximum Output Swing:	-5 V at 200 mA ^{Note 1} $+250$ mV at 5 mA ^{Note 3}
Output Impedance:	$<0.2 \Omega$ for negative outputs
Frequency Response:	≥ 170 MHz for 2 voltage operation ^{Notes 4, 7} ≥ 200 MHz for 3 voltage operation
Full Signal Bandwidth (3 dB)	
Risetime (10% to 90%):	≤ 2 nsec
Input Signal Range:	
Maximum Safe Input Signal	± 1 V; external clamp diodes recommended ^{Note 6}
Linear Range	-0.5 V to $+0.01$ V
Wideband Output Noise: (referred to input)	<50 μ V rms
Input Impedance:	>1 k Ω
Input Bias Current:	-25 μ A
Drift vs. Temperature	250 nA/ $^{\circ}$ C
Input Offset Voltage:	
Typical	2 mV, adjustable to 0
Drift vs. Temperature	10 μ V/ $^{\circ}$ C (max)
Drift vs. Supply Voltage	<100 μ V, for $\pm 1\%$ variation
Drift vs. Time	<100 μ V, long term
Coupling:	
Input	Direct
Output	Direct
Temperature Range:	0° C to 70° C
Power Supply Rejection Ratio:	90 dB at 120 Hz
Power Supply:	(Two Voltage Operation) ^{Note 4}
Rated Voltage, Quiescent	$V_1 = 30$ mA at $+6$ V
Current	$V_2 = -20$ mA at -6 V to -12 V (Tie pin 9 to pin 2)
Power Supply:	(Three Voltage operation) ^{Note 5}
Rated Voltage, Quiescent	$V_1 = 30$ mA at $+6$ V
Current	$V_2 = -28$ mA at -6 V to -12 V
	$V_3 = -8$ mA at $V_2 = -12$ V (e.g., -24 V when $V_2 = -12$ V and pin 9 open)
Overload Recovery:	Operation with $V_2 = -12$ V supply: saturated for approximately 15 nsec after $10 \times$ overload.
Package:	Standard 16-pin dual in-line hybrid integrated circuit.

NOTES:

1. Overload protected to limit the average output current to <60 mA. See application notes.
2. No overload protection. Average output current should be <50 mA to avoid damage to the unit.
3. For increased positive swing, see applicaiton notes.
4. Three voltage operation recommended for most applications.
5. Three voltage operation provides increased bandwidth.
6. See Figure 1.
7. For two voltage operation install a 6.8μ F capacitor from pin 13 to ground with the positive lead grounded.

SPECIFICATIONS SUBJECT TO CHANGE

APPLICATION NOTES

The LeCroy model VV100B is a hybrid circuit designed as a high bandwidth amplifier primarily intended for amplification of negative pulses such as those from photomultiplier tubes. It has a fixed gain of 10 and a risetime of less than 2/1 nsec. The output is capable of driving two 50 Ω loads (25 Ω). The linear range of the VV100B is + 200 mV to - 5 V. The user may supply suitable input impedance for his particular needs. The unit requires an input terminating resistor, power supply bypass capacitors, input and output DC trims and an output shape capacitive trim.

Figure 1 shows a typical application circuit for the VV100B and is the circuit on the LeCroy VV100BTB amplifier. Here input trim T1 is accomplished by the series combination of a 27 kΩ resistor and a 500 kΩ potentiometer. Trim T2 is set by the 1 MΩ potentiometer and series 100 kΩ fixed resistor. A fixed resistor to ground sets the low frequency gain trim (T3). High frequency compensation is set by the 51 Ω, 6-35 pF combination.

The VV100B contains output protection circuitry which limits the average output current to 60 mA. The time constant of the limiting circuit is approximately 6 μsec.

The internal current limiting of the VV100B may be defeated by placing a jumper between pins 13 and 2. This connection allows bipolar operation if an additional resistor is connected from the output to a positive supply voltage. All positive current delivered to the load is through this additional resistor. The DC value of this added current should be held to less than 40 mA.

If internal current limiting is not defeated, the maximum positive voltage excursion into a load R_L is

$$V_{Max}^+ = \frac{6 R_L}{R_P + R_L}$$

The most negative will be given by

$$V_{Min}^- = (0.06 V) \frac{R_P R_L}{R_P + R_L}; \quad V_{Min}^- \geq -5 V$$

LAYOUT

Because of the extremely high bandwidth of the VV100B, care should be used in layout of the printed circuit board. Continuous ground plane construction is essential. To ensure minimum inductance, low profile sockets like the TI or AUGAT should be used. Insertion pins (Berg 75315-001 or equivalent) are even better. Input busses should be separated from the output. Interconnections to other circuitry greater than 3 cm away should be made only by properly terminated coaxial cable. Input protection circuitry and bypass capacitors as described below should be located as close to the hybrid as possible.

THE INPUT

Proper termination and protection must be supplied to the input. In most cases, input to the amplifier will be via 50 Ω cable. In this case, a 50 Ω resistor from the input (pin 8) to ground should be employed. In addition, three 1N4448 or equivalent diodes to ground as shown in Figure 1 will provide overload protection. The input DC level must be trimmed to zero by a trim resistor (T1) to a negative supply. Where the best DC stability is required, this supply should be regulated. Note that fluctuations in the input offset will appear at the output amplified 10 fold.

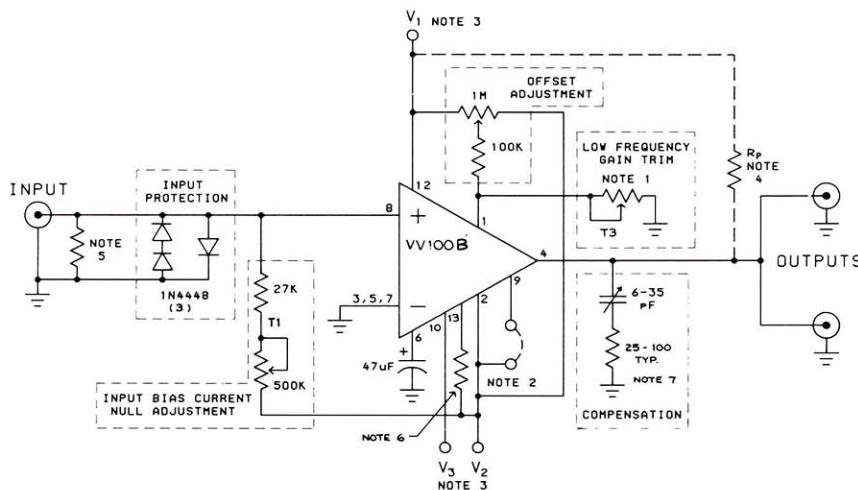


Figure 1

NOTES:

1. Typical value = 7.5 kΩ
2. Add jumper for 2-supply operation
3. All power supply voltage lines should include a high frequency bypass, typically a 6.8 μF capacitor to ground and a 50 μH series choke.
4. Optional pull-up for extended positive voltages exclusions.
5. Input termination resistor, chosen to match input cable impedance.
6. 10 Ω current limiting resistor should be added when driving 25 Ω load.

POWER

A current of about 30 mA from +6 V must be supplied at pin 12. In addition, two negative supplies, V_2 and V_3 , are recommended. V_2 (pin 2) requirement is 20 mA at a voltage between -6 and -12. V_3 (pin 10) is to be set 12 V more negative than V_2 . For example, with V_2 set to -12 V, V_3 should be -24 V. The VV100B requires about 8 mA from the V_3 supply. Proper bypass requires at least 6.8 μ F tantalum capacitors to ground from pins 2, 12, (and 10 if three voltages are used) and 47 μ F on pin 6. Minimum length leads should be employed. Be sure to observe proper polarity. See Figure 1. Model VV100B can be operated with only two proper power supplies at the expense of risetime and linearity. For this configuration, tie pin 2 to pin 9, set $V_2 = -6$ V to -12 V, V_3 is omitted and $V_1 = +6$ V.

THE OUTPUT

The VV100B is optimized for a 25 Ω load in order to drive two 50 Ω cables simultaneously. If only one cable is to be driven, a 50 Ω resistor should be connected from the output of the VV100B to ground, to provide a net 25 Ω load. Other numbers of cables, and cables of impedances other than 50 Ω may be driven, always taking care to maintain the required 25 Ω through the use of additional series or shunt resistance. For example, three 91 Ω cables require an additional 142 Ω shunt to ground; five 50 Ω cables may be driven via five 75 Ω series resistors (yielding reduced gain and output swing as the price of the additional fan-out). Driving loads other than 25 Ω will cause output shape and stability problems. Loads less than 25 Ω degrade risetime, gain, and linear range; loads larger than 25 Ω produce ringing and oscillation.

OUTPUT PROTECTION

The output of the VV100B is protected against sustained shorts to ground in the presence of DC inputs. This short circuit protection is implemented by an integrating stage which senses output current and limits it to an average current of 60 mA. The time constant of the limiting stage is approximately 6 μ sec. The maximum pulse output current is a function of the input pulse width, amplitude and repetition rate.

When limiting occurs, this integrating stage must recover before linear operation may resume. Longer averaging times can be achieved by adding capacitance from pin 13 to ground. Current limiting may be defeated by a jumper from pin 2 to pin 13. Under this condition, safe operation requires $(V_{out} - V_2) i_{out} < 1$ W.

The limiting circuitry is based upon the average output current of the VV100B. The maximum output swing for pulses less than the averaging time will be

$$d_{max} = \frac{(60 \text{ mA})}{D}$$

Here, D is the duty factor. For larger widths the VV100B output will begin to shut down after a time t_{limit} and approach 60 mA with a 6 μ sec time constant.

TRIMS

The VV100B requires three separate trims: input DC level, output DC level, and fast compensation.* The values of these trims must be selected for each VV100B and hence must be reset if the VV100B is replaced. All trims should be made with the VV100B output loaded with 25 Ω .

The first trim, T1, is used to set the input DC offset. With no input to the VV100B, install a resistor between the input connector and a regulated negative supply. The value of the resistor should be chosen to set the input voltage to 0.0 mV. Typical values of this trim are 30 k Ω to 300 k Ω .

The second trim, T2, is used to set the output DC level to zero. This trim is a resistor from pin 1 to either the negative or positive supply, depending upon the polarity of the initial DC offset. Typical values of this trim are 100 k Ω to 1 M Ω . The last trim is an RC adjustment of the overshoot of the output. A 6-35 pF trimmer capacitor in series with a 25-100 Ω resistor is required to minimize the overshoot. Using a fast risetime input pulse, observe the output of the VV100B. Adjust the trim capacitor to give the best output pulse shape.

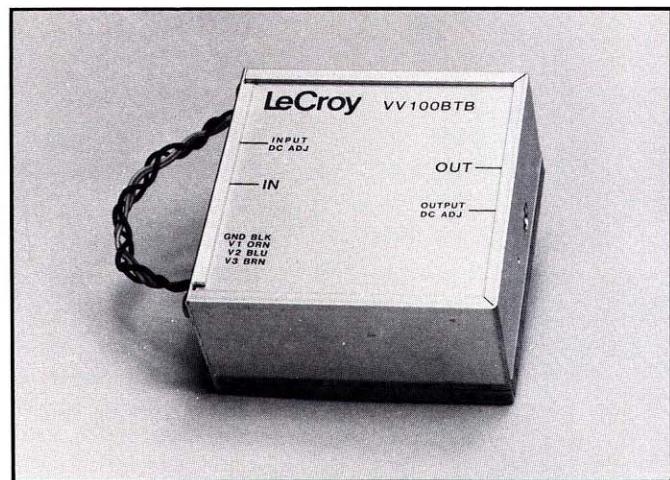
* Occasionally an additional slow compensation trim (T3) is required. To make this trim, a flat-topped pulse of about 10 μ sec duration is applied to the VV100B input. A resistor in the range of 10 k Ω to 300 k Ω connected from pin 1 to pin 4 (or ground as required) is used to trim the output pulse to a flat top.

ORDERING INFORMATION

The LeCroy Model VV100BTB provides the high bandwidth circuitry, shown in Figure 1, in a ready-to-use format. The 3 inch \times 3 inch \times 1.6 inch enclosure size of the device allows one to use the Model VV100B in locations too small for many fast amplifiers. The amplifiers employ Lemo type coaxial cable connectors. The units may be purchased with a Model VV100B. The trim and compensation variables are factory adjusted for optimum high-speed performance.

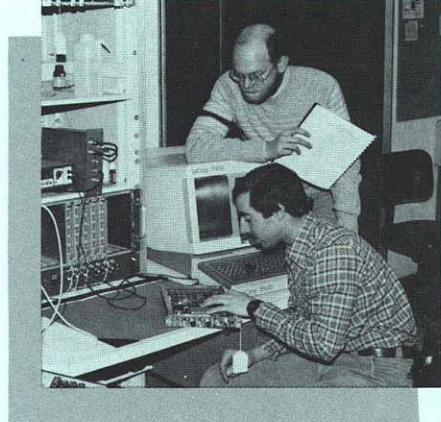
MODEL DESCRIPTION

- | | |
|----------|---|
| VV100B | Amplifier hybrid. |
| VV100BTB | VV100B mounted in circuit board. Lemo connectors. |

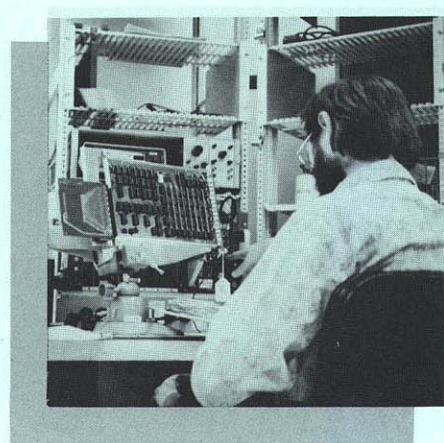
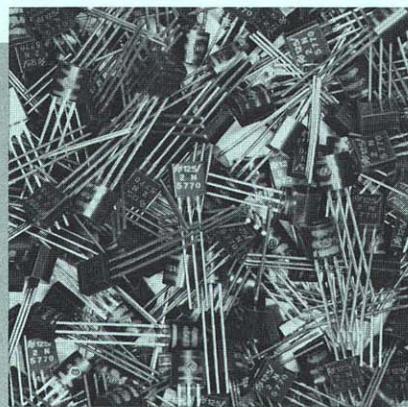
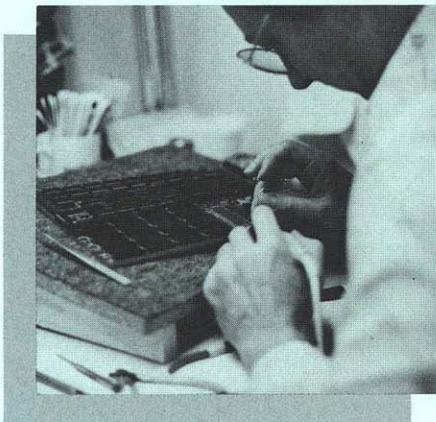


Model VV100BTB wideband amplifier module.

Waveform Measurement Concepts



Transient Recorders
Analog-to-Digital Conversion
Signal Sampling
Video Digitizing
Memory Buffering
Transient Recorder Performance
Accessory Modules
Configurations and Packaging



Waveform Recording

Conversion of an analog signal into digital values allows the full range of digital techniques to be applied to the data. Once stored in the digitizer memory, the digital data can be transferred via various digital input/output interfaces to computers, displayed back in graphical form (on raster or analog oscilloscopes), scanned for phenomena of interest, printed, plotted, processed or archived for future use.

Being able to convert non-repetitive (transient) signals to digital form provides an invaluable tool for studying single-shot events, as the entire trace is captured and held as long as required. If a repetitive signal is available, then signal enhancement is possible by: 1) recording multiple events and averaging to eliminate noise and/or 2) interleaving to increase effective sampling rate.

Key to obtaining a good digital representation of the original signal is the analog-to-digital converter and the sampling circuits that precede it. Accuracy, linearity, sampling speed, etc., all contribute to the performance required to acquire and store accurate digital records.

Analog-to-Digital Conversion

Several techniques are in current use for transforming the signal into a digital number: Wilkinson run-down method, successive approximation, flash conversion, or the use of some combination of these.

The Wilkinson run-down method stores the sampled voltage in a capacitor. Using a constant current source, the capacitor is discharged linearly. The time it takes to run down (discharge from its original value to zero) is accurately measured by a crystal clock. The combination of a fast clock and a slow discharge can result in a very precise digitization. With present state-of-the-art electronics, conversion by this method can provide high resolution with excellent differential and good integral linearity. However, minimum practical conversion times of several μ sec per sample makes this technique of marginal use for most high-speed transient recorder applications.

The successive approximation technique uses a series of comparisons (one per bit), matching a reference level to the input voltage (see Figure 1). Conversion begins by setting

the MSB, which via a digital-to-analog converter, generates a half-full-scale reference level (the analog value of the MSB). A comparison is then made to determine if it is greater than or less than the input signal. If the input voltage is less, the MSB is cleared (set to "0"); if more, the MSB is left (set to "1") and the value of the half-full-scale reference level is subtracted from the input. The next approximation is made by setting the MSB-1, comparing the quarter-scale analog representation against the input voltage remaining from the previous comparison, etc. This continues until each bit of the final desired "word" has been cycled through. This method is typically faster than the Wilkinson method above (e.g., a 10-bit conversion can be easily completed in less than 1 μ sec) but achievable differential linearity values of 10-30% are not as good. This technique is useful for high resolution (10- to 12-bit) conversions at medium speeds (in the range of 1 megasample/sec and down).

The flash converting method uses a parallel array of comparators, one for each level of required resolution (e.g., a 6-bit converter would require 64 comparators). Each comparator matches the input signal to its appropriately adjusted reference level. After allowing sufficient settling time, the outputs of the comparators are latched and encoded. Using proper design techniques, this method of conversion can be extremely fast (e.g., settling and latch times of 10 nsec are achievable, resulting in 100 megasample/sec conversion rates). This method is one of the best for high speed digitizers (10 to 200 megasample/sec rates). The major drawbacks are the difficulty in controlling the differential linearity (may approach 50% in practical circuits, especially at high bandwidth and sample rates) and the fact that the large number of comparators

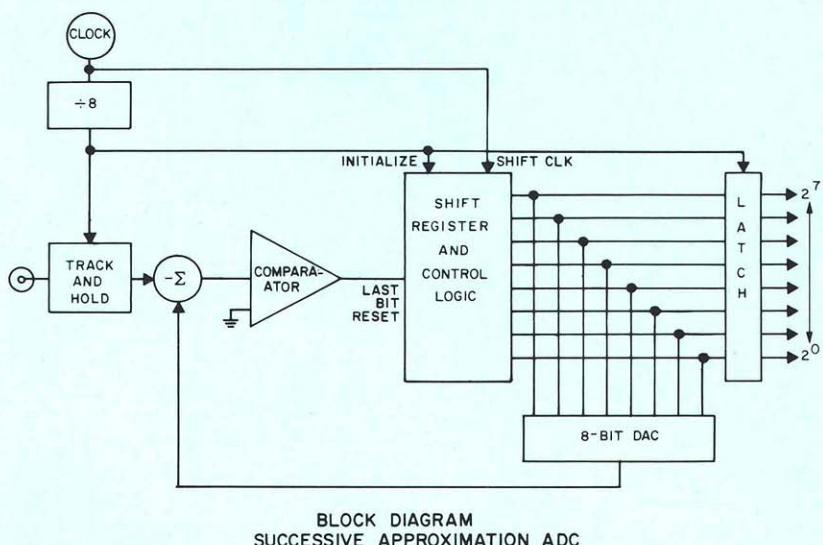


Figure 1

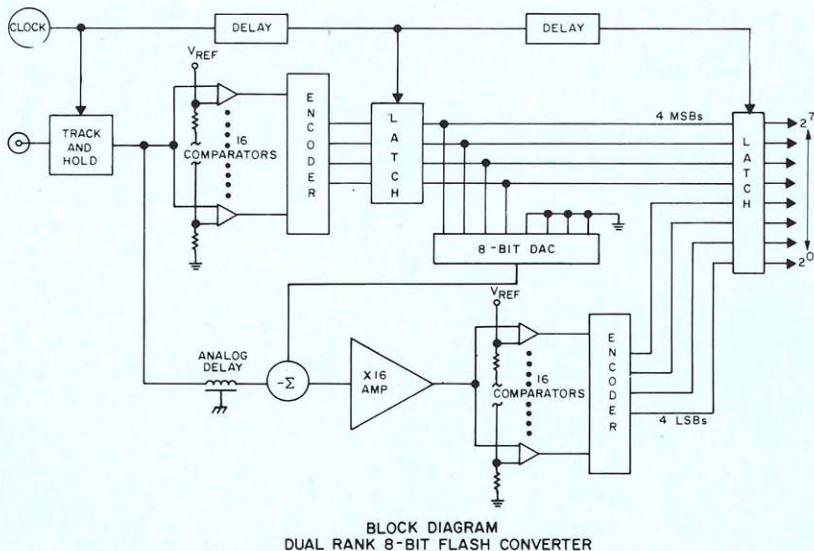


Figure 2

required limits flash conversion's practical use to low-resolution applications (6- to 8-bits) unless special techniques (e.g., multiple ranking) are used.

Often the best results can be obtained by using combinations or multiple stages of the above. The possible combinations are many, but one of the most popular is the use of two flash converters in a "dual-rank" configuration (see Figure 2). For example, by using a 4-bit flash converter in the first rank, the signal can be divided into 16 levels. Following the 4-bit flash with an accurate digital-to-analog converter and subtracting its output from the input signal will produce a remainder that can be converted by a second flash converter. If the second flash is also 4 bits, and the gains and offsets are properly set, the 4 bits of the second rank can be stacked under the first rank, resulting in 8 bits (256 levels) with only 32 comparators (16 per rank). To further improve speed, pipelining (using analog delays, temporary digital storage, etc.) can be employed. This allows the first rank to begin a second conversion while the second rank is still finishing the first. These techniques can considerably reduce the number of compo-

nents, reducing instrument cost, power and size.

Signal Sampling

With any analog-to-digital conversion technique it is important that the input signal be held constant during the entire conversion. If it is not, uncertainty in the sampling time will translate into inaccuracy in signal conversion (see Figure 3). This requires a track-and-hold circuit that is capable of storing the value of the analog voltage at the instant the conversion is ready to begin and holding it through the conversion time. Basically, the amplifier stage in the track mode is critical in determining input bandwidth, phase distortion and integral linearity. Switching to the hold mode

must be virtually instantaneous [to prevent bandwidth limiting caused by $(\sin x)/x$ effects] and jitter free [to prevent amplitude errors caused by aperture uncertainty]. Even flash converters require an analog hold circuit for optimum performance, as each of the comparators may have different settling times or propagation delays.

An extension of the single sampling circuit for increasing sampling-rate speed involves multiplexing the input data into multiple analog hold circuits. These circuits can be in the form of discrete capacitor hold stages, charge coupled devices (CCD's), etc. Ultimately, this method allows high speed analog storage of as many samples as there are analog storage locations. Once stored, a slow, economical ADC can sequentially scan through the storage locations, converting and storing the digital values in memory. It is possible, for example, to sample and store analog samples at a 1 GHz rate, then sequentially convert each stored sample at 1 megasample/sec, giving a 1000-to-1 sample rate increase. The problems encountered in this technique, other than the requirement for extremely high-speed analog sampling, are that the record length will be limited to the number of analog store locations available, and off-line data correction probably will be required due to the multiplicity of analog paths.

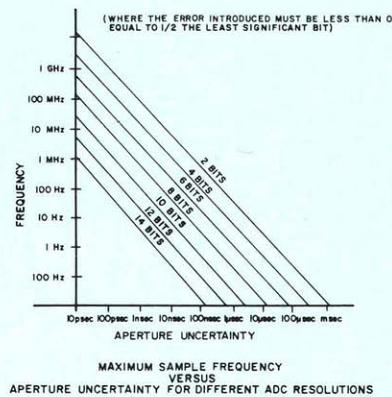


Figure 3

Video Digitizing

A special type of transient recorder, called a video digitizer, can be used for digitizing video signals from standard North American or European frequencies or nonstandard high-frequency video cameras. This device digitizes the analog signal variations for each scan line of the video camera. Standard U.S. video cameras produce 525 scan lines at a sweep frequency of 30 Hz, pro-

ducing one complete interlaced video frame in 33.3 msec. The horizontal resolution desired determines the sampling frequency of the video digitizer. To produce horizontal resolution of 256 samples per video scan line requires a digitizer sampling rate of about 4 MHz and requires a memory length of approximately 128,000 words to produce one complete video field of 262.5 lines. Multiple video fields can be digitized and stored either by increasing the memory length in increments of 128K words (LeCroy's video digitizers support up to 2 megawords of memory) or by decreasing the sampling frequency (this is less desirable because horizontal resolution will degrade).

For nonstandard video frequencies employing high-speed cameras, it is necessary to digitize at higher sampling rates to maintain nominal 256-word horizontal resolution. Currently, high-speed cameras are available with sweep rates up to 10 times greater than standard video frequencies, and therefore require sampling frequencies that are 10 times greater. While such sampling frequencies are not available on most video digitizers, LeCroy's video digitizers sample at rates up to 50 MHz to accommodate the fastest known video cameras.

Once digital video data is stored in the semiconductor memory, it can be accessed by a computer for viewing or processing via a bi-directional communication bus (CAMAC). Computer processing such as enhancement, subtraction and intensification can be performed and the video frame(s) can be rewritten into the memory.

A companion display controller permits direct display of memory contents — either raw or processed — onto a standard video monitor. The display controller frequency is matched to U.S. or European monitor sweep frequencies and its output is synchronized

on the vertical sync pulse stored in the digitizer memory. Thus, immediate display of one or more digitized video fields is conveniently and inexpensively available for monitoring experiments and video phenomena.

Memory Buffering

Digitization of transient signals frequently generates data at a faster rate than the real-time capability of most modern computers. The problem increases if there are multiple signal channels. Even when an array processor or ultrafast computer allows an adequate data transfer rate, local data storage in a buffer memory usually is more cost effective.

An effective means of providing memory is via expandable, modular slaves to the digitizers. It is possible, for example, to cascade 32K word modules to provide sample memory lengths from 32K to 512K words.

Multichannel digitizers share a common memory string but dynamically allocate all memory to the number of digitizer channels activated. In addition, they allow selection of an individual channel for readout even when multiple channels are written sequentially into memory. Since the length or time scale of the waveform record stored in memory is dependent on the total memory length and the sampling frequency, the modular memory allows easy adjustment of record lengths to match the user's requirements.

An especially useful memory feature of transient recorders is pre- and post-trigger sampling. When triggering from a transient (randomly occurring) signal, it is often useful and sometimes necessary to record the waveform prior to the transient event. This is achieved by continuously digitizing and storing data in memory, continuously over-writing the oldest data un-

til a trigger command stops the digitizer (either immediately or after storing a predetermined number of additional samples after the trigger). The result is that data prior to the trigger is available (a feature not possible on an analog oscilloscope).

Transient Recorder Performance

The function of a digitizer is to record the magnitude of a waveform at specific times. How well a system performs this operation is disclosed by several specifications including bandwidth, aperture uncertainty, linearity, monotonicity and noise. While it is often assured that the performance of a digitizer is indicated by the number of "bits" (e.g., 8 bits provides a resolution of one point in 256 or 0.4%), the interaction of other mechanisms described by the above specifications can substantially reduce the real accuracy from this value, and it generally does so with increasing signal frequency and sampling rate.

The best measure of a digitizer's overall performance is given by the dynamic accuracy specification, an expression that includes all errors, whatever their origin. It may be expressed either as signal-to-noise ratio or effective bits. Essential to both measures is the concept of rms error. If one analyzes the output of a digitizer, there is an error for each sample point. The rms value (defined as the square root of the sum of the errors squared) describes the average deviation over the entire array of sample points. The signal-to-noise ratio, R, is then given by the ratio of rms signal to rms error and its equivalent in decibels is given by $20 \log R$. Alternately, the rms error can be expressed as the equivalent number of lost bits via $\text{Lost Bits} = \log_2 (\text{rms error}/\text{ideal rms error})$, where the ideal rms error is the quantizing error of a perfect ADC, and is equal to the LSB size divided by 12. The

Signal/Noise dB	Signal/Noise Ratio	% Error (1/R x 100)	Lost Bits	Effective Bits
20	10	10.0	5.0	3.0
32	40	2.5	3.0	5.0
42	126	0.8	1.3	6.7

lost bits are related to digitizer resolution by the definition: Effective Bits = Total Bits - Lost Bits. (e.g., if an 8-bit digitizer has three lost bits, its effective bits are $8 - 3 = 5$). Representative values for dynamic accuracy in different units for an 8-bit digitizer are compared above.

Since a digitizer is required to operate over a wide bandwidth, the most informative measure of performance is dynamic accuracy plotted as a function of signal frequency (see Figure 4). In better instruments the curve is relatively flat with increasing frequency

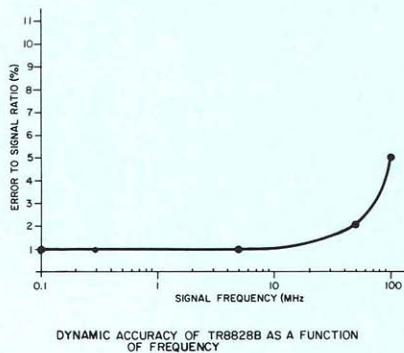


Figure 4

and preserves precision and dynamic range up to the Nyquist limit, equal to 50% of the maximum sampling frequency.

Another important measure of performance is given by the histogram of ADC codes for a signal of known characteristics. These data are indicative of differential nonlinearity and disclose the existence of any missing codes. Figure 5 compares the histogram of codes from an 8-bit ADC sampling a sine wave with the histogram generated by an ideal ADC. Any gaps in the plot indicate

missing codes, while substantial deviations show non-uniformity in individual code size over the dynamic range.

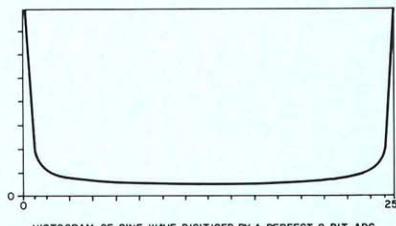


Figure 5A

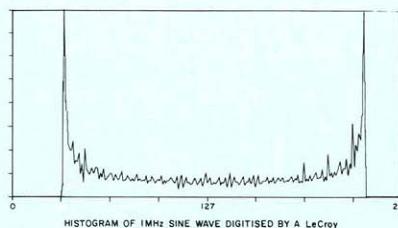


Figure 5B

Accessory Modules

Signal Conditioning: All transient recorders have a single input range (generally 512 mV p-p for $50\ \Omega$ inputs or +5 V for high impedance inputs). Where required, separate signal conditioning modules may be used to attenuate, amplify or match impedances to the signal source. The appropriate instrument is selected according to the function required and bandwidth capability of a particular digitizer.

Triggering: Each digitizer has its own stop trigger input. Typically, this input requires either TTL or ECL level logic signals. If these signal levels are not available or if it is necessary to trigger on the signal itself, a trigger generator is required. Operating much like an oscilloscope trigger con-

trol, a trigger generator (which may share a module housing with a signal conditioning circuit) gives the operator full control of trigger level, polarity, slope and input coupling.

Sampling Clocks: Transient recorders usually include built-in clocks which determine the sampling period. They are programmable from the CAMAC dataway and sometimes from the front panel. In multi-recorder applications it is possible to use one digitizer's clocks as a master and distribute it to the other units in the system, thereby assuring a uniform phase relationship between samples. A separate clock module is used when more complex clocking functions are desired. Examples include generating clock signals in a series of bursts, sampling at two different rates within one record or sampling synchronously with external events (e.g., sampling the output of charge-coupled devices). Unlike transient recorders, video digitizers do not contain internal clocks and a separate clock module is used to "sync" acquisition and display to the video frame data.

Configurations and Packaging

A Modular Transient Recorder consists of independent modules which are assembled building-block fashion in a powered housing to form a waveform digitizer system of desired characteristics. Modules conform to the international CAMAC (IEEE Standard 583 and ESONE Standard EUR4100). Transient recorders configured as plug-in modules offer these advantages:

1 — Multichannel Operation. Compact system components permit many channels to share common mainframe, interface and display facilities. This not only lowers cost, but is ideal for operation in test systems, remote environments or wherever space is limited.

2 — Flexibility allows selecting performance to match the application and the budget. Also, the ability to modify the system at any time permits expansion and inclusion of newer system components. Modularity allows the mixing of different frequencies and resolutions. LeCroy's modular digitizers offer maximum sampling speeds from 100 kHz to 200 MHz, resolution from 8 to 12 bits, and the opportunity to record transient signals in detail down to 5 nsec per sample.

3 — Expandable Waveform Memories. Basic memories may be expanded by addition of inexpensive memory modules to 512K or larger. Long waveforms can thus be digitized without reducing sampling resolution.

4 — Multifunction Capability. The modular transient recorder system can do much more than just record waveforms. Since the plug-ins adhere to the Computer Automated Measurement Control Standard IEEE 583 (CAMAC), more than 2000 commercially available DVM's, data loggers, time interval digitizers, stepping motor controllers, relay drivers, etc., are compatible with this system.

Standard CAMAC instrument housings and power supplies are available to hardware interface and power up to 23 module widths in a rack-mountable housing or 13 module widths in a portable bench top housing.

Basic manual control or waveform display of data for local display is provided on most transient recorders by using either their built-in capability or using an external hardware control and display accessory module. In display mode, digital memory contents are converted to analog for direct display on an oscilloscope.

Using one of the many standard CAMAC interfaces avail-

able (e.g., LeCroy Model 8901 GPIB Controller) in the instrument housing, stored waveform data can be transferred to an associated computer for display, processing, hard copy or archiving on the computer's disc or tape.

The availability of turnkey software for the popular IBM PC and "PC compatibles" entirely eliminates software development necessary to read transient recorder data and process and display it on a computer's graphic terminal. User interaction with the computer is by single keystrokes for operations such as acquisition, display, processing and outputting data. For special acquisition, display or processing requirements, the software can be readily user-modified within the structure of the standard software.

High speed signal processing generally requires a more sophisticated, multiprocessor acquisition system. Systems like LeCroy Models 3500 and 3500SA combine a built-in module housing with keyboard, graphics display and several processors. These user programmable systems offer software packages to control the transient recorders, display or archive data, perform high-speed signal averaging, generate FFT's, etc.

Quick Reference Chart/Page Guide for Transient Recorders

Model	8210	8212A 8212A/8	2264	TR8837F	TR8857A	TR8818	TR8828B
Maximum Sampling Rate	1 MHz (4 ch)	100 kHz (8212A) 40 kHz (8212A/8)	4 MHz (1 ch) 2 MHz (2 ch) 1 MHz (4 ch) 500 kHz (8 ch)	32 MHz	50 MHz	100 MHz	200 MHz
Resolution	10 bits	12 bits	8 bits	8 bits	8 bits	8 bits	8 bits
Full Scale Range	± 5V	± 5V	512 mV	512 mV p-p	512 mV p-p	512 mV p-p	512 mV p-p
Channels per Module	4	32 (8212A) 8 (8212A/8)	8	1	1	1	1
Input Impedance	1 MΩ	1 MΩ	50 Ω	50 Ω	50 Ω	50 Ω	50 Ω
Compatible Memory Modules	8800A (32K)	8800A (32K)	8800A (32K)	none	MM8306A/9 (64K)	MM8103A (32K)	MM8104A (32K) or 2 MM8103A (64K)
Maximum Memory per Channel	96K*	512K	128K*	8K	1M	512K	512K
CAMAC Width	3	3	3	1	2	2	3
Maximum No. of Channels per 23-slot CAMAC Crate	20	160 (8212A) 40 (8212A/8)	5 @ 4 MHz 20 @ 1 MHz 40 @ 500 kHz	20	5	5	4
Page	365	367	347	397	401	389	393

*up to 512K by factory-installed option

See also Models LG8213 and LG8252 Multichannel Dataloggers (Pg. 383)

Product Guide for Waveform Measurement Applications

MODULAR TRANSIENT RECORDERS

Recorders/Memories: 2264, 8210, 8212A,
8212A/8, 8800A, TR8818, TR8828B,
TR8837F

Data Loggers: LG8213, LG8252

Video Digitizers: 8658A, TR8857A

SIGNAL PROCESSING AND CONDITIONING MODULES

Amplifiers/Attenuators: 8100, 8102

Clock and Function Generators: 8501, 8601

Trigger Generators: TG8610B

MEMORY MODULES

Transient Recorder: 8800A
Dual Ported: MM8201A, MM8206A

FAST SIGNAL AVERAGERS/ PROGRAMMABLE WAVEFORM ANALYZERS 3500SA Series

MAINFRAMES, CONTROL AND INTERFACING

Benchtop Housings: 3500SA Series, 8103

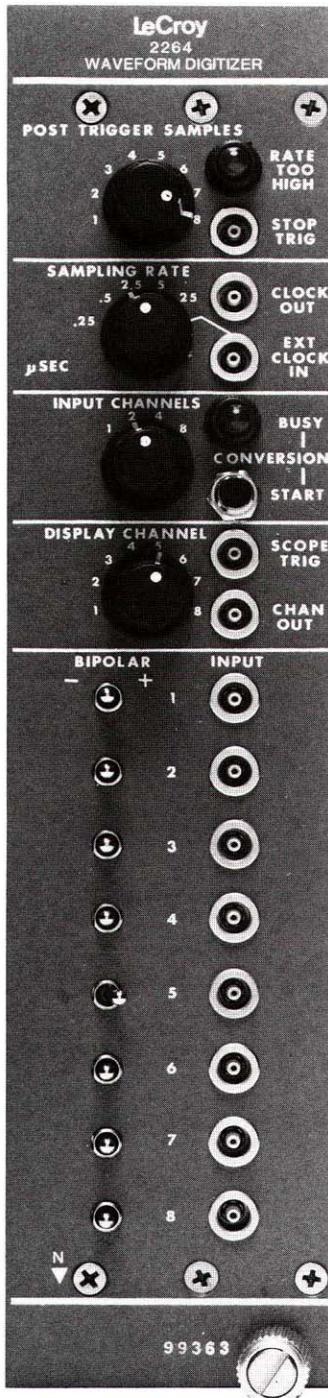
Rackmount Housings: See 1434, page 73

Manual Control/Display: CD8828B, 8658A

GPIB Interfacing: 8901

TECHNICAL DATA

LeCroy



Model 2264 Multichannel Waveform Digitizer

- 1, 2, 4, or 8 input channels
- 8 bits of dynamic range and resolution
- 500 kHz maximum sampling rate (4 MHz in single channel mode)
- 150 psec sample time uncertainty; 1 MHz analog bandwidth
- Inputs fully protected with good overload recovery
- Companion memory expandable in 32K word steps
- High sensitivity of 2 mV/count, maximum
- 3-level input offset for each channel
- Excellent interchannel cross talk isolation
- Analog readout of memory viewable on any scope
- Non-destructive readout by standard CAMAC commands
- Post-trigger sampling

The LeCroy Model 2264 is an 8 Channel 8-bit transient recorder. Either 1, 2, 4, or 8 channels may be active and will be sampled 200 nsecs apart at a rate determined by the number of active channels: 4 MHz for 1 channel, 2 MHz for 2 channels, 1 MHz for 3-4 channels and 0.5 MHz for 5-8 channels. Sample aperture uncertainty is less than 150 psecs and, together with the 1 MHz analog bandwidth, assures excellent dynamic accuracy. When more than one channel is selected, the used inputs are sampled sequentially. Digitized information from the transient recorders is automatically transferred to associated memory modules, which may be cascaded to achieve the desired record length for each digitizer. The minimum record is 32K samples divided equally between the number of active inputs. Up to 96K words may be addressed by the standard unit.

The number of inputs enabled is determined by a front-panel switch and, as with all manually settable controls, may be read via CAMAC. The input range is independently selectable for bipolar or monopolar signals of either polarity. Once initiated by the front-panel start pushbutton of CAMAC F(9) command, all enabled channels are sampled 200 nsecs apart at the rate of the conversion clock. The front-panel control provides internal clock rates from 40 kHz to 4 MHz. However, any clock rate up to 4 MHz may be applied to the external clock input. A clock output is provided to permit synchronizing several units using one unit as a master. Sampling of all channels continues indefinitely until receipt of a stop trigger via the front panel or a CAMAC command. A front-panel control determines the fraction of memory devoted to pretrigger and post-trigger samples in 1/8s of total memory and is usually set to view a signal's edge or level proceeding an event of interest. For example, a post-trigger setting of 4 means that memory is equally divided between samples taken before and after the trigger. Once stopped, the 2264 automatically enters a manual readout mode where the contents of one selected channel is presented in analog form at a front-panel display output for viewing on any real-time oscilloscope. Note that the front-panel conversion start pushbutton, in conjunction with the display output, permits manual operation without need for CAMAC intervention.

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SPECIFICATIONS

CAMAC Model 2264

MULTICHANNEL WAVEFORM DIGITIZER

INPUT CHARACTERISTICS

Number of Inputs:	1, 2, 4, or 8; switch selectable.
Impedance	50 Ω (up to 100 kΩ at a reduced bandwidth—Model 2264, Mod 100).
Full Scale Amplitude Range:	512 mV. Each input can separately accept negative, positive, or bipolar signals. In the bipolar mode, maximum signal amplitude is 256 mV (10.24 V range available—Model 2264, Mod 100).
Overvoltage Protection:	Input protected against ± 5 A transient for 0.5 μ clamping at ± 1 V.
Input Analog 3 dB Bandwidth:	1 MHz for all configurations (>100 kHz for 100 kΩ input impedance—Model 2264, Mod 100.)
System Aperature Uncertainty:	<150 psec; defined as the uncertainty in the actual sample-taking time relative to the leading edge of the clock. This corresponds to an upper limit of 2 MHz on the frequency of the sinusoidal wave which can be reconstructed with 8-bit accuracy from the ADC.
Integral Linearity:	Better than 0.5% of full scale.

WAVEFORM SAMPLING ORGANIZATION

Sampling Rate:	DC to a maximum of 4 MHz for 1 input, 2 MHz for 2 inputs, 1 MHz for 3, 4 inputs, and 0.5 MHz for 5, 6, 7, 8 inputs. Front-panel LED blinks for improper combinations of sampling and number of channels.
Internal Clock:	Front-panel selectable from 40 kHz to 4 MHz. Stability ± 0.01%. The internal clock is available for synchronization purposes.
External Clock Input:	One Lemo connector, 50 Ω input, TTL-level pulses; valid frequency range 0 to the maximum frequency given by the number of active channels. The external clock can be varied in frequency to achieve important sampling.
Burst Mode Multiplexing:	Each clock pulse triggers an internal 5 MHz sampling sequence of all active inputs.
Digitizing:	The tracking and digitizing accuracy is 8 bits (1 part in 256 or 0.4%).
Pretrigger Sampling:	A programmable number of samples taken before the Stop Trigger will be saved in memory, with the remainder of the memory containing samples taken after the Stop Trigger.
Memory Organization:	The memory is contained in separate modules, each capable of storing up to 32,768 samples. (See description of LeCroy Model 8800A) The size of the memory, which depends upon the number of expandable memory modules used, is programmed into the Model 2264 by a jumper option.

READOUT METHODS

Display:	A built-in display driver allows the memory contents of a switch-selected input channel to be viewed on any real-time oscilloscope. Each sweep consists of a separate negative sync signal for trigger purposes and a waveform proportional to the amplitude of the input signal.
Computer Readout:	Once a conversion cycle has been completed, the data can be read two words at a time. For two or less active channels, readout speed can be CAMAC maximum. For more than two channels, readout speed is less. See manual for details. Separate CAMAC commands read the status of the front-panel switches. Word count and Q-stop DMA's are possible.

CAMAC COMMANDS

L:	LAM indicates data is ready to read. Requires F(26) to enable LAM, disable display. (May require up to 20 msec per 32K memory module to cycle to end of memory.) LAM also raised upon completion of data readout.
Q:	A Q = 1 (Data Valid) response is generated only when a valid word is being read, or in response to F(8) if LAM is set. (When using F(2) Q = 0 after all data has been read for a selected channel or pair of channels.)
Z or C:	Initiates continuous sampling cycle; disables LAM. (Equivalent to F(9) command.)
X:	An X = 1 (Command Accepted) response is generated when a valid F and N are received.

CAMAC FUNCTION CODES

F(0):	All commands require N and A(0) except F(16) as shown. Reads front-panel offset switches, 2 bits for each of the eight switches. R1 and R2 are assigned to Channel 1, up to R15 and R16 for Channel 8. Binary value 01 to 11 of the two bits correspond to negative unipolar, positive unipolar and bipolar, respectively.
F(1):	Reads remaining front-panel switches as follows: Post-trigger Samples: Binary values of 111 to 000 of R3-R1 correspond to 1024 to 8192 samples after the trigger. Sampling Clock: Binary values of 010 to 111 of R6-R4 correspond to Ext Clock, 25 μsec, 5 μsec, 2.5 μsec, 0.5 μsec, 0.25 usec sampling period. Number of Active Channels: Binary values of 00 thru 11 of R8-R7 correspond to 1, 2, 4 or 8 channels. Odd/Even Flag: Indicates an odd number of samples taken after the trigger causing an undefined last data word. (Single-channel mode only). Incompatible Switch Flag: R10 is set if combination of sampling rate and number of channels is not allowed.
F(2):	Read data registers. Successive F(2) commands will read successive 16-bit words from memory corresponding to two 8-bit samples, either the same sample of adjacent channels or successive samples of Channel 1. See F(16) below.
F(8):	Test LAM. Q response is generated if LAM is set.
F(9):	Initiate continuous sampling cycle, clear control register and reset LAM. (Equivalent to front-panel push button or C or Z.)
F(16):	Select channel to be read. Combination of front-panel switch position and sub-address lines determines the channel(s) to be read out as follows: 1 Channel Selected: A(0) enables readout of channel 1, with lower 8 bits containing first sample and upper 8 bits containing second sample. 2 Channels Selected: A(0) enables readout of channels 1 and 2 in lower and upper 8-bits, respectively. 4 Channels Selected: A(0) enables readout of channels 1 and 2 in lower and upper 8-bits, respectively; A(1) enables readout of channels 3 and 4 in lower and upper 8-bits, respectively. 8 Channels Selected: A(0) or A(1) or A(2) or A(3) enables readout of channels (1 and 2) or (3 and 4) or (5 and 6) or (7 and 8) respectively in a manner similar to above. Disable (LAM), Enable Display (see manual). Provides a "Stop Trigger" via the Dataway.
F(24):	Enable LAM and disable display. (This command necessary for any computer readout of the module.) The state of the LAM mask is arbitrary after power-up.
F(25):	
F(26):	

GENERAL

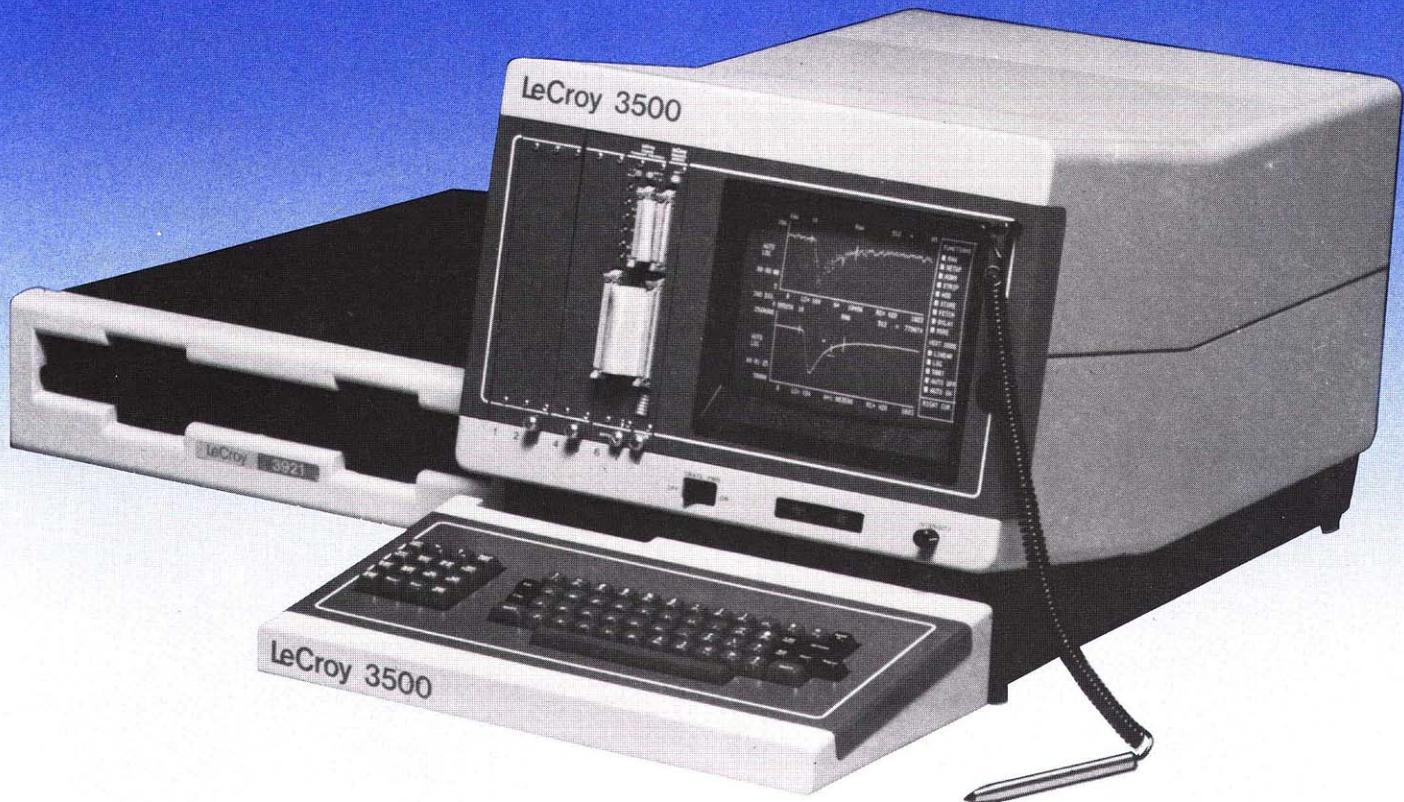
Interconnecting Cable:	To permit data transfer from the Model 2264 to the Model 8800A Memory Modules, a Model DC8800/n Data Cable is required, where "n" equals the number of memory modules linked to the 2264.
Packaging:	Conforms to the CAMAC standard for nuclear instrumentation modules (ESONE Committee Report EUR 4100e or IEEE Report #583); RF-Shielded #3 width modules.
Current Requirements:	1.50 A at + 6 V 250 mA at - 6 V 100 mA at + 24 V 50 mA at - 24 V

SPECIFICATIONS SUBJECT TO CHANGE

System 3500SA

FAST WAVEFORM ANALYZERS

Repetitive or transient signals digitized and averaged at high speed with the flexibility and storage of a digital computer.



- Sampling rates to 200 MHz
- High-speed averaging
- Wide dynamic range
- Modular expandability
- Light pen and dedicated keys for setup and operation
- Programmable in BASIC and FORTRAN
- Controls any CAMAC (IEEE-583) module

LeCroy

Innovators in high-speed instrumentation

PERFORMANCE FOR TODAY...



HIGH-SPEED SAMPLING...plug-in input modules provide digitizing rates up to 200 MHz, 100 MHz, or 32 MHz, allowing capture of wide-band signals.

INDEPENDENT MULTIPLE INPUTS...a number of the same or different input modules can be combined in one system and can operate simultaneously with separate rates and triggering, providing multiple views of one or many signals.

PRECISION DIGITIZING...8-bit digitizing with less than 5 psec "aperture uncertainty" and wide analog bandwidth assures accurate recording of dynamic signals — optional 20 mV sensitivity.

FASTEAST AVERAGING...700,000 samples/sec are averaged to achieve maximum noise reduction in the least time. On-line viewing allows the operator to manually stop averaging when the signal has sufficient quality.

LONG WAVEFORM MEMORY... 8 K samples for each input enables fine time resolution to be used over longer signals and insures the capture of transients whose timing is not precisely related to a trigger.

WIDE DYNAMIC RANGE...achieved by use of a 24-bit averager memory, preserving subtle differences in waveforms.

DATA CALCULATIONS...built-in programs aid in data interpretation with computations such as on-line FFT, smoothing, automatic peak listing, integration, and background subtraction.

FLEXIBLE DISPLAY...time expansion in any selected region reveals detail on-line or from stored data while still viewing the total signal. Automatic scaling optimizes display dynamic range; lin, log, or square root scales available; variable amount of pretrigger storage.

RECONFIGURATION, EXPANSION...a variety of compatible input and processing modules can be field installed; for example, histogramming and multichannel scaling plug-ins are available.

CP/M* BASED COMPUTER...user programmable in FORTRAN and BASIC, archive to floppy disc, hard copy using optional printer, five RS232 ports standard, and IEEE-488 GPIB optional.

*CP/M is a trademark of Digital Research, Inc.

...AND MODULAR EXPANSION FOR TOMORROW

MODULAR FLEXIBILITY

System 3500SA Analyzers are modular, digital instruments which accurately capture and process one or more fast transients or wide bandwidth repetitive signals. Signal processing includes fast averaging, FFT, smoothing, scaling and stripping. Active display allows waveforms to be presented in their most meaningful form as the data is acquired.

INDEPENDENT MULTIPLE INPUTS

Various configurations are possible with a choice of plug-in modules to match input signal characteristics and the type of processing needed. For example, three different input modules allow selection of maximum sample rates. The fastest is 200 Msamples/sec, which provides 5 nsec time resolution, ideal for sub-microsecond transients and signals with bandwidths to 100 MHz. Modules with 100 Msamples/sec and 32 Msamples/sec digitizing rates are also available. All input modules digitize with an amplitude resolution of 8 bits or 1 part in 256.

A COMPLETE SYSTEM

Since each module is a transient recorder with an independent clock, trigger, and waveform storage, **independent** multichannel signal acquisition is possible. Up to eight signals can be simultaneously acquired at **different sampling rates** and/or at **different times**. Alternatively, one signal can be digitized at a number of different rates, for example, to simultaneously acquire a total signal and a more detailed, shorter portion of it. In this way the fast leading edge of a transient can be captured with 5 nsec resolution and its slow decay with 31.25 nsec resolution. For frequency locked sampling, the clock output of one module can be used as the external clock input to multiple transient recorders.

EXPANSION

Each Analyzer consists of a multi-microprocessor main frame with a 9-inch raster scan CRT and a pair of 8-inch double-density floppy disc drives for archiving. Ultra-fast waveform averaging and rapid Fast Fourier Transforms (FFT) are made possible by bit-slice processor technology. Five RS232-C ports are standard. The system is a full-feature CP/M based computer, permitting user programmed data manipulation with FORTRAN or BASIC.

Each Analyzer contains eight CAMAC slots for front-end plug-in modules which conform to the CAMAC IEEE-583 International Standard. The Analyzer provides total control of any CAMAC module under FORTRAN or BASIC. Available LeCroy modules include: high sensitivity analog signal conditioning and trigger units, 12 and 13-bit analog-to-digital converters for multichannel nuclear analysis, time-to-digital converters for highly accurate time-difference measurements and histogramming, and multichannel scalers for event counting at rates up to 100 MHz. Another option is a dot matrix printer for graphics and text.

ACCURATE WAVEFORMS AT 200 MHZ DIGITIZING

Exceptionally high digitizing rates

of the System 3500SA input modules are made possible by LeCroy's proprietary hybrid and monolithic circuit designs. LeCroy's analog-to-digital converters provide accurate digitizing of rapidly changing analog signals. Typically, errors resulting from analog signals being sampled at the

"wrong" time (aperture uncertainty) are negligible when digitizing a full scale sine wave whose frequency is one-half the maximum digitizing frequency of the particular module. Aperture uncertainty (see box) is only 5 psec (5×10^{-12} sec) for the 200 MHz module. Likewise, response time, settling time, and slew rate are exceptionally fast.

ACCURATE DIGITIZING AND APERTURE UNCERTAINTY

Aperture uncertainty is defined as the time uncertainty between the digitizing clock and the instant of waveform sampling. As shown in Figure 1, the effect of uncertainty in time causes an inaccuracy in the amplitude conversion of a waveform. At frequencies up to

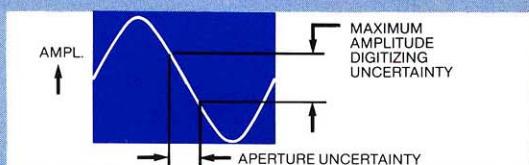


Figure 1. Typical effect of aperture uncertainty on amplitude accuracy.

Input Module	Maximum Sampling Rate	Aperture Uncertainty	Test Sine Wave Frequency	Accuracy Degradation Compared to Nominal 8 bits
LeCroy	200 MHz	± 5 psec	100 MHz	Negligible
	100 MHz	± 10 psec	50 MHz	Negligible
	32 MHz	± 15 psec	16 MHz	Negligible
Other 100 MHz Systems	100 MHz	± 100 psec	50 MHz	3 bits
	100 MHz	± 50 psec	50 MHz	>2 bits
	100 MHz	± 30 psec	50 MHz	~2 bits

Table 1. Effect of Aperture Uncertainty on Amplitude Accuracy

one-half the maximum sampling rate of the input module, the effect of the aperture uncertainty is virtually negligible in LeCroy systems. As aperture uncertainty increases, dynamic performance deteriorates. Table 1 illustrates this effect for values of aperture uncertainty outside the LeCroy specifications.

Very high dynamic range of averaged data — 16×10^6 or 144 dB — is made possible in the System 3500SA by the 24-bit word length in the averaging memory. The System 3500SA can accommodate the average of 65,536 full scale waveforms without truncation or overflow distortion. Low level waveform details are well preserved and small changes in waveform features from one experiment to the next can be detected. In contrast, if only a 16-bit word length were used in the averager memory, overflow would occur after averaging only 256 full scale (8-bit) waveforms, thereby limiting the attainable signal-to-noise enhancement.

Acquiring the total waveform of interest results from adjusting the record length to the signal while providing the desired time resolution. Digitizing rate and record length may be set differently for each input channel (module). A longer record with lower resolution may be obtained for all or a portion of a waveform, while simultaneously capturing another shorter portion with higher resolution. Record length can be as short as 256 points or as long as 8 K points for each input channel. Using additional (optional) memory, the system can digitize and store as many as eight channels of data of 8 K each.

Variable pretrigger allows a selected amount of information preceding the trigger to be stored and viewed. In the System 3500SA up to 7/8 of the waveform storage memory may be filled with pretrigger data.

For example, when measuring fluorescence induced by a laser pulse, pretrigger recording permits triggering on the laser shot and then "looking back" in time at the pretrigger waveform to establish a reference level.

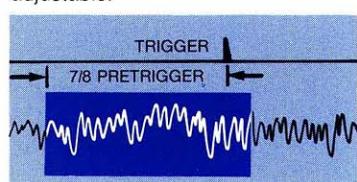


Figure 2. The amount of pre-trigger waveform captured is adjustable.

FASTEST AVERAGING... most noise reduction in the least time

System 3500SA is unique in its ability to average more than 700,000 waveform points per second, for example, 700 waveforms of 1 K sample points each. This high averaging speed significantly reduces data collection and experiment times and it provides the maximum improvement in signal-to-noise ratio in the shortest possible time. The System 3500SA speed also permits the efficient processing of data from phenomena stimulated by high repetition rate lasers or other fast pulse rate sources.

The number of points in the averaged waveform, or "record length," is selectable in binary steps from 256 to 8192. With this "memory segmentation," the user can choose between the length of the processed waveform and the maximum number of waveforms averaged per second. Averaging 10,000 waveforms of 1 K points each yields a signal-to-noise ratio improvement of 100 ($= \sqrt{10,000}$), and can be achieved by the System 3500SA in **less than 15 seconds**. By con-

trast, the traditional boxcar averager or typical multipoint averager takes many times longer, up to many hours, to achieve the same result (see Table 2).

Comparison Of Averaging Times

Type of System	Maximum Averaging Rate	Time to Average 10,000 1 K Point Waveforms		
		7 waveforms/sec	70 waveforms/sec	700 waveforms/sec
Typical Boxcar Averager	1 point per waveform	400 hours	40 hours	4 hours
Typical Multipoint Averager	10,000 points per second	24 min	16.7 min	16.7 min
LeCroy System 3500SA	700,000 points per second	24 min	2.4 min	14 sec

Table 2. Comparison of averaging times for various systems. The table indicates the total time required to achieve 100:1 signal-to-noise ratio improvement on a 1 K point waveform.

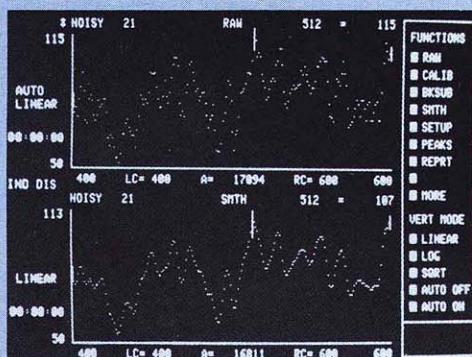


Figure 3. A noisy transient and a smoothed version of the same transient.

On-line viewing during even the fastest averaging is possible without interrupting or slowing down either the averaging or display updating, and is the result of the unique multiprocessor architecture of the System 3500SA. It allows the user to evaluate the average as it builds up and to stop it manually as soon as the waveform features are sufficiently clear. In this manner the experimenter can be assured that the measurements are proceeding as expected. For exponential averaging the user can observe long term trends, including changes in waveforms from dynamic experimental conditions.

A variety of averaging modes is provided to fit the characteristics of the signal measured. **Summation averaging** achieves the maximum signal-to-noise improvement in a given time for random noise processes. A maximum of 65,536 full scale signals (8 bits each) can be averaged into the 24-bit memory without overflow. Assuming statistically independent noise from one waveform to the next, this summa-

tion of waveforms results in a $256 \times (= \sqrt{65,536})$ improvement in signal-to-noise ratio. All 24 bits of the averaging memory are available for readout.

Exponential averaging is a continuous averaging process which weights the most recent waveforms more heavily than older waveforms. This type of averaging is useful when the waveforms exhibit relatively slow time variations. In exponential averaging the contribu-

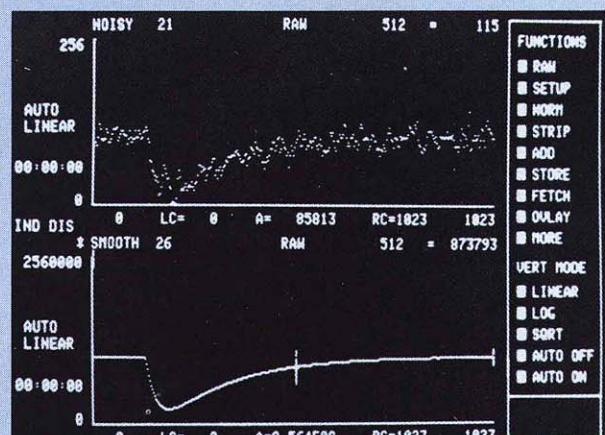


Figure 4. Viewing of a noisy signal and its average is possible on the System 3500SA split screen display.

tion of older waveforms decays exponentially, in contrast with summation averaging, where each waveform contributes equally to the final average. The exponential time constant may be chosen so that short term fluctuations are averaged out while longer term trends remain visible. When the exponential weighting factor is set to zero, no averaging takes place and the display is continually updated with the most recent unaveraged waveform.

COMPUTATION AND DISPLAY FLEXIBILITY...aids understanding

System 3500SA intelligence extends to data manipulation, multiple display formats, fast disc storage and recall, and communication.

Computation of area under a portion of the waveform is obtained by setting the two cursors at the two extremes of the region of interest. The area under the selected portion of the waveform is displayed on the CRT.

Autoscaling sets the amplitude maximum in the display to match the highest point in the displayed waveform, insuring that all the peaks of the waveform are on the screen. Proper scaling is maintained when the display is expanded. Autoscaling can be disabled by a simple light pen command so that scale values can be entered from the keyboard.

Flexible display formats include linear, log, or square root of the amplitude as chosen for the best waveform appearance. Waveforms can be displayed singly or in combination as dual up/down or dual overlayed. Overlayed curves can be scaled and offset to simplify comparison.

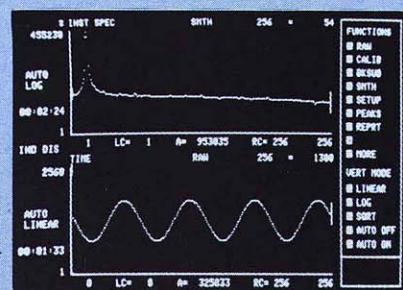


Figure 5.

FFT conversion the frequency domain can be performed on a 1 K portion of the waveform. Averaged time domain data can be transformed and the power spectrum itself can be averaged. Uniform, Hanning, or user defined weighting functions can be applied. FFT calculation time is less than 1 second for 1 K points. The spectrum can be displayed **while** acquiring time domain data.

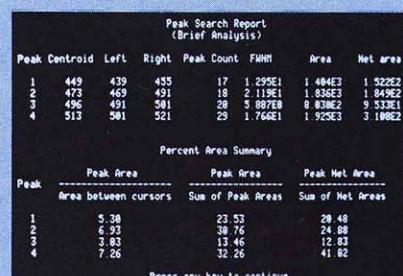


Figure 6.

Peak search locates waveform peaks which exceed a user set threshold and width. Each valid address, amplitude, and peak area is listed in a report format.

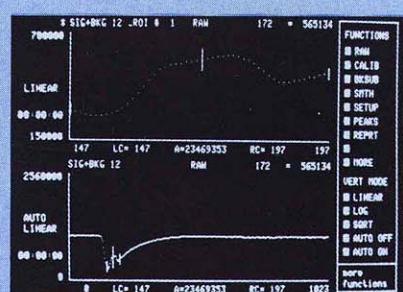


Figure 7.

Expansion between cursors provides increased visual resolution for detailed waveform examination. An on-line dual display shows the expanded segment simultaneously with the unexpanded waveform. The cursor defined segment can be scanned along the waveform **while** viewing the expanded region for accurate positioning.

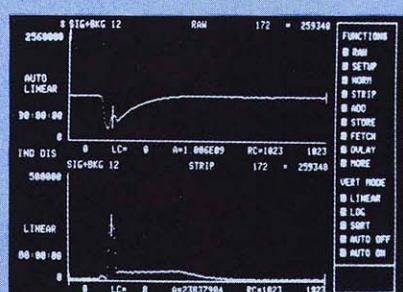


Figure 8.

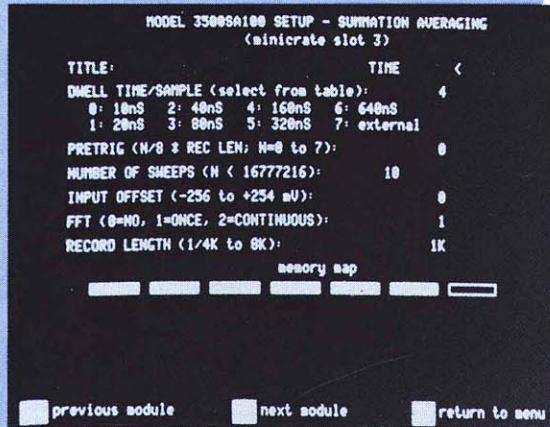
Background subtraction permits the removal of unwanted linear experimental artifacts from the waveform. Any two waveforms can be subtracted or added following independent scaling on each. Resultant waveforms can be stored in memory or on floppy disc.

SIMPLIFIED CONTROL

...menus, light pen, and keypad

A built-in light pen provides a fast, simple means of selecting menu items. Three main menus present a hierarchy of setup, with the most often used parameters chosen from the module SETUP MENU (see Figure 11) or from a menu of functions on the waveform display itself. (For example, see right side of Figure 4.)

Figure 11.



MODULE SETUP MENU includes the settings for each input module: dwell time/sample, pretrigger delay, number of sweeps per average (weighting factor in exponential averaging), input DC offset, FFT processing command, and the memory destination for the digitized waveform. Each input module may be assigned a title.

The KEYPAD on the System 3500SA provides simple, one key-stroke implementation of many of the more common system and display commands. The following are particularly useful:

Cursor Manipulation: Left and right arrow keys provide for movement of either of the two cursors or a "marker" along the displayed waveform. These positions can also be defined numerically from the keyboard.

Acquisition Start: Begins data acquisition from all input modules and initializes the acquisition timing.

Vertical Max/Min: Permits scaling the display to a desired amplitude

3500 SA System Architecture			
slot	module type	module types	module types
1	empty	TR8837SU	TR8818SU
2	empty	TR8837EX	TR8818EX
3	empty	3511	3521A
4	empty		
5	empty		
6	TR8818SU		
7	empty		
8	empty		

Figure 10.

SYSTEM ARCHITECTURE MENU

reviews plug-in module locations and provides a choice of averaging modes.



Figure 12.

THE KEYPAD

when the autoscaling function is not selected.

Memory Group: Allows the user to scroll through the entire memory in the system using the arrow keys. One memory group is assigned to each input module in normal operation.

Regions-Of-Interest Functions: A region-of-interest (ROI) can be created by positioning the left and right cursors on a displayed waveform. ROI's thus defined may be stored and recalled at will using the ROI and arrow keys to scan through the various defined regions.

User Designed Computation Routines: Written in either FORTRAN or BASIC, these can be used

3500 SA SETUP Version 2.0

- Load system file
- System Architecture
- Module Set-up
- Save system file
- Return to graph



Figure 9.

SETUP MENU provides a directory for initializing the system or choosing other menus.

SYSTEM 3500SA SPECIFICATIONS

SPECIFICATIONS SUBJECT TO CHANGE

October 1984

INPUT CHARACTERISTICS:

System 3500SA configurations include:

	32 MHz Module	100 MHz Module	200 MHz Module
Number of Modules per System (max):	8.	1 (may be combined with up to two 32 MHz Modules.)	1 (may be combined with one 32 MHz Module.)
Maximum Sampling Rate:	32 Msamples/sec	100 Msamples/sec	200 Msamples/sec
Internally Generated Sample Periods:	31.25 to 2000 nsec in 6 steps(1)	10 to 640 nsec in 6 steps(1)	5 to 320 nsec in 6 steps(1)
External Digitizing Clock Input Maximum Frequency: Pulse Duration:	32 MHz 12 nsec, min	100 MHz 5 nsec, min	200 MHz 5 nsec \pm 5%
Number of Bits:	8 bits (256 levels)	8 bits (256 levels)	8 bits (256 levels)
Aperture Uncertainty	\pm 15 psec	\pm 10 psec	\pm 5 psec
Effective Accuracy vs. Signal Frequency:(2)	DC-5MHz: 0.8% FS 5-16MHz: 1% FS	DC-5MHz: 0.8% FS 5-16MHz: 1% FS 20-50MHz: 1.6% FS	DC-5MHz: 0.8% FS 5-20MHz: 1% FS 20-100MHz: 1.6% FS
Analog Bandwidth: (without 6102)	>100 MHz (-3 dB)	>100 MHz (-3 dB)	>100 MHz (-3 dB)
Full Scale Sensitivity:	512 mV p-p	512 mV p-p	512 mV p-p or 5.12 V p-p(3)

(1) A/D conversion rate can be set independently for each input.

(2) "Effective Accuracy" describes the dynamic performance of transient recorders including front-end circuitry and AD converter. When higher frequency signals are being digitized the effective accuracy decreases due to circuit response time, settling time, and slew rate limitations in the electronics. The sum of all these high frequency effects is small in the System 3500SA.

(3) 512 mV and 5.12 V inputs are linearly summed prior to digitizing; signal connections can be to either or both inputs.

Sensitivity (with 6102): 50 mV to 2.5 V p-p.

Adjustable Offset: \pm half of full scale on all ranges.

Impedance: Standard - R = 50 ohms; C = 15 pF nominal.

Maximum Input Voltage: (50 Ω Source) \pm 100 V for 100 μ sec; \pm 2.5 V continuous.

Overdrive Recovery: Recovers to within \pm 1 LSB in 25 nsec following 2 \times full scale input.

Trigger: TTL or ECL (jumper selected); positive going edge.

Trigger (with 6102): 50 mV to 2.5 V.

FFT: A 1 K segment of waveform can be transformed to 512 spectrum points in less than one second; averaging of spectrum power; Uniform, Hanning, or user-defined weighting; concurrent displays of frequency and time domain data.

DISPLAY

Waveforms: Data displayed on-line, from memory or recalled from disc storage.

Format: Single or dual display; displays can be independent or subsets of each other.

Vertical Scale: Linear, log, or square root; upper and lower limits can be entered manually or via autoscale function.

Horizontal Expansion: Waveform segment between two settable cursors can be expanded to full width of display; cursors can be scanned through a waveform while viewing expanded portion on top half of dual display.

Normalization: Subtracts a chosen base value from a waveform and then multiplies the result by a constant.

Stripping: Multiplies a waveform by a chosen constant, then subtracts the result from another curve; constant may be selected automatically from waveform values.

Clock: Displays elapsed time from start of data collection until manual stop command.

MASS STORAGE

Medium: Dual 8-inch floppy discs; single sided, double density.

Capacity: 16 records of 8 K \times 24 bits; total memory is always stored on command, along with header containing date, time and experimental parameters.

Transfer Time: About one second for 1 K 24-bit words.

Setup Storage: Individual sets of setup parameters can be stored on and recalled from floppy disc files for simple repetition of measurements.

Auto-Program: Permits storage on disc of strings of keystroke commands and/or light pen entries for later execution.

REAR PANEL OUTPUTS

Printer: Dedicated RS232-C port for output to LeCroy Model 3931A Graphic Printer.

Digital: RS232-C (4 ports in addition to the printer port) at 75 to 19,200 baud are standard; GPIB optional.

Video Output: Composite video available at BNC connector for external display or video recorder/plotter.

PHYSICAL

Console: 15.85 in (40.2 cm) high \times 17.38 in (44.1 cm) wide \times 24.77 in (62.9 cm) deep; keyboard adds 7.8 in (19.6 cm) to depth.

Disc Drive: 5.25 in (13.3 cm) high \times 17.6 in (44.7 cm) wide \times 21 in (53.4 cm) deep.

Weight: Console - 80 lbs (36 kg); Disc Drive - 48 lbs (21.6 kg).

Operating Temperature: 15° to 40° C (60° to 104° F) at 10% to 95% relative humidity.

Power: 115/230 Vrms (\pm 10%), 50/60 Hz, 1200 VA max.

HOW TO ORDER A 3500 SA SYSTEM

The System 3500SA is available in three basic configurations:

3500SA32: Includes **two** input modules with 32 Msamples/sec maximum sampling rate each and one 8 K \times 24-bit waveform memory.

3500SA100: Includes **one** input module with 100 Msamples/sec maximum sampling rate and one 8 K \times 24-bit waveform memory.

3500SA200: Includes **one** input module with 200 Msamples/sec maximum sampling rate and one 8 K \times 24-bit waveform memory.

Extra Input Modules: Extra 32 Msamples/sec input modules, Model TR8837F, may be ordered for any of the above systems: up to six additional modules may be installed in the 3500SA32; up to two additional in the 3500SA100; and one additional module in the 3500SA200. (For multiple 100 MHz or 200 MHz input modules consult the factory).

Extra Waveform Memory: Extra blocks of 8 K \times 24-bit waveform memory, (Model 3500-2) may be added to any of the above systems. A maximum of seven (7) additional memory blocks, for a total of 8 (64 K \times 24-bit) may be installed in any system.

Signal Preamplifier/Trigger Generator Option (Model 6102): Provides signal conditioning and trigger generation for signal inputs which do not fall within the "standard" specification limits (see page 6 and specifications). One Model 6102 option may be installed for each input module in the System, if desired. Space in the System 3500SA is limited to eight slots. Since each 32 Msamples/sec module requires one slot and each Model 6102 option also requires one slot, the configuration must be confined to the space available.

Peripherals and Accessories:

Model 3931A Printer/Plotter: Supplied with interface cable to dedicated RS232C port on System 3500SA.

GPIB Interface, Model 3500-38: Provides GPIB (IEEE Standard 488-1978) Input/Output for interconnection to other devices.

Software: BASIC or FORTRAN. The System 3500SA includes a choice of either FORTRAN or BASIC for the user programming facility. Please specify your choice when ordering the system. If both FORTRAN and BASIC are desired, specify 3910-3.

LeCroy

TECHNICAL DATA

LeCroy



Model 6102

Amplifier/Attenuator and Trigger Generator

- Two amplifiers and one trigger generator in a single-width module
- Wideband, DC coupled operation, 0 to 150 MHz
- Extend 0.5 V transient recorder inputs from 50 mV to 2.5 V in six ranges
- Less than 2.5 nsec risetime
- Excellent temperature stability
- Internal or external trigger source
- Adjustable trigger level and slope
- Built-in test pulser/noise generator
- Provision for powering optional external Hi Z probes

The LeCroy Model 6102 houses two independent amplifier channels and one trigger generator which have been optimized for use with LeCroy's high-speed transient recorders. Each amplifier channel is identical and extends the range of recorders with 0.5 V, 50 Ω inputs from 50 mV to 2.5 V in six gain steps. The impedance at the front-panel input connector is 50 Ω and is designed to provide terminated operation with coaxial cable inputs. Recessed connectors on the module provide power for the optional Model 6102P Hi Z (1 M Ω) Probe Accessory which may be used with sources requiring a high impedance. The amplifiers are completely direct coupled and offer a 3 dB bandwidth from 0 to greater than 150 MHz. Input signals can be bipolar or unipolar of either polarity, provided they are within the selected p-p range. The output for a full-scale input is 0.5 V p-p and is designed to drive a 50 Ω impedance.

A front-panel DC offset potentiometer permits the quiescent output to be adjusted \pm 100 mV to compensate for input DC offsets of up to 20% of the full scale range. The gain and DC offset are both very stable with temperature, varying less than 0.2% per degree C. Output noise is less than 60 μ V RMS or less than 2% of full scale, making the amplifier suitable for use with digitizers having resolutions under 9 bits.

Normally, both amplifiers are driven by their respective inputs. However, to facilitate system setup, a front-panel switch connects an internal pulse generator to either input. A side-panel jumper allows the user to sum an internal noise generator with the test pulse train for use in checking signal averaging systems.

The trigger generator section is designed to accommodate a wide range of input signal conditions and give flexible control over trigger pulse generation. In providing stop triggers to transient recorders, it is used much like the trigger section in a standard oscilloscope.

The source of the trigger signal is either the external input or the internal amplifier Channel B as determined by a front-panel switch. In internal, the trigger range is identical to the amplifier range; in external the range is \pm 2 V into a 1 M Ω impedance. When used with high-speed signals, an external 50 Ω terminator may be required to prevent unwanted cable reflections.

The trigger generator produces a TTL level output (quiescently 0 V, switching to 2.5 V for 80 nsec) approximately 15 nsec after a signal with the selected slope crosses the input level determined by the input level control. The output is capable of driving 25 Ω or greater and is compatible with all LeCroy transient recorders.

The Model 6102 is packaged in a single-width CAMAC module that utilizes BNC connectors for all inputs and outputs. Adapter cables are available to connect the unit to the analog and trigger inputs of devices employing either Lemo or SMA connectors. All controls and operating parameters are manually set; no CAMAC control is provided.

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SPECIFICATIONS

Model 6102

AMPLIFIER/ATTENUATOR AND TRIGGER GENERATOR

AMPLIFIER CHARACTERISTICS (Channel A and B)

Input Range:	Six input steps from 50 mV p-p to 2.5 V p-p full scale provide outputs of 0.5 V p-p over a 1.0 V range. (Signals can be bipolar, positive unipolar or negative unipolar. For example, a 100 mV p-p signal can be at any voltage level from + 100 mV to - 100 mV.)
Range Accuracy:	$\pm 3\%$ of full scale $\pm 0.2\%$ per $^{\circ}\text{C}$.
Input Impedance:	$50 \Omega \pm 2\%$ for inputs not exceeding $10 \times$ input range settings; direct coupled.
Input Protection:	± 5 V DC continuous, except on 100 mV and 50 mV ranges which are limited to 2 V DC and 1 V DC respectively.
	50 Vpk (applied for less than 1 msec and duty factor not exceeding 10%) except on 50 mV range which is limited to 25 Vpk.
Test Pulse:	Front-panel switch allows selection of internally generated alternating positive and negative monopolar test pulses for use in setup or rough system check (not intended for calibration). Leading edge time constants are about 10 nsec, trailing edges are about 100 nsec, equivalent Input amplitudes are approximately ± 25 mV when single channel is selected. (Test Pulse must be disabled on both channels during normal use or feedthrough may result.)
Noise Generator:	Side-panel jumper sums wideband noise generator into Test Pulse for use in setup or checking signal averaging systems. Equivalent Input amplitude is approximately 10 mV RMS when single channel is selected.
Output Linear Range:	Noninverting 0.5 V p-p signals over 1.0 V range.
Output Impedance:	0.25 Ω source resistance optimized for 50 Ω load, but will drive any impedance of 25 Ω or greater.
DC Offset:	Front-panel potentiometer allows output to be DC offset up to 100 mV positive or negative with drift less than $\pm 200 \mu\text{V}/^{\circ}\text{C}$ at output with input grounded.
Frequency Response:	DC to 150 MHz (3 dB).
Output Noise:	Less than 600 μV RMS.
Overdrive Recovery:	Recovers to within 1% from $\times 2$ overdrive in 5 nsec, from $\times 10$ overdrive in 25 nsec.
External Hi Z Probe:	Optional Probe available to be used on either or both channels. Provides high impedance input, 50 Ω output, packaged in minibox. Recessed power connectors on amplifier module.

TRIGGER GENERATOR CHARACTERISTICS

Input Range:	Internal Trigger selects Channel B amplifier output as source; therefore the range tracks the amplifier setting. With an External Trigger input the range is ± 2 V.
Level Control:	Front-panel markings allows setability to ± 50 mV or $\pm 10\%$ of setting, whichever is greater.
Slope:	+ or - corresponding to a rising or falling level.
Input Impedance:	Greater than 1 M Ω paralleled by 8 pF for inputs not exceeding 3 V; direct coupled.
Input Protection	± 5 V DC continuous, 50 Vpk (applied for less than 1 msec and duty factor not exceeding 10%).
Trigger Output:	Quiescently 0 V, switching to + 2.5 V for approximately 80 nsec when input signal crosses level. Rise and falltimes nominally 10 nsec. Low source resistance optimized for 50 Ω load, but will drive any impedance of 25 Ω or greater.
Propagation Delay:	Approximately 15 nsec.

GENERAL

Connectors:	All BNC type.
Controls:	All operating parameters are manually set.
Packaging:	In conformance with the CAMAC standard for instrumentation modules (IEEE Standard 583, European Esone Report EUR4100). RF-shielded CAMAC #1 module.
Temperature Range:	Ambient operating range to maintain specifications; + 10 $^{\circ}\text{C}$ to + 30 $^{\circ}\text{C}$.
Power Requirements:	190 mA at + 6 V 50 mA at + 24 V 130 mA at - 6 V 120 mA at - 24 V Plus optional external probe power.

SPECIFICATIONS SUBJECT TO CHANGE

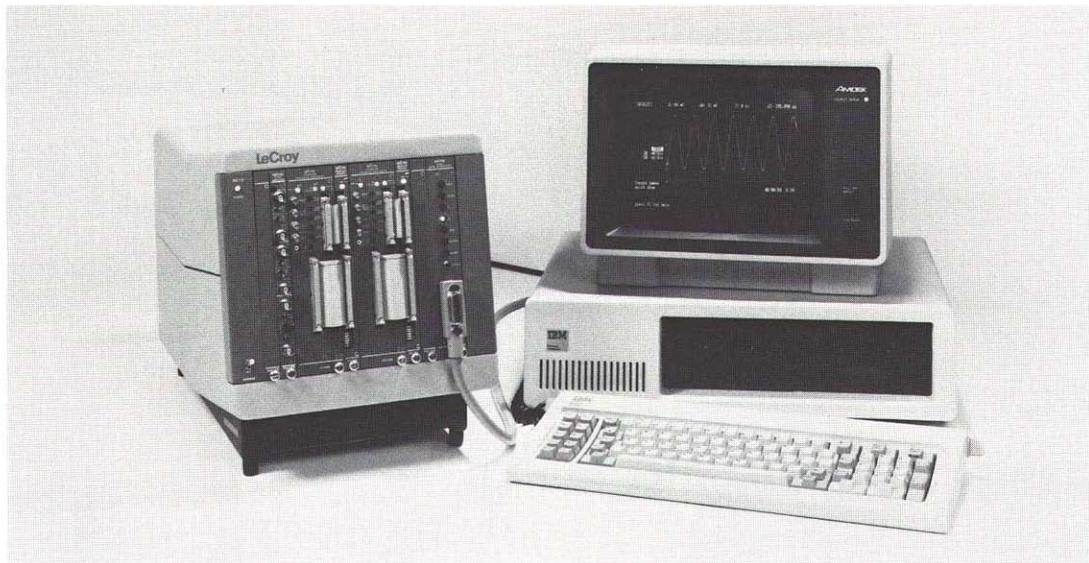
Model 8013 Instrument Module Housing

- 13 module plug-in slots
- 350 W power output
- Instrumentation quality regulation for AC line changes and for large load changes
- Fast regulation response time
- Wide operating temperature range
- Low temperature coefficient
- Internal energy storage for protection against brief line power interrupt
- Thermal protection
- Short circuit and overvoltage protection
- RFI filter



The Model 8013 Instrument Module Housing is a mainframe for configuring benchtop instruments from LeCroy plug-in instrument modules. It provides all operating power, cooling and an instrumentation quality receptacle for up to eleven instruments, plus a two-slot wide position for digital I/O (such as LeCroy's Model 8901 GPIB Interface).

Modular packaging offers major advantages. The number and type of Transient Waveform Digital Recorder channels required can be combined into a single instrument housing. Control and signal conditioning plug-ins such as trigger generators, sampling clock generators, amplifiers, and attenuators can be selected to tailor the instrument configuration to the application. Plug-ins can be interchanged among mainframes to meet changing requirements without additional cost. New modules incorporating advances in technology can be added to cost-effectively upgrade instrument performance. LeCroy Instrument modules are designed and manufactured to be compatible with IEEE Std. 583, CAMAC (Computer Automated Measurement and Control). This assures unrestricted choice of modules for tailoring your instrument or system configuration (including CAMAC modules from other manufacturers).



Model 8013 with GPIB Interface and installed transient recorder modules. Photograph shows Model 8013 Instrument Housing in an IBM PC controlled system.

SPECIFICATIONS Model 8013 INSTRUMENT MODULE HOUSING

MODULE CAPACITY

Number of Modules:

13 module plug-in slots allow installation of up to 11 single width CAMAC instrument modules (or any combination of different width modules not exceeding 11 slot widths) plus a single #2 width module for digital I/O.

Power Available:

21 A of + 6 V 21 A of - 6 V
2.5 A of + 24 V 1.5 A of - 24 V

All supplies are independent. Maximum current can be drawn from all supplies simultaneously. Total DC power available is 350 watts.

PERFORMANCE

Ripple:

Maximum of 50 mV peak-to-peak (50 MHz bandwidth).

Line Regulation:

\pm (0.1% + 1 mV) for line changes within AC limits specified below.

Load Regulation:

$<\pm$ 1% for no load to full load changes on \pm 24 V supplies and $<\pm$ 3% for no load to full load on \pm 6 V supplies.

Temperature Coefficient:

<100 ppm/ $^{\circ}$ C.

Long Term Stability:

$<0.1\%$ /8 hours of constant load and temperature. Measured after 1 hour warm-up.

Response Time:

Settles to within 1% of final value in less than 500 μ sec for 50% to 100% load change.

Energy Storage Time:

16 milliseconds holdup after loss of AC power.

GENERAL

Overload Protection:

Built in overvoltage protection. Protected against overload by current limit circuit; short-circuit proof.

Cooling:

The instrument module plug-in compartment is thermally isolated from the power supply. Two separate fans on the bottom of the Model 8013 Instrument Module Housing provide bottom to top positive airflow. The unique package profile assures good air access to the fan inlets even when placed on a solid flat surface.

Thermal Protection:

Thermal sensor in supply shuts down supply in the event of cooling failure.

Ambient Temperature Range:

+ 0 $^{\circ}$ C to 50 $^{\circ}$ C.

Line Power:

110 \pm 12% or 230 V \pm 12%

47 to 65 Hz.

450 watts maximum.

RFI:

A power line interference filter controls conducted RFI both into and out of the housing. By controlling RFI conducted onto the power cord, the filter also significantly reduces radiated RFI.

Power Cord:

The 2.3 m (7.5 ft.) 3 conductor line cord plugs into a rear panel connector.

Control and Indicators:

Front panel power light. Circuit breaker on left rear side. Front panel power off switch.

Size:

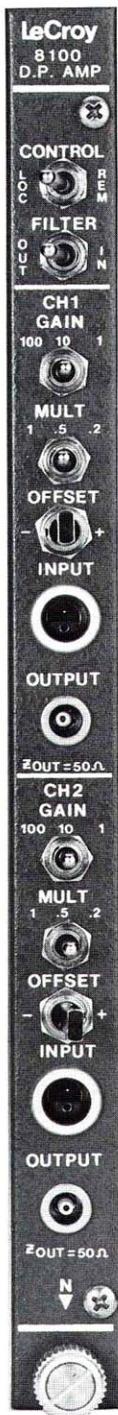
356 mm H, 292 mm W, 546 mm D (14" \times 11.5" \times 21.5").

Weight:

16 Kg (35 lbs.).

TECHNICAL DATA

LeCroy



Model 8100 Dual Programmable Differential Amplifier

- Programmable input range from 0.1 V to 50 V full scale
- Good common mode rejection
- DC to 1 MHz (3 dB) frequency response
- Switch-selectable 200 kHz cut-off filter
- Programmable offset range of ± 5.5 V

The LeCroy Model 8100 Programmable Differential Amplifier is designed to provide signal conditioning and noise immunity for experiments where gain has to be optimized quickly and flexibly to extend the dynamic range of the following instrumentation. The gain of the amplifier is fully programmable by computer through the international standard CAMAC interface. All settings can also be made by hand to facilitate setup or to operate without a computer.

The single-ended outputs are designed to match the line of CAMAC transient recorders offered by LeCroy. The outputs can drive a high impedance to ± 10 V or a $50\ \Omega$ impedance to ± 2.5 V. The differential inputs are accommodated by a shielded two-element Lemo connector and can operate in the presence of a common signal of up to 100 V. A switch-selectable cut-off filter is available to limit the 1MHz bandwidth to 200 kHz in order to prevent aliasing when in use with the LeCroy Model 8210 or Model 2264 Transient Recorders (typical sampling rates of 1 MHz). The common mode rejection is 100 to 1 at 100 kHz on the 100 mV range, and 60 dB at 60 Hz on all ranges.

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SPECIFICATIONS

Model 8100

DUAL PROGRAMMABLE DIFFERENTIAL AMPLIFIER

INPUT CHARACTERISTICS

Type:	Differential Amplifier, shielded 2 element LEMO connectors.
Impedance:	1 M Ω , 30 pF.
Input Ranges:	9 steps from 0.1 to 50V in a 1, 2, 5 sequence. Locally settable by 2 three position switches for 0.1, 1, and 10 volts with a multiplier of 1, 0.2, and 0.5. Programmable by computer in the same steps. Each channel can be independently set.
Common Mode Range:	± 5 V on 0.1, 0.2, and 0.5V ranges. ± 50 V on 1, 2, and 5V ranges. ± 100 V on 10, 20, and 50V ranges.
Common Mode Rejection:	100:1 at 100 kHz on 0.1V range. 60dB at 60 Hz on all ranges.
Input Protection:	200V for 10 μ sec on all sides.
Frequency Response:	dc to 500kHz (1dB); dc to 1 MHz (3dB).
Anti-aliasing filter:	Switch selectable 2 pole butterworth filter with 200 kHz cutoff (3dB point). Switch selects filters for both amplifiers at once; computer interface can select filter on each amplifier separately.

OUTPUT CHARACTERISTICS

Linearity:	$\pm 0.05\%$
Maximum Linear Range:	± 10 V into high impedance (± 2.5 V into 50 Ω).
Noise:	10mV pp (2mV with filter). Tangentially measured.
Output offset Temp. Coefficient:	10mV/°C.
Output Impedance:	50 Ω

GENERAL

Gain:	Settable for each channel in steps of 0.2 to 100 in a 1, 2, 5 sequence. See input range. Gains should be divided by 2 when driving 50 Ω . Accuracy is better than $\pm 3\%$.
Input Offset Voltage:	Computer settable by on-board DAC (offset binary code). Front panel toggle-switch to set offset driving the DAC with up/down counter so that offset is readable and reproducible when switching from local to remote. When driving high impedance, resolution is approximately 2.7 mV/step referred to the output with a range of ± 5.5 V (12 binary bits). Driving 50 Ω DAC resolution is approximately 1.35 mV/step within a ± 2.75 V range. With digital data input set for 0 offset, offset is within 50 mV of 0.000 Vdc. For full-scale offset data, accuracy is better than 3%.

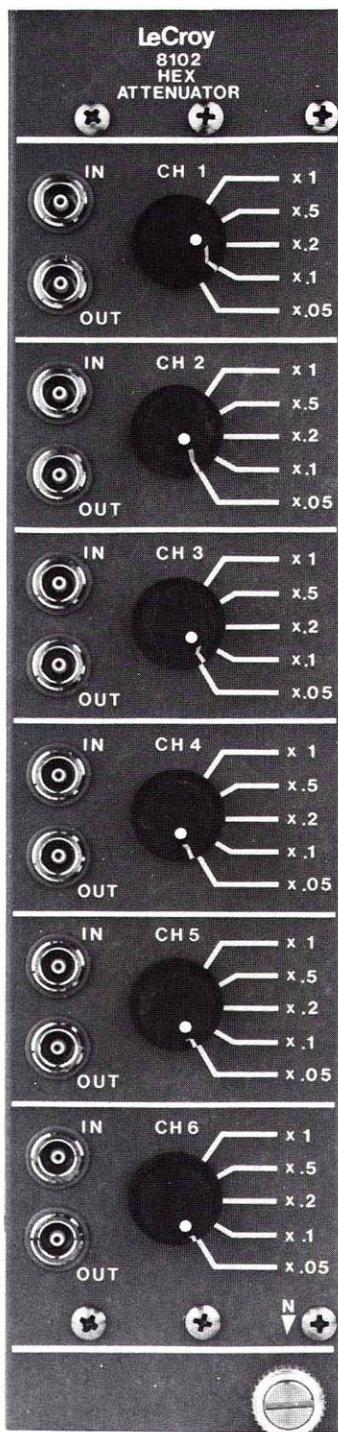
CONTROL AND READOUT FUNCTIONS

CAMAC Commands:	Q: A Q = 1 response is generated only in recognition of a F(1)•N or F(0)•N when a valid word is being read. X: An X = 1 (Command Accepted) response is generated when a valid F, N, and A are generated.
CAMAC Code:	F(0)•A(0): Reads channel 1 gain. F(16)•A(0): Sets channel 1 gain at S2. F(1)•A(0): Reads channel 1 offset. F(17)•A(0): Sets channel 1 offset at S2. F(0)•A(1): Reads channel 2 gain. F(16)•A(1): Sets channel 2 gain at S2. F(1)•A(1): Reads channel 2 offset. F(17)•A(1): Sets channel 2 offset at S2. The A1-A8 lines are used to address the desired amplifier circuit. A(0) address amplifier #1 (upper amplifier), A(1) addresses amplifier #2 (lower amplifier). F(0) reads gain and status information on the addressed amplifier. Status can be read whether or not the unit is in remote mode. Gain status is read on bit 1-6; bit 7 indicates status of amplifier ground setting, bit 8 indicates status of filter switch. When amplifier #1 is addressed, bit 9 indicates status of remote/local switch. F(16) sets gain of the addressed amplifier. Bits 1-6 set amplifier gain, bit 7 can ground inputs, bit 8 switches the filter in or out. F(1) reads the setting of the offset DAC on the addressed amplifier. Setting is offset binary, and data appears on the R1-R12 lines, with R1 the LSB and R12 the MSB. DAC setting can be read whether or not the unit is in remote mode. F(17) sets the offset DAC on the addressed amplifier. Offset data is accepted on lines W1-W2, with W1 the LSB and W12 the MSB. DAC Polarity: Programming all (1)'s into the offset DAC register will offset the amplifier's output by the maximum negative amount (approximately -5.5V), assuming no input signal.
Packaging:	In conformance with the CAMAC standard for modules (IEEE Std.#583, USAEC Reports TID-25875, ESONE Report 4100e) in an RF shielded #1 CAMAC package.
Current Requirements:	420 mA at + 6 V 20 mA at - 6 V 140 mA at + 24 V 130 mA at - 24 V

SPECIFICATIONS SUBJECT TO CHANGE

TECHNICAL DATA

LeCroy



Model 8102 Hex Step Attenuator

Six independent channels with one input and output each provide front-panel settable attenuation factors of 1, 2, 5, 10, and 20. The position of each switch can be read out digitally to a computer.

This high density unit can be relied upon to give flexibility and convenience to any data acquisition system using coaxial cables, especially systems of high speed and moderate resolution. The full-scale input of LeCroy transient recorders can be extended by attenuation of the input signal with a Model 8102.

SPECIFICATIONS

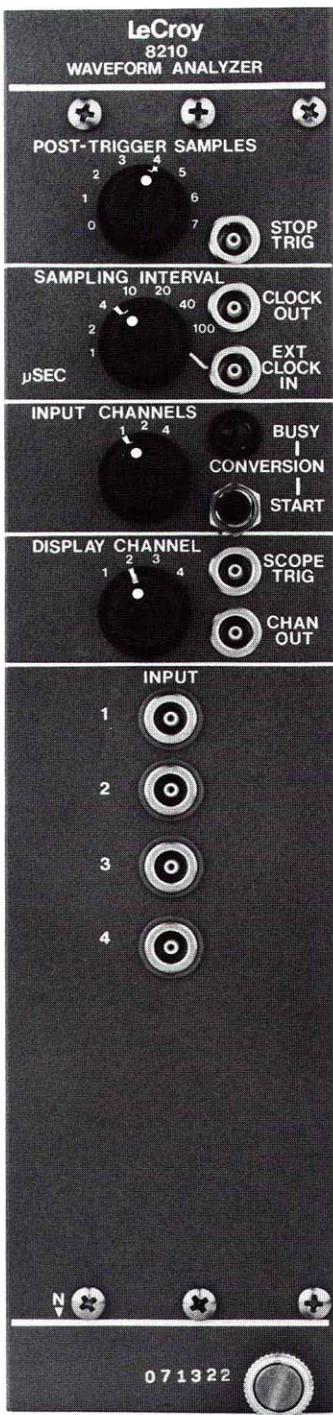
Channels/Module:	Six
Input:	50 Q impedance, Lemo connectors
Output:	50 Q impedance, Lemo connectors
Attenuation:	1, 2, 5, 10, 20. Switch-selectable for each channel
Accuracy:	4%
Rise and Falltimes:	2 nsec
Reflection Coefficient:	4% for risetimes \geq 20 nsec
Grounding:	Each channel ground floats relative to each other and to chassis ground.
CAMAC Commands:	F(0): Read status of front-panel switches (A(1)]A(6)).
Packaging:	CAMAC triple width module. In conformance with IEEE Standard #583 and ESONE Report EUR 4100e.
Power Requirements:	140 mA at +6 V

SPECIFICATIONS SUBJECT TO CHANGE

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TECHNICAL DATA

LeCroy



Model 8210 Quad 10-Bit Transient Digitizer

- 4 Analog inputs
- 10-bit resolution
- 10mV/count sensitivity
- ± 100 psec aperture uncertainty
- Simultaneous sampling (<5 nsec uncertainty)
- 5 MHz analog bandwidth
- Front-panel post-trigger sample select
- Large scale expandable memory of 32K words/module
- Protected inputs
- Built-in display driver
- System compatibility—part of a LeCroy digitizer family
- Varying clock rates possible

The LeCroy Model 8210 Quad 10-Bit Transient Digitizer is part of an expanding line of LeCroy products for the study of transient phenomena. The 8210 offers the user a medium speed, high performance, modular waveform digitizer designed in accordance with CAMAC standards, providing high data transfer rates and system flexibility. Up to 4 analog inputs to the 8210 are sampled simultaneously by track-and-hold circuits having analog bandwidths greater than 5 MHz and channel-to-channel sampling uncertainty of <5 nsec. The analog signal is digitized by a 10-bit, successive approximation ADC. The data is stored in the Model 8800A memory module under the control of the 8210. Each 8800A module has a capacity of 32K, 10-bit words; up to 3 memory modules may be used in a serial fashion. The memory per channel is the total memory divided by the number of active channels. (Further expansion possible as factory option.)

The data is read out through the memory control circuitry in the Model 8210. Each of the four channels can be separately addressed. Readout is non-destructive, and a DAC display is provided for presentation on any scope.

The flexibility of the design concept also allows the external clock frequency to be varied with time, permitting "importance" sampling along a single waveform. LeCroy's CAMAC Model 8501 Programmable Three-speed Clock Generator provides a wide range of clocking capabilities including "importance" sampling under CAMAC control.

The flexibility of 8210 may be enhanced through the use of the Model 8100 Dual Programmable Differential Amplifier. This module affords excellent common mode rejection and offers a wide range of CAMAC-programmable gain.

The 8210 system digitizes continuously, which allows retention of waveform data recorded before the stop trigger. This pretrigger sampling capability allows recording the baseline value previous to the occurrence of the meaningful signal or allows triggering from a feature of the signal while retaining previous detail.

The Model 8210 is packaged in a #3 width CAMAC module. All integrated circuits are socketed, and boards are hinged for easy maintenance.

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SPECIFICATIONS

CAMAC Model 8210

QUAD 10-BIT TRANSIENT DIGITIZER

Input Characteristics:

Number of Inputs:	1, 2 or 4, switch selectable.
Analog Input Impedance:	1 MΩ (50 Ω optional).
Full-Scale Amplitude Range:	±5 volts—10 volt range.
Input Analog 3 dB Bandwidth:	5 MHz.
Overvoltage Protection:	±65VDC, ±100V for 1sec, ±200V for 10msec.
Stop Trigger Input:	LEMO connector, TTL level required to terminate conversion cycle after preset number of samples.
Input Connectors:	Coaxial LEMO.
Input Coupling:	Direct.

Digitizing Sections:

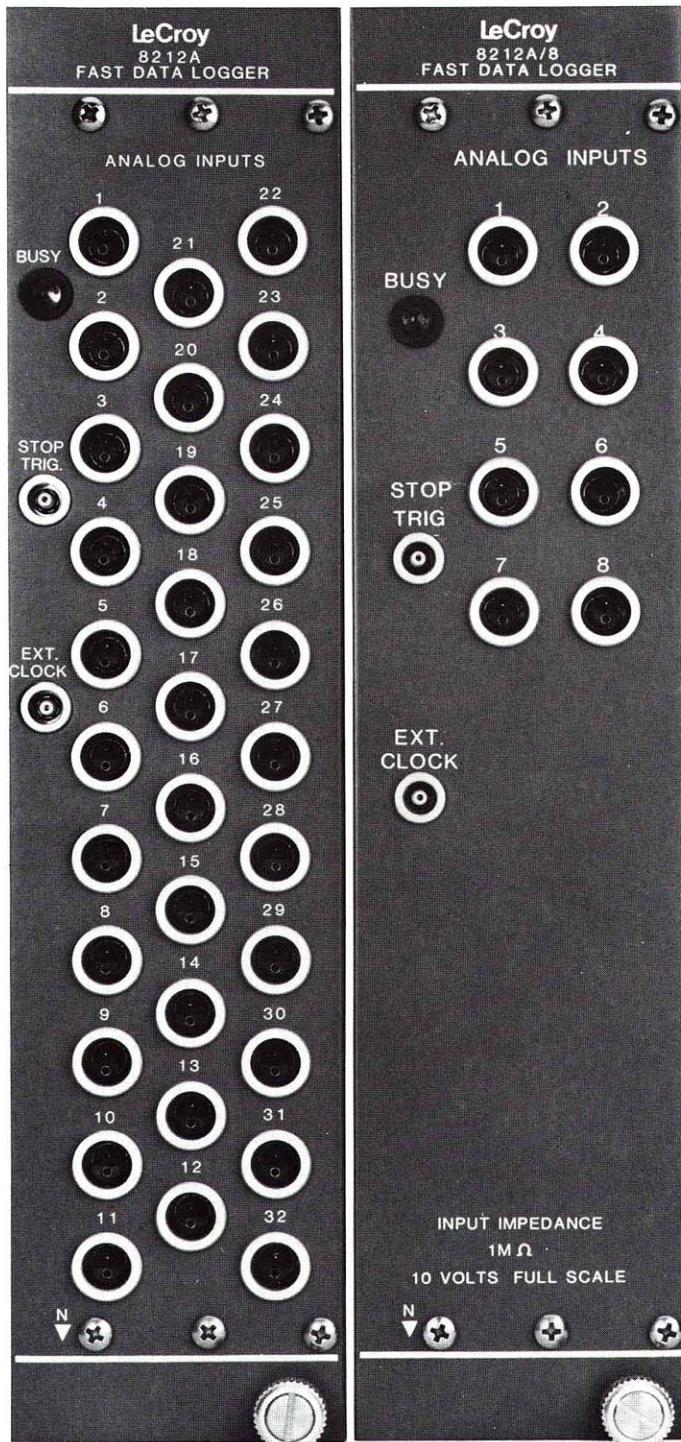
Internal Clock:	Front-panel switch selects rate: 1 MHz, 500 KHz, 250 KHz, 100 KHz, 50 KHz, 25 KHz, and 10 KHz, or EXT.
External Clock Input:	One coaxial LEMO-type connector (500Ω impedance, TTL level). Minimum duration of clock pulses, 100 nsec. Valid frequency range 0 to 1 MHz. Time varying frequencies allowed to achieve "importance" sampling along a single waveform.
Sensitivity:	9.8 mV/count.
Analog-to-Digital Conversion:	10 bits or 1 part in 1024.
Linearity:	±0.2% of full scale.
Aperture Uncertainty:	±100 psec maximum, defined as the uncertainty in the actual sample-taking time relative to the leading edge of the clock. This corresponds to a capability of frequency reconstruction of 1.5 MHz with 10-bit accuracy.
Channel-to-Channel Sampling Uncertainty:	≤ 5 nsec.
Memory Organization:	The memory is contained in separate modules which can be cascaded each capable of storing up to 32,768 10-bit words. (See further description of LeCroy Model 8800). Memory is divided equally among the active channels.
Display:	A built-in display driver allows the digitized waveform to be viewed on any real time oscilloscope. A channel select switch is located on the front panel.
Post Trigger Sampling:	The number of samples taken after the stop trigger is set by a front panel switch in multiples of 1K (2K optional).

Readout Characteristics:

Readout Scheme:	The standard CAMAC organization is used permitting readout at the maximum rate allowed by CAMAC unless 4 channels are active (2μsec/word). Word count and Q-switching DMA transfers are possible. Readout is non-destructive. Data from individual channels is accessible and the first word corresponds to the earliest sample taken. Readout is serial, but readout can be terminated for a given channel at any point.
CAMAC Commands:	<p>L: A Look-At-Me signal is generated at the end of the final sampling sequence.</p> <p>Q: A Q=1 response is generated in recognition of a F(2)•N only when a valid word is being read. After all data has been read for a given input channel, the next readout will generate a Q=0 response. The size of the memory, which depends upon the number of memory modules used, is programmed into the 8210 by a jumper option. Q=1 also returned on F(8) if internal LAM is on.</p> <p>Z: The continuous sampling cycle is reinitiated; requires S2.</p> <p>C: Same effect as Z.</p> <p>X: An X=1 (Command Accepted) response is generated when a valid F and N are generated.</p>
CAMAC Function Codes:	<p>F(1): Reads out front-panel switches (number of post-trigger samples, number of channels and internal clock frequency).</p> <p>F(2): Read data registers; requires N. Successive F(2)•N commands will read successive 10-bit words from memory.</p> <p>F(8): Test for LAM.</p> <p>F(9): Initialize module.</p> <p>F(10): Clear LAM.</p> <p>F(16): Select channel to be read. F(16)•A(0) through A(3) selects channel 1–4 of the quad unit.</p> <p>F(24): Disable Look-At-Me (LAM); requires N • S2.</p> <p>F(25): Generates a "Stop Trigger."</p> <p>F(26): Enable LAM and stop DAC display. This command is necessary for any computer readout of the module. There may be as much as a 20 msec latency period (for 1 memory module) to allow the DAC to cycle through the rest of memory. (Caution: the state of the LAM mask, and hence the state of the display, may be arbitrary after turn-on.) No latency time if issued before stop trigger.</p>
Packaging:	In conformation with the CAMAC standard for nuclear instrumentation modules. (IEEE Standard 583, or European Esone Report #EUR4100e.) RF shielded CAMAC #3 module. Approximate current requirements are within CAMAC standards for a #3 width.
Power Requirements:	2.2 A at + 6 V 13 mA at – 6 V 490 mA at + 24 V 310 mA at – 24 V

TECHNICAL DATA

LeCroy



CAMAC Models 8212A and 8212A/8

High Accuracy Simultaneous Sampling Data Loggers

- **High density:** up to 32 inputs
- **Independent measurements:** Operates as if there were a separate ADC for each input
- **High sensitivity:** 12 bits, or 0.025% resolution
- **50 KHz bandwidth**
- **Full-scale range of either ± 5 V or 0 to 10 V**
- **Differential inputs:** Eliminate 50-60 cycle and other common mode noise
- **Up to 5 kHz simultaneous sampling:** 32 channels
- **100 kHz maximum sampling rate:** One active channel
- **Expandable memory:** Utilize 32K word Model 8800A Memory modules

The LeCroy Models 8212A and 8212A/8 are multi-input 12-bit ADC's intended for use with the LeCroy Model 8800A 32K word Memory module in low frequency transient monitoring applications. The Model 8212A contains 32 independent channels with simultaneous sampling speeds from 40 kHz to 0.2 kHz depending upon the number of active channels. The 8212A/8 contains 8 channels and supports sampling from 100 kHz to 0.5 kHz.

With both versions, the number of active inputs is programmable. As fewer inputs are used, available memory storage per channel and maximum achievable sampling rate are increased. This allows flexible reorganization of sampling and storage parameters for unique experimental situations.

Both digitizers offer full differential inputs which accept ± 5 V signals (or by factory modification, 10 V signals of

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either polarity). Common Mode rejection, better than 40 dB at 4 kHz and 66 dB under 500 Hz, eliminates noise which would otherwise disturb the 12-bit resolution.

Each input to the digitizers has a separate track-and-hold driven by a common clock, ensuring that all inputs are sampled simultaneously, minimizing aperture uncertainty and channel-to-channel phase shifts in the digitized waveforms.

The 8212A can be used in one of two modes. In a "Sweep-and-Log" mode the data logger continually samples all channels simultaneously. The analog signal level from each channel's independent track-and-hold is converted sequentially, each measurement requiring less than 6 μ sec dwell time. A complete scan of 32 inputs takes less than 200 μ sec. Digitizing is governed either by the internal clock or by clock cycles applied to an external clock input. The data is sequentially stored in

up to four Model 8800A 32K word Memory modules. Equal memory segments are automatically assigned to the programmed number of active channels. In this Sweep-and-Log mode, memory is continually overwritten retaining only the most recent conversions. An externally applied Stop Trigger or a CAMAC F(19) or F(25) will stop the digitizer and memory, either instantly or after a pre-programmed number of post-trigger conversions, thus capturing a digitized window of interest. A "Single Scan" mode allows one sample on each active input to be acquired under direct computer supervision for real-time control applications.

The Model 8212A is ideal for logging fast response thermocouple and strain gauge readings on tokamaks, mirror machines and other fusion devices, biomedical transducers, superconducting magnet currents, or other measurements where a computer-compatible high-resolution measurement of millisecond type transients is required.

SPECIFICATIONS CAMAC Models 8212A and 8212A/8 SIMULTANEOUS SAMPLING DATA LOGGERS

INPUT CHARACTERISTICS

Analog Inputs:

Active Inputs:

Bandwidth:

CMRR:

Cross Talk:

Overshoot Protection:

Protection:

ADC CHARACTERISTICS

Full-Scale Range:

Resolution:

Gain Accuracy:

Non-Linearity:

Conversion Time:

FRONT-PANEL CONTROLS

Busy:

Stop Trig:

Ext. Clock:

SAMPLING RATE

32 differential, Lemo connectors, direct coupled $1M\Omega$ input impedance.

The number of active inputs is programmable in binary steps. The number of active inputs can be programmed as either 4, 8, 16 or 32 for the 8212A, and 1, 2, 4 or 8 for the 8212A/8. 3 dB—50 kHz.

Common Mode Rejection Ratio: 66 dB (DC—500 Hz), greater than 40 dB at 5 kHz.

66 dB isolation or better between any two channels, from DC to 500 Hz, greater than 40 dB at 5 kHz.

± 140 V DC or 115 V rms at 60 Hz across: input pins, or either pin with respect to ground.

± 5 V full-scale. 0 to +10 V or 0 to -10 V full-scale is available as a factory installed option.

ADC resolution is 12 bits (0.025% of full scale with $\pm 1/2$ LSB relative accuracy).

Maximum channel-to-channel variation is $\pm 0.1\%$ and stable within $\pm 0.2\%$ over a 10°C to 40°C range.

Integral non-linearity $\pm 1/2$ LSB.

The output of the front end track-and-holds are converted sequentially. Total conversion time is approximately the number of active channels times 5.5 μ sec. During conversion, the data is presented to the memory port for transfer to LeCroy Model 8800A Memory modules.

LED lit indicates conversion is in progress.

Lemo connector, 510 Ω , TTL compatible, edge sensitive.

Lemo connector, 510 Ω , TTL compatible, edge sensitive.

Sampling is governed either by a fixed set of seven sampling frequencies available from internal clocking circuitry, an external clock input, or individual commands from the CAMAC dataway (see F(27)). The sampling frequencies in the table below are available under program control (see F(17) under CAMAC commands). Alternatively, an external clock can be supplied via a front-panel connector. Note that in certain instances higher sampling rates are achievable in the 8212A/8 by using an external clocking source, such as the LeCroy Model 8501.

Number of Active Inputs	8212A Internal Clock	8212A/8 Internal Clock	8212A or 8212A/8 External Clock
1	—	100 kHz	DC to 100 kHz
2	—	50 kHz	DC to 80 kHz
4	40 kHz	25 kHz	DC to 40 kHz
8	20 kHz	12.5, 5.0, 2.5, 0.5 kHz	DC to 20 kHz
16	10 kHz	—	DC to 10 kHz
32	5, 2, 1, 0.2 kHz	—	DC to 5 kHz

READOUT

Internal memory:

Before or during any scan, the 8212A may be switched to the Single Scan mode with a CAMAC F(19), which causes a LAM to be generated when conversion is complete. The internal memory may then be read at the maximum CAMAC rate.

External Memory:

After the stop-trigger and post-trigger samples, the 8212A automatically enters the data output mode. A single channel may be selected (see F(16) of CAMAC commands) where the time between reads is approximately 0.6 usec times the number of active channels. Q = 1 indicates a valid read, Q = 0 indicates data is being read too quickly. Alternatively, the Data Streaming mode may be used in which successive locations in memory are read at the maximum CAMAC rate with the data from all active channels interlaced.

OUTPUT PORT

TTL data levels; one 40-conductor cable (Model DC 8800); consists of 12 data lines, 12 ground, 7 control lines, and 7 grounds. Output is compatible with LeCroy Model 8800A 32K Memory module. Up to four Memory modules may be used with one 8212A.

CAMAC COMMANDS

L:

A LAM is generated at the end of the next conversion following the F(19) Single Scan command. A LAM is generated 7 μ sec following the final conversion after a stop-trigger and post-trigger scans. A LAM is also generated following the reading of external memory.

Z or C:

Resets into the Sweep-and-Log mode.

Q:

A Q = 1 response is generated for valid F(0), F(1), and F(2) reads and also for a test LAM, F(8), if the LAM is set. When F(2) readout is used, Q = 1 will be generated until the last word from the selected channel is read. The next read will generate a Q = 0 response, facilitating DMA transfers. The size of the available memory must be programmed by a switch, having been determined by the number of memory modules attached.

X:

An X = 1 (command accepted) response is generated when a valid F, N, and A command is applied.

F(0):

Read data from inputs 1-16; requires "A"; A(0) through A(15) are used for channel addresses.

F(1):

Read data from inputs 17-32; requires "A"; A(0) through A(15) are used for channel addresses.

F(2):

Read successive values from each channel onto the dataway; requires F(16). If input 33 is selected with F(16), initiating the Data Streaming mode, subsequent F(2)'s will read successive memory words (interlaced data) at up to the maximum CAMAC rate.

F(3):

Read function data back to computer. Same data written with F(17).

BIT PATTERN

CAMAC	Post-trigger Scans			Clock Frequency			Number of Channels	
	2^2	2^1	2^0	2^2	2^1	2^0	2^1	2^0
F(17)	W8	W7	W6	W5	W4	W3	W2	W1
F(3)	R8	R7	R6	R5	R4	R3	R2	R1

F(8):

Test LAM, Q response if a LAM is being generated, even if the CAMAC L line is disabled.

F(9):

Resets into the Sweep-and-Log mode.

F(10):

Reset LAM.

F(11):

Re-enable the Sweep-and-Log mode. Used only after the LAM generated by the F(19) Single Scan command. The data in external memory remains valid unlike the result of C, Z, and F(9) resets.

F(16):

Load data from write lines into channel select memory. Used to select a single channel and have the data read from it in chronological order. Values of n-1 select channel number n.

Writes function data into module (see F(3)).

F(17):

Enables the Single-Scan mode, causing a LAM at the end of the next scan. F(0) and F(1) reads are then valid.

F(24):

Disable the CAMAC L line. LAM's can still be detected using F(8).

F(25):

Generates a Stop Trigger.

F(26):

Enable LAM.

F(27):

When the external clock is enabled, instead of using an external clock, a single clock pulse can be generated using F(27) and S2.

GENERAL

Packaging:

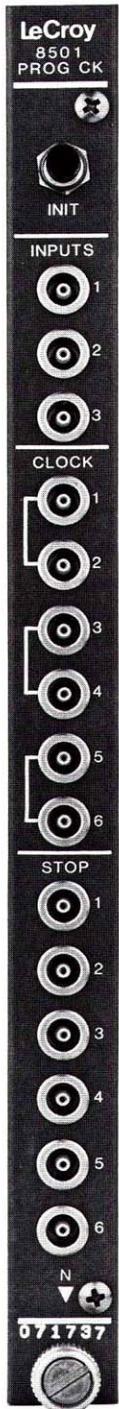
In conformance with CAMAC standard for nuclear modules European ESONE Committee Report EUR4100e or IEEE standard #583). RF-shielded CAMAC #3 module.

Power Requirements:

1 A at + 6 V	325 mA at - 6 V
310 mA at + 24 V	240 mA at - 24 V

TECHNICAL DATA

LeCroy



CAMAC Model 8501 Programmable 3-Speed Clock Generator

- Multi-speed, multi-mode clocking
- High fanout capability — up to 6 parallel clock outputs
- Triggerable Clock Bursts
- Interleaving mode — use two transient recorders at twice the maximum sample rate
- Total CAMAC programmability — set frequencies and number of samples and enable operational modes

The LeCroy Model 8501 is intended to provide a sequence of clocking pulses for use with the LeCroy series of CAMAC transient recorders, or for other applications requiring an accurate flexible clock generator. The unit is fully programmable, or it can be switched from one frequency to another by an external pulse. To further optimize the use of the memory in the transient recorders, a burst mode allows the recording of multiple records smaller in size than the memory. Again, the size of the burst and the speed of the sampling can be programmed.

The unit also functions as a 2-phase clock, allowing two transient recorders to be used as a single system at double the maximum sampling rate. This solution is often more cost-effective than a transient recorder with twice the speed while permitting a reuse of the component units as separate channels at slower speeds.

A front-panel pushbutton allows initialization of the sampling sequence without resort to the computer. In multi-speed modes the first external trigger to the clock module will switch the output to the second programmed frequency and produce clock pulses until a change is initiated by a second external trigger or a preset number of samples, at which point the clock rate changes to the third frequency and takes the final set of samples. The number of samples taken and their frequencies can all be set and read by standard CAMAC function commands.

The LeCroy Model 8501 allows the programming of a CAMAC crate full of transient recorders. The sequences of clock frequencies and stop triggers can be fanned out to six transient recorders. The number of transient recorders driven can be further increased by fan-out techniques external to the 8501 to provide a master clocking circuit for an entire transient-recorder-based data acquisition system.

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SPECIFICATIONS CAMAC MODEL 8501 PROGRAMMABLE THREE-SPEED CLOCK GENERATOR

MODES

- I. **Presettable Frequency Shift:** Three programmable frequencies with presettable control counter. Upon initiation of a cycle by either the front-panel Initiate pushbutton or by CAMAC command, clock pulses are output at frequency f_1 . Receipt of a rising signal at the Input #2 connector shifts the clock to f_2 . After the number of clock pulses preset for f_2 , the frequency shifts to f_3 . After the programmed number of pulses at f_3 , the unit outputs a positive-going Stop pulse and issues a LAM. f_3 continues until an Initiate signal is received.
The maximum number of clock pulses at f_2 is 64k. The maximum number at f_3 prior to output of a Stop pulse is also 64k. No minimum for either.
In a transient recorder the number of samples taken at each of the three frequencies can be preset using Mode I:
 - f_2 Number of samples at f_2 = number of clock pulses programmed for f_2 .
 - f_3 Number of samples at f_3 = number of clock pulses programmed for f_3 plus the number of post trigger samples the transient recorder is set for (with the Stop output from the Model 8501 used as the Stop trigger for the transient recorder).
 - f_1 Number of samples at f_1 = transient recorder memory length minus the number of samples at f_2 and at f_3 .
- II. **Triggerable Frequency Shift:** Three programmable frequencies with external control trigger inputs. Here, as in Mode I, f_1 clock pulses appear when the cycle is initiated. Upon receipt of a rising signal at the Input #1 front panel connector, the frequency shifts to f_2 , but unlike Mode I, remains there until receipt of a rising signal on the Input #2 connector, at which time the frequency shifts to f_3 and remains until the next sequence is initiated. A rising signal on the Input #3 connector during f_3 generates a Stop pulse for use as a Stop Trigger to a transient recorder. Two sixteen-bit counters keep a tally of the number of pulses at f_2 and at f_3 (before the Stop pulse) and can be read via the CAMAC bus. A LAM is issued on Stop out and/or if either counter overflows.
- III. **Interleaved Clock:** The 8501 outputs a single presettable frequency (f_1) from its 6 clock output connectors; however, the signals on each pair of connectors are shifted from each other by $\frac{1}{2}$ clock period. This allows interleaved samples to be taken by two transient recorders.
- IV. **Burst:** A burst of clock pulses is issued each time a rising signal is applied to the Input #2 connector. Frequency (f_2) and burst length are programmable. Maximum burst length is 64k clock pulses. No minimum. A stop trigger output is issued at the end of each burst. A burst can be terminated early by the front-panel Initiate button or by an F(25) command.

STOP (TRIGGER) OUTPUTS

The Stop outputs are provided primarily to supply stop trigger inputs to transient recorders which are using the 8501 clocks. The six outputs are all in phase TTL level signals capable of driving 50Ω terminated lines.

Mode I : Stop trigger is issued when the counter for clock frequency f_3 reaches the programmed number.

Mode II : Signal at Control Input #3 generates stop trigger. (Must be preceded by control #1 and #2 in sequence).

Mode III: No stop trigger is issued.

Mode IV: Stop trigger issued at end of each burst.

CLOCK FREQUENCY

20Hz to 20MHz in two ranges:
200Hz — 20 MHz (Hi range) 20Hz — 2.0 MHz (Lo range)
 f_1 , f_2 , f_3 must all be within same range. Frequency steps are 1, 2, 5 sequence.

CLOCK OUTPUTS

Accuracy 0.01%. Six clock outputs, each capable of driving a 50Ω terminated line. All outputs are in phase, except in mode III, where outputs 2, 4, and 6 are shifted $\frac{1}{2}$ clock period from outputs 1, 3, and 5, to allow double-rate sampling using pairs of transient recorders. All clock signals in all modes are 50% duty cycle, TTL level, crystal-controlled.

(CONTROL) INPUTS

General:

Impedance:	1.5k Ω
Trigger Level:	TTL or NIM (jumper option)
Overvoltage Protection:	± 15 volts DC.
Input #1:	Low to high transition causes clock outputs to shift from f_1 to f_2 in modes I and II. No effect in other modes.
Input #2:	Low to high transition causes clock outputs to shift from f_2 to f_3 in mode II; initiates clock pulse burst in mode IV. No effect in other modes.
Input #3:	Low to high transition causes low to high transition on Stop outputs in Mode II (after signal has been received at Inputs #1 and #2). No effect in other modes.

READOUT CHARACTERISTICS

CAMAC Commands: Z or C or F(9): Reinitiates continuous sampling cycle (Mode III). Requires S2. Also clears LAM register.
X: An X=1 (command accepted) response is generated when a valid N, F and A are present.

CAMAC Function Codes:

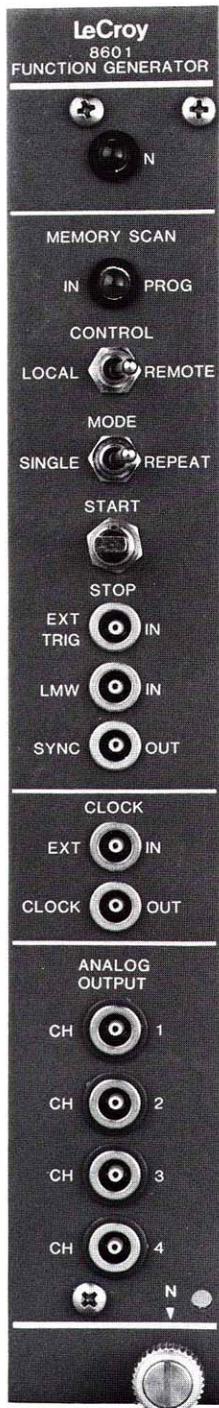
F(0)•A(0):	Reads the number of clock pulses at the second frequency (f_2) in Mode II. Returns Q = 1 only in Mode II and when Stop Out high.
F(0)•A(1):	Reads the number of clock pulses at f_3 in Mode II. Returns Q = 1 only in Mode II and when Stop Out high.
F(0)•A(2):	Reads the LAM register. Returns Q = 1 except in Mode III. R1 — Stop trig LAM. R2 — f_2 counter overflow. R3 — f_3 counter overflow.
F(8):	Test LAM. Q response is generated if LAM is set.
F(10):	Clear LAM.
F(10)•A(0):	Clear Stop Out LAM.
F(10)•A(1):	Clear f_2 counter overflow LAM (Mode II).
F(10)•A(2):	Clear f_3 counter overflow LAM (Mode II).
F(16)•A(0):	Writes the number of clock pulses at f_2 in Mode I and the number of burst pulses in Mode IV.
F(16)•A(1):	Writes the number of f_3 clock pulses preceding Stop Out (Mode I).
F(16)•A(2):	Selects the frequency range.
F(16)•A(3):	Sets frequencies f_1 , f_2 , f_3 .
F(24):	Disable LAM.
F(25):	Resets sequences. In Mode I, loads counters, enables and starts clock 1; resets control inputs. In Mode II, clears counters, enables clock 1, resets control inputs. No action in Mode 3. In Mode 4, loads counters, disables clock, resets control inputs.
F(26)•A(0):	Enables Mode 1.
F(26)•A(1):	Enables Mode 2.
F(26)•A(2):	Enables Mode 3.
F(26)•A(3):	Enables Mode 4.
F(26)•A(4):	Enables LAM.

CONNECTORS: All connectors are coaxial LEMO type.

PACKAGING: In conformance with CAMAC standard (USAEC Reports #TID-25875, IEEE standard #583, European ESONE report #EUR4100e). RF-shielded CAMAC #1 module.

APPROXIMATE POWER REQUIREMENTS: +6V at 1.25A -6V at 70mA

SPECIFICATIONS SUBJECT TO CHANGE



Model 8601

Quad Programmable Complex Function Generator

- High-speed, arbitrary-shape signal generation
- Large dynamic range (programmable transition of 20 μ V to 20 V)
- Up to 1 M Ω stored transitions (memory words)
- Four separate output channels
- Fast setting time (7 μ sec, full scale change)
- De-glitched outputs
- Real-time computer control of amplitude, offset and clock rate
- Pre-programmed control of amplitude, offset and clock rate
- Burst update mode for multiple channels
- Update rates to 1 MHz
- Power-up to zero volts output
- High output drive capability
- Single-scan and repeat modes

The LeCroy Model 8601 Complex Function Generator is a 4 channel 10-bit digital-to-analog converter (DAC) which uses the data stored in companion LeCroy memory modules to generate waveforms under the control of an internal or external clock. The Model 8201A 16K, 16-bit Memory or the Model 8206A 64K, 16-bit Memory may be cascaded to provide memory lengths to 256K or 1 M Ω respectively. The CAMAC packaging of these units simplifies their use as the front end of a computer-based control or data acquisition system. Each channel is organized as a 1024-step bipolar signal within the programmable voltage amplitude range. This is summed with the programmable offset voltage to produce the desired output. The signal generated by the signal DAC is normally updated by the information stored in the companion memories but may be updated directly via computer. Direct programming of amplitude range, voltage offset, signal DAC, and clock frequency make possible real-time computer feedback modifications of the waveforms generated.

The four channels can be programmed to allow low frequency channels to use much less memory space than fast channels. Nearly simultaneous outputs from the four channels can be achieved, even at low clock frequencies, by a special multiword memory read feature ("Burst Mode"). The 1 MHz update rate and the \pm 12 V drive satisfy most control applications. Low drift and a predictable power-up sequence achieve reliable control operation.

These units find use in many different control applications where non-sinusoidal single scan or multiple scan functions are necessary. Designed for control of fusion reactor power supplies and accelerator magnet ramping, the general usefulness extends to many magnet control, voltage shaping or scanning, feedback control, or ATE applications.

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SPECIFICATIONS

Model 8601

QUAD PROGRAMMABLE COMPLEX FUNCTION GENERATOR

ANALOG OUTPUTS

Number:

Output Limits:

Linear Range:

Amplitude Full

Scale Ranges:

Amplitude Resolution:

Linearity:

Offset Range:

Absolute Accuracy:

Setting Time:

Risetime:

Aberrations:

Delay Time:

Interchannel Cross Talk:

Power-up Mode:

Operating Temp. Range:

Output Protection:

External Memory:

Four de-glied outputs with Lemo connectors, one for each channel.

When selecting signal amplitude range and offset values, the combination of the two must be considered in order to remain in a linear range. The linear range of the output circuitry is from +12 V to -12 V into a high impedance. Therefore, if an amplitude range of 20 V (i.e. ±10 V) is desired, the offset must not exceed ±2 V. On the other hand, if an amplitude range of ±2 V is set, the offset may be programmed at any point between -10 V and +10 V. If the ±12 limit is exceeded, the output waveform will saturate.

+12 V to -12 V into a high (>10 kΩ) impedance. +6 V to -6 V into 50 Ω.

0 to 20 V (±10 V) in 20 mV steps (10-bit resolution) centered around the offset level. Example: ±5 V range, +1 V offset, is range from +6 V to -4 V. Programmable. F(16).

One part in 1024 (10-bits) of amplitude range (Signal DAC). Programmable. F(18).

±½ LSB deviation from best straight line

+10 V to -10 V in steps of 20 mV (10-bit resolution). Programmable F(17).

±0.1% at 20 V amplitude full scale range, OV offset and 25°C. Plus ±20 mV at other full scale ranges; ±20 mV at other offset values and ±10 mV/°C temperature coefficient

To within ±10 mV: 7 μsec for 20 V change; 6 μsec to 10 V; 5 μsec for 2 V.

2 μsec typical (10-90%).

Overshoot <3%; Maximum glitch 10 mV; Noise Level <15 mV p-p (1 Hz-1 MHz).

2.5 μsec typical (clock edge to one LSB change). Jitter, <50 nsec. Channel-to-channel variation <100 nsec.

<60 dB, transient; <80 dB, DC.

Upon power-up, output voltages are at 0 V.

10-50°C.

Will survive short circuit for at least 30 seconds. Series output 50 Ω resistor may be permanently damaged thereafter.

Compatible with Models 8201A and 8206A 16-bit Memory Modules. Lower 10 bits are interpreted as data for the Signal DAC and upper 2 bits as channel routing ('00' = Ch. 1, '01' = Ch. 2, '10' = Ch. 3, and '11' = Ch. 4). Multi-pin connector at rear of modules interconnects 8601 and memories.

MEMORY SCAN CONTROL

Local/Remote Switch:

"REMOTE" selects CAMAC control of Scan Mode and of Start/Stop.

Single/Repeat Switch:

Enables single or repetitive scans through companion 8801/12 memory (local mode only). Programmable (remote mode only). F(19)•A(0).

Start/Stop Switch:

3-position momentary switch initiates/terminates a memory scan (local mode only). Termination is normally at the end of the scan in progress. Internal jumper can change termination to immediate. A start command then causes the 8601 to resume at the next memory word in sequence. The scan could begin at the first memory word by reprogramming. Start/stop commands can be issued via computer. F(24)•A(1) and F(26)•A(1).

Initiates Memory Scan on positive-going TTL edge in local or remote mode. Programmable Disable/Enable. F(19)•A(0).

Positive-going pulse (TTL, 500 nsec) at beginning of memory scan.

Indicates memory scan is in progress.

Ext Trig In:

Input for last memory word (LMW) signal from companion memory module. Connection required for single scan mode, for Synch Out generation and for normal functioning of manual Stop.

Synch Out:

In Progress LED:

LMW In:

Indicates memory scan is in progress.

Burst Mode:

Permits multiple (1, 2, or 4) memory reads at 1 MHz rate for each Data Clock pulse. This feature provides for nearly simultaneous outputs in the 4 channels. F(19)•A(1).

Computer Clock:

Computer command acts as single data clock pulse. F(25).

FRONT PANEL "N" LED

DATA FORMAT

CAMAC CONTROLS

L:

A Look-At-Me (LAM) is generated at the end of a scan (single-scan-mode) if previously enabled by F(26)•A(0).

Q:

Q = 1 is generated in response to F(8) if LAM is set, or to F(27) if the unit is in Remote Mode. Otherwise Q = 0.

X:

X = 1 is generated in response to all valid F and A codes.

Z or C:

Resets all status bits to 0, and gain and signal DAC's to zero. Resets offset to zero volts and terminates scan.

CAMAC FUNCTIONS

F(6):

Read Module Identifier. Returns the number 601 in binary code in R1-R10.

F(8):

Test LAM. Generate Q = 1 response if LAM is active, whether or not LAM is enabled.

F(9):

Resets module. Equivalent to Z or C.

F(10):

Resets LAM.

F(16)•A(N):

Determines signal full scale of Channel N + 1 (N≤3). 10-bit word in W1-W10 provides full scales in the range of ±10 V to ±10 V in steps of 20 mV.

F(17)•A(N):

Determines voltage offset of Channel N + 1 (N≤3). 10-bit word in W1-W10 provides offsets between ±10 V.

F(18)•A(N):

Writes directly into Signal DAC register of Channel N + 1 (N≤3). 10-bit word in W1-W10 provides output between ±Full Scale.

F(19)•A(0):

Data remains valid until overwritten from memory or from CAMAC dataway.

F(19)•A(1):

Set Scan and Trigger Mode. W1 = 0/1 Selects Repeat or Single Scan Mode. W2 = 0/1 Disables or Enables External Trigger.

F(19)•A(2):

Set Clock Source and Range, and Burst Mode. W1 = 0/1 Selects Internal or External Data Clock Source. W2 = 0/1 Selects 1 kHz or MHz Master Clock. W3, W4 sets burst length.

F(24)•A(0):

Set Data Clock period. 16-bit word in W1-W16 multiplies Master Clock period (1 msec/1 μsec) to determine Data Clock period.

F(24)•A(1):

Ranges are 1 μsec to 64 msec in 1 μsec steps and 1 msec to 64 sec in 1 msec steps.

F(25):

Disable LAM.

F(26)•A(0):

Stop Memory Scan (Remote Mode only).

F(26)•A(1):

Equivalent to Data Clock at S1 time.

F(27):

Enable LAM.

GENERAL

Start Memory Scan (Remote Mode Only).

Packaging:

Test Local/Remote status (Q = 1 returned in Remote Mode).

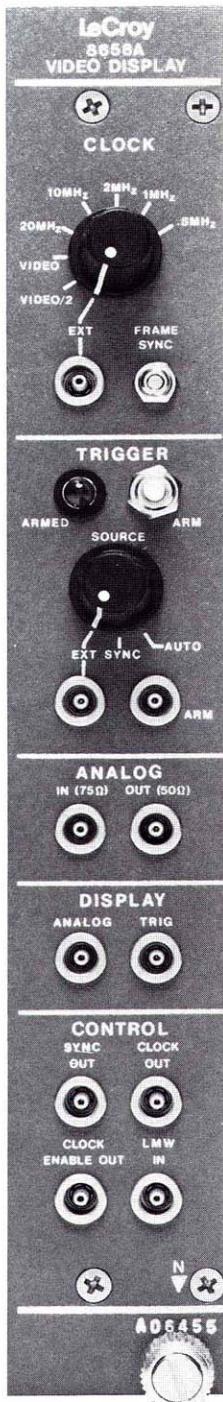
Power Requirements:

In conformance with the CAMAC standard (IEEE #583, ESONE Report #EUR4100e, EUR 46003). RF-shielded #2 width module.

1.1 A at +6 V; 0.8 A at +24 V; 0.7 A at -24 V.

TECHNICAL DATA

LeCroy



CAMAC Model 8658A Video Digitizer Display Module

- Permits display of full frames of digital video
- Synchronizes acquisition and display of video
- Permits display of up to one million samples

The LeCroy Model 8658A is a companion module to the TR8857A Video Digitizer System. The module provides a crystal-based data-taking clock at switch selectable rates including the appropriate frequency to exactly fill the available memory with one field or one frame of video data (European* format also available). The triggering circuit synchronizes the start of data taking with the beginning of a video frame, an external trigger, a front-panel pushbutton, or a computer command.

The data stored in the TR8857A system is accessed and displayed in analog form by the 8658A module. For video signals, it is assumed that the synchronization information is digitized. Then the display output will drive a standard TV monitor (European or American). Otherwise the display trigger out facilitates viewing of analog signal on a standard oscilloscope.

The Model 8658A together with the TR8857A Digitizer and an optional number of MM8306A memory modules (2, 4, 6 . . . 16) in increments of 128K samples each provides a fast high resolution stand-alone "frame grabber" video record and display system. It may be interfaced to any of the standard available computers through an off-the-shelf CAMAC interface/controller.

*Specify 8658A MOD 100 for PAL format—625 line, 50 Hz field.

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SPECIFICATIONS

CAMAC Model 8658A

VIDEO DIGITIZER DISPLAY MODULE

ANALOG CHARACTERISTICS

Input Signal Range: 1.4 V p-p into 75 Ω impedance (50 Ω optional). Lemo connector.
Output Signal Range: Maximum 512 mV p-p into 50 Ω. Compatible with TR8857A.

CLOCK CHARACTERISTICS

Internal: Crystal controlled 0.5, 1, 2, 10 and 20 MHz. Video rate (1 field per 128K memory). Video/2 Rate (1 frame per 128K memory). NTSC (USA) or PAL (European) frequencies available.
External: TTL level pulse, rising edge triggers. Maximum rate 20 MHz, minimum rate 500 kHz. 50 Ω impedance.
Frequency sync: Front-panel potentiometer permits fine adjustment of the overall video frame playback rate in order to synchronize playback for most video monitors.

TRIGGER CHARACTERISTICS

Arming: Trigger must be armed to fire. Trigger arming is possible via computer control (CAMAC), manually or via a front-panel ARM input (100 Ω input impedance, TTL positive-going pulse 100 nsec duration required). An LED is lit when the trigger is armed.
Source: The trigger source is selectable via a front-panel rotary switch as follows:
EXT: External 50 Ω Lemo connector accepts TTL, 100 nsec minimum duration pulses.
SYNC: Internal pick-off triggers on the composite video vertical frame sync pulse.
AUTO: Triggers directly from the ARM command.

DISPLAY CHARACTERISTICS

Analog: Reconstructed analog signal. Analog (Display) is suitable for input to a scope for non-video viewing. If the original input includes sync pulses (composite video), it can also be used as an input to a video monitor. Drives approximately 1.5 V p-p into 75 Ω.

Trigger: TTL output pulse to trigger high-impedance scope in non-video display applications.

CONTROL CHARACTERISTICS (or compatible with TR8857A)

Sync Out: TTL output level during horizontal and vertical synchronization intervals of Analog (Video) Input signal, used to set sync (9th) bit in digitizing system.
Clock: The internal or external clock generated by the Model 8658A is fed through this connector.
Clock Enable: As soon as the trigger fires (after arming) this signal clamps high and enables the digitizer until the memory is full, at which time the last memory word (LMW) pulse is returned from the digitizer, resetting the Enable state.
LMW: Accepts TTL input pulse from digitizer, indicating last memory word has been accessed.

CAMAC COMMANDS

Z or C: Disables trigger and enable display.
Q or X: An X = 1 response (1) is generated for a valid F and N.

FUNCTION CODES

F(1): Read Clock and Trigger Source switch register.
F(9): Arm the trigger.
F(17): Display re-enable command.
F(25): Provides a trigger event via CAMAC.

MODULE INTERCONNECTIONS

Front Panel: Five Lemo-to-Lemo connectors between the 8658A and the TR8857A.
Rear Panel: 9-bit data word plus read-out clock is transferred via 20-conductor flat cable between 8658A and TR8857A External Port.

GENERAL

Packaging: In conformance with CAMAC standard for nuclear modules (IEEE Report #583, or European ESONE Reports #EUR4100e, EUR46003). RF-shielded CAMAC #2 module.
Power Requirements: 40 mA at + 24 V
600 mA at + 6 V
500 mA at - 6 V

SPECIFICATIONS SUBJECT TO CHANGE

TECHNICAL DATA

LeCroy



CAMAC Model 8800A Memory Module

The Model 8800A is designed to provide data storage for a wide variety of LeCroy instruments, including transient recorders, video digitizers, and fast data loggers. Each module has a capacity for 32K 12-bit data words and modules may be cascaded to provide record lengths to 256K words.

All read and write operations to the 8800A are controlled by the companion digitizer. Data from the digitizer is sequentially stored as acquired; if the controlling unit has more than one channel, the total of all cascaded memory is divided equally among the active channels. During readout to the CAMAC dataway, the memory contents are reconstructed so that each channel's data is in contiguous time sequence.

Readout is nondestructive and the memory is protected against write operations from the CAMAC dataway; it can only be written from the companion digitizer.

The Model 8800A Memory module is compatible with the following LeCroy digitizers:

Model 2264	8 channel, 0.5 MHz 8-bit Waveform Digitizer
Model 8210	4 channel, 1 MHz 10-bit Waveform Digitizer
Model 8212A	32 channel, 0.5-40 kHz, 12-bit Data Logger
Model 8212A/8	8 channel, 12.5-100 kHz, 12-bit Data Logger

SPECIFICATIONS

CAMAC Model 8800A

MEMORY MODULE

Inputs:	TTL Levels. Lines: 12 data, 12 grounds; 7 control lines, 7 grounds. One 40-conductor edge connector located at the upper rear of the module. Mates with LeCroy Model DC8800/n Data Cable (where "n" equals the number of memory modules linked to one data acquisition device).												
Memory Active Light:	Front-panel LED indicates when memory is being loaded or read.												
Memory Size:	32,768 words, 12 bits.												
Memory Expansion:	Serial organization permits adding the Model 8800A modules in a daisy-chained fashion with the maximum memory size dictated by the control board of the ADC module. Memory size must be internally specified on the control board of the "front end" ADC (jumper option) and on the memory modules (onboard Programming Switch). The LeCroy Models 2264 and 8210 can drive three modules, and Model 8212A can drive four modules with larger memory extention possible as a factory option.												
Packaging:	In conformance with the international CAMAC standard for nuclear modules (European ESONE Report #EUR4100 or U.S. IEEE Report #583). RF-shielded CAMAC #1 module.												
Power Supplies:	The Model 8800A Series can draw + 12 V from the + 12 V CAMAC bus or can be jumpered internally to use a built-in + 24 to + 12 V converter. Since the memory is not read directly, it can be located in an adjacent power crate (<4 feet of cable) with only + 12, + 6 V power.												
Power Consumption:	<table><thead><tr><th>Voltage</th><th>Current</th><th>Power</th></tr></thead><tbody><tr><td>+ 12 V (or + 24 V)</td><td>490 mA</td><td>5.9 W (11.8 W)</td></tr><tr><td>+ 6 V</td><td>650 mA</td><td>3.9 W</td></tr><tr><td>- 6 V</td><td>30 mA</td><td>0.2 W</td></tr></tbody></table>	Voltage	Current	Power	+ 12 V (or + 24 V)	490 mA	5.9 W (11.8 W)	+ 6 V	650 mA	3.9 W	- 6 V	30 mA	0.2 W
Voltage	Current	Power											
+ 12 V (or + 24 V)	490 mA	5.9 W (11.8 W)											
+ 6 V	650 mA	3.9 W											
- 6 V	30 mA	0.2 W											
Total Power Dissipated:	10 W (+ 12 V), 15.9 W (+ 24 V)												

SPECIFICATIONS SUBJECT TO CHANGE

TECHNICAL DATA

LeCroy



Model 8901 CAMAC to GPIB Interface*

- Allows GPIB users access to the wide range of inexpensive instrumentation available from LeCroy and dozens of other CAMAC manufacturers.
- Converts up to 23 individual instruments in a CAMAC crate into standard Listeners and Talkers on a GPIB while using up only one of the 15-device capacity of the GPIB.
- Block Transfer Mode. The 8901 can be programmed to transmit all data from a CAMAC module upon receipt of a single talk command.
- High-speed operation. Data transfer rates of several hundred megabytes may be achieved.

Simple program instructions via the GPIB to registers in the Model 8901 select an individual instrument module within the CAMAC crate, select any sub-address within that module, and establish the function (read, write, control). This allows the user to handle the entire CAMAC crate of up to 23 individual instrument modules in the same manner as any ordinary single device connected to the IEEE 488 bus. It is possible to interconnect up to 15 different CAMAC crates in this way.

The cost of a CAMAC crate (housing, power supply and internal digital bus) approximately equals the usual packaging cost of a single stand-alone instrument. As a result, the economic advantage of buying one GPIB interface and CAMAC crate for up to 23 individual instruments is substantial.

The 8901 can be programmed to transfer all data within a CAMAC module to a GPIB Listener without additional intermediate commands. In this high-speed data transfer mode, the 8901 will alternately transfer one, two or three 8-bit bytes (as programmed) as fast as the Listener can accept them, and then initiate a new CAMAC acquisition cycle. Time required for this procedure is approximately 2 μ sec.

As the list of computer, programmable calculator and intelligent terminal manufacturers offering the GPIB grows, so do the inherent advantages of uniting the GPIB and CAMAC concepts. The combination enhances the flexibility of both standards, decreases per-channel cost and retains most performance characteristics of each.

*CAMAC Computer Automated Measurement and Control (IEEE Std. 583-1975).

*GPIB General Purpose Interface Bus (IEEE Std. 488-1975)

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SPECIFICATIONS

CAMAC Model 8901

CAMAC TO GPIB INTERFACE

LOADING THE INTERNAL REGISTERS

Registers in the crate controller are sequentially loaded with data after the crate controller has been commanded to enter the listen mode by the GPIB System Controller. These registers store all the information necessary (N, A, F, W, C, Z, I) to generate standard CAMAC cycles.

The first byte received by the crate controller after it has entered the Listen mode contains the F code or control information.

The second byte accepted by the crate controller is a CAMAC subaddress (A Code). This is followed by a CAMAC station number (N Code) and three bytes of data for the CAMAC write lines.

Once these registers have been loaded, the information will be retained until modified or power is turned off. The GPIB system controller must issue a Listen command in order to initiate this loading procedure. The loading process can be terminated after any number of bytes have been transferred by commanding the crate controller to enter the Talk mode, by issuing an IFC command, or by issuing an Unlisten command.

INITIATING CAMAC CYCLES

A CAMAC cycle is executed every time the crate controller is commanded to enter the Talk mode and a Service Request is not pending. At the completion of the CAMAC cycle, the crate controller asserts the signal DAV notifying all GPIB Listeners that data is ready to be read. Every time a byte is accepted by the Listener, the crate controller makes a new byte available.

CLEAR, INITIALIZE, and INHIBIT

The 8901 can be programmed to generate clear (C), initialize (Z), or inhibit (I) signals on the dataway when a CAMAC cycle is executed. The C and Z registers are cleared after the completion of each CAMAC cycle. In other words, the clear and initialize signals will be turned on only during the first CAMAC cycle executed after the C and Z registers have been set under program control. Once the inhibit register is set, it will remain set until it is programmed off.

HIGH SPEED DATA TRANSFER MODE

The 8901 can be programmed for a high speed data transfer mode. In this mode, the first CAMAC cycle is initiated by commanding the Crate Controller to be a Talker. After the GPIB controller reads one, two, or three bytes of data from the Crate Controller, another CAMAC cycle is automatically initiated. Approximately 2 μ sec later, new data is available to be read. CAMAC cycles will continue to be executed until a Q = O condition causes the 8901 to stop executing CAMAC cycles and exit the high speed data transfer mode.

If the 8901 was programmed for the two, three, four-word return a new CAMAC cycle will be initiated after one, two, or three bytes of data are read, respectively.

Each time the 8901 exits from the high speed data transfer mode, it must again be programmed for a two, three, or four-word return.

SERVICE REQUESTS

There are three conditions which can cause the 8901 to issue a service request to the GPIB controller.

- 1) Whenever a LAM is set by a CAMAC module.
- 2) Whenever a CAMAC cycle is executed and a Q = O response is detected.
- 3) Whenever a CAMAC cycle is executed and a X = O response is detected.

SERIAL POLL

When the 8901 is polled, it sends one status byte to the controller. A service request by the 8901 will be terminated after the controller reads the status byte. However, if the service request was caused by a LAM, unless the LAM is cleared or the LAM Enable is disabled in the 8901 before the poll is taken another service request will immediately be issued.

FRONT PANEL FUNCTIONS

CLEAR:

Manual pushbutton for initializing data and state registers in all CAMAC modules.

TALK:

Lights when 8901 is a Talker

LISTEN:

Lights when 8901 is a Listener

X:

Lights when a command accepted signal is generated within the CAMAC crate

Q:

Lights when a Data Valid signal is generated within the CAMAC crate

ENABLE:

Lights when 8901 is enabled to carry out service requests

LAM:

Lights when any CAMAC module sets "Look-at-me", a service request

INHIBIT:

Lights when CAMAC dataway is inhibited

GENERAL

The Model 8901 resides in slots 24 and 25 in a CAMAC crate and generates all CAMAC dataway signals in response to commands from a GPIB controller. A standard GPIB connector on the front panel of the Model 8901 permits easy interconnection to any GPIB system. A GPIB controller can read 24 bits of data from the dataway Read lines (8 bits a time) and can also monitor the status of 23 LAM signals. The Model 8901 can be programmed to generate service requests to a GPIB controller if a LAM is set, a no X response, or a no Q response is detected.

Packaging:

In conformance with CAMAC Standard, RF shielded #2 module.

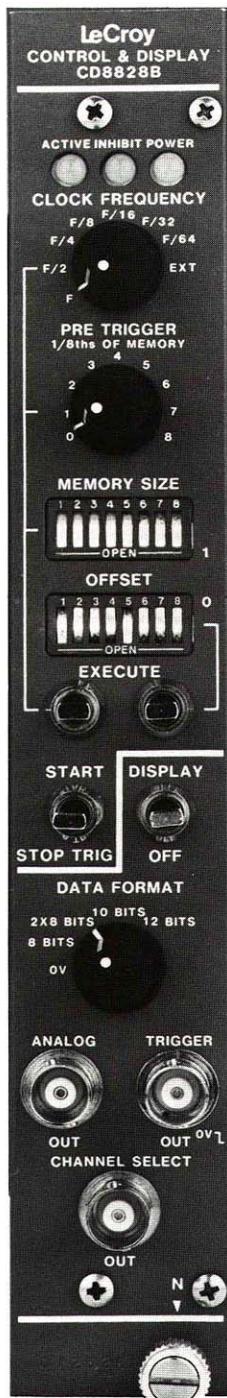
Power Requirements:

1.2 A at + 6 V

SPECIFICATIONS SUBJECT TO CHANGE

TECHNICAL DATA

LeCroy



Model CD8828B Control and Display Module

- Ideally suited for computer independent instrument operation. No programming is required
- Permits manual control of transient recorders without expensive and bulky controls on each instrument
- Reconstructs stored waveform data for viewing on any oscilloscope
- Compatible with the following digitizers:
 - Model TR8837F, 32 megasample/sec
 - Model TR8818, 100 megasample/sec
 - Model TR8828B, 200 megasample/sec
- May be operated with or without a controller in the crate

The LeCroy Model CD8828B provides optional manual control and display capabilities for the Models TR8837F, TR8818, and TR8828B Transient Recorders. Designed to be operated in the same CAMAC crate as the digitizers, it permits local setup of module parameters, generation of acquisition control signals, and display of stored waveform on an external oscilloscope.

The CD8828B may occupy any two normal stations in the crate and operates independently of any crate controller such as the LeCroy Model 8901 GPIB Interface. When both controllers are present, the CD8828B's actions can be inhibited under program control to assure that the dataway is available for externally generated CAMAC operation.

Any digitizer in the crate can be associated with the Control and Display Module by means of a coaxial cable installed between the units. Front-panel controls on the CD8828B may then be used to determine memory size, sampling rate, input offset, and pretrigger sampling as well as manually generating digitizer START and STOP Trigger commands. Depressing the Display Control automatically retrieves stored data from the selected digitizer and presents it, in reconstructed analog form, for viewing on any conventional oscilloscope. The display is maintained until it is switched off or the digitizer is restarted.

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SPECIFICATIONS

Model CD8828B

MANUAL CONTROL AND DISPLAY MODULE

GENERAL OPERATION

To set the sampling parameters of, to control, or to display data from any of the supported transient recorders, the transient recorder must have the CD SELECT input connected to the SELECT output on the control and display unit.

- Setup:** The desired sampling parameters are entered using front-panel rotary and dip switches. These parameters are then sent via the CAMAC dataway to the instrument when the appropriate EXECUTE switch is toggled.
- Control:** The unit may also be started and triggered by using the START/STOP TRIGGER SWITCH.
- Display:** To display data from a transient recorder, the correct data format is selected using the DATA FORMAT rotary switch and then DISPLAY ON is depressed. The CD8828B then retrieves the data from the connected/selected transient recorder for display.

FRONT-PANEL INDICATORS AND CONTROLS

- ACTIVE:** LED is lit when unit is using the CAMAC data bus for transferring data/commands.
- INHIBIT:** LED is lit to indicate that the unit is inhibited, that is, no front-panel operations will permit bus operations. See F(24)•A(1) and F(26)•A(1) under CAMAC commands.
- Power:** LED is lit when the correct operational voltages are supplied to the CD8828B. Will not necessarily indicate overvoltages.
- CLOCK FREQUENCY:** Rotary switch sets the sampling interval for the supported transient recorders. The selection is made in fractions of the master oscillator. For example, if the switch is set to F/2 for the TR8837F 32 MHz transient recorder, the sampling rate will be 16 MHz. The value selection must be succeeded by an EXECUTE to actually load the value into the transient recorder.
- PRE TRIGGER:** Rotary switch sets the pretrigger record length in eighths of the total record length. The value selection must be succeeded by an EXECUTE to actually load the value into the transient recorder.
- MEM SIZE:** Dip switches. Data entered using dip switches d1-d8 correspond to data written to the transient recorders on the CAMAC W9-W14 lines using an F(16)•A(0). The table below gives some of the dip switch settings which must be set to achieve the corresponding memory size, for the supported transient recorders.

d1-d8	TR8837F	TR8818	TR8828B
00000000	1K	8K	16K
00000001	2K	16K	32K
00000010	3K	24K	48K
00000011	4K	32K	64K
00000100	5K	40K	80K
00000101	6K	48K	96K
00000110	7K	56K	112K
00000111	8K	64K	128K
00001000	—	72K	144K
00001001	—	80K	160K
•	—	•	•
•	—	•	512K maximum
•	—	•	
11111111	—	512K	

- OFFSET:** Dip switches. The ± 256 mV offset of the transient recorders is settable using these 8 dip switches. The 8 bits of the dip switch settings d1-d8 correspond to the 8 bits which are written into the instrumentation modules using F(19)•A(0). OFFSET is not used for the TR8837, which does not have programmable offset. The table below gives some of the dip switch settings and the corresponding offset value that will be set when EXECUTE is performed.

d1-d8	approximate offset
00000000	-256 mV
00011100	-200 mV
01001110	-100 mV
10000000	0 mV
10110010	+100 mV
11100100	+200 mV
11111111	+256 mV

- EXECUTE:** Two single throw switches. Used to enter the selected sampling parameters into the connected transient recorder. Throwing left switch upward enters the CLOCK FREQUENCY, PRE TRIGGER and MEM SIZE. Throwing right switch upwards enters the OFFSET value.
- START/STOP TRIGGER:** Double throw switch. Upward deflection starts selected transient recorder. Downward deflection supplies a stop trigger to the selected digitizer.
- DATA FORMAT:** Rotary Switch, selects the correct data decoding mode for the control and display unit. Is used to distinguish between different resolution and differently formatted transient recorder data. Set to 8 BITS for model TR8837F. Set to 2 \times 8 BITS for the TR8818 and TR8828B.
- ANALOG:** 0 to 2.5 V output, $Z = 50 \Omega$, drives oscilloscope.
- TRIGGER:** Positive TTL level 40 μ sec pulse—Synchronizes TR8837 display on leading edge—Synchronizes TR8818/TR8828B display on trailing edge—output precursor to first sample in record.
- SELECT:** Output, TTL. Must be connected to the CD SELECT input of the transient recorder which is going to have its sampling parameters modified or data viewed.
- PACKAGING:** In full mechanical conformance (only) with CAMAC standard for instrumentation modules (IEEE Standard 583, European ESONE Report #EUR4100e). In full electrical conformance when inhibited. RF shielded #2 module.

POWER CONSUMPTION

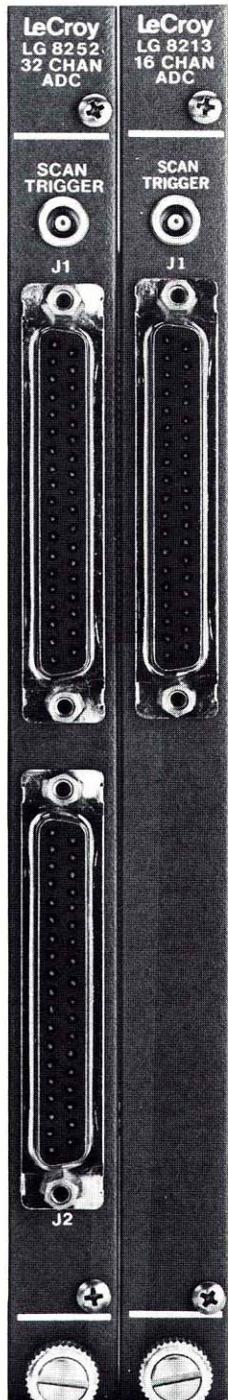
500 mA at + 6 V, 100 mA at + 24 V, 100 mA at - 24 V.

ORDERING INFORMATION

Specify the Model CD8828B. The model LE/BC-3 signal cable is supplied to allow interconnection between the CD SELECT input and the SELECT output of the CD8828B.

CAMAC COMMANDS

- Z,C Power-Up:** Places unit in inactive state, cancels inhibit.
- F(24)•A(1):** Inhibits unit—front panel operations will not generate CAMAC bus operations. This is a user strap selectable option.
- F(25)•A(1)** Same as Z,C or power-up.
- F(26)•A(1):** Clears inhibit.



Models LG8252 and LG8213

Fast Scan, 32 and 16 Channel Data Loggers

- **High Sensitivity:** 12 bits (0.025% Resolution)
- **Two Digitizing Modes:** Continuous Scan or Single Scan
- **Asynchronous Readout:** Any Channel can be read at any time
- **Bipolar or Unipolar operation over a 10 volt range**
- **Differential Inputs:** common mode noise rejection
- **Flexible Readout:** Block Transfer (DMA) or address selection
- **Sample and Hold Acquisition for high speed, high accuracy**

The LeCroy Model LG8252 is a 32-input ADC intended for use in general purpose voltage-monitoring applications. The Model LG8213 is a 16-channel version with identical characteristics unless otherwise noted. The $>10M\Omega$ inputs of the LG8232 respond to voltages over a 10-volt range, converting them to proportional 12-bit digital data words. An on-board switch provides the choice of a unipolar mode, 0 to + 10 volts, or a bipolar mode, -5 to + 5 volts. The differential inputs suppress common mode signals and noise.

The voltage levels at the 32 inputs on the front panel connectors are converted sequentially, requiring a maximum of 60 microseconds/channel for conversion and storage in random access memory. During readout the addressed 12-bit data word is placed on the Dataway without any interference with a store cycle, should one be present (asynchronous readout). In the Continuous Scan Mode each channel of the LG8232 continuously updates its memory every 2 ms (1 ms for the LG8213).

Random access readout over the CAMAC Dataway allows the flexibility of reading individual channels or subgroups of the 32 channels more frequently than others, permitting low maintenance items to be monitored compatibly with ones that demand a higher level of attention. Alternatively, a block transfer mode is incorporated which permits all channels to be read sequentially. Q = 0 is generated after the last channel is read in block transfer mode.

In the Single Scan Mode, either an input into the front-panel Scan Trigger or the CAMAC function F(25)•A(0) initializes the address to Channel 1 and starts a single scan of all channels. This mode thus permits all 32 measurements to be more clearly related in time to some external event or reference. LAM may be generated after the scan is completed.

SPECIFICATIONS

Models LG8252 and LG8213

FAST SCAN 32 AND 16 CHANNEL DATA LOGGERS

Analog Inputs:	32(16) differential voltage-sensing inputs; direct coupled; $>10\text{ M}\Omega$ impedance; front-panel connectors mate with LeCroy model CK2232 Connector Kit (2 required for LG8252).
Input Protection:	$\pm 300\text{V}$ for Transients ($\leq 100\mu\text{sec}$), $\pm 50\text{V}$ for dc.
Full-Scale Range:	Bipolar Mode – 5 to + 15 volts between minus and plus input (– 10 to + 10 volts jumper selectable). Unipolar Mode: 0 to + 10 volts between minus and plus input.
Common Mode Input Voltage Range:	$\pm 13\text{V}$.
Common Mode Rejection Ratio:	60 dB at 60 Hz.
Integral Non-linearity:	$\pm 1/2$ count ($\pm 0.012\%$ of full scale).
ADC Resolution:	12 bits ($\pm 0.025\%$ relative accuracy). Input source impedance of less than $50\text{ K}\Omega$ is required for 1 bit accuracy over full range.
Accuracy:	$\pm 2.4\text{ mV}$.
Temperature Coefficient:	Accuracy, 30 PPM/degree C, linearity 20 PPM/degree C.
Conversion Time:	$<60\mu\text{sec}$ per channel. Total scan time is approximately 2 msec. (1 msec for LG8213).
Operating Modes:	In the Continuous Scan Mode, continuously converted data is always available for readout. In the Single Scan Mode, the data acquired during a scan is available until a new scan is initiated. A scan may be initiated either by a Scan Trigger input or by an F(25)•A(0) CAMAC cycle.
Readout Time:	Readout may proceed at the fastest rate ($1\mu\text{sec}/\text{word}$) permitted by the CAMAC standard.
Data:	The proper CAMAC function and addressing scheme gates the 12 binary bits of the selected channel onto the R1 to R12 Dataway bus lines. The user may select either offset binary format or 2's complement format (sign bit is extended through R16).

CAMAC COMMANDS

Z and C: INITIALIZE and CLEAR both terminate scanning, reset and disable LAM, and enable continuous scan mode.

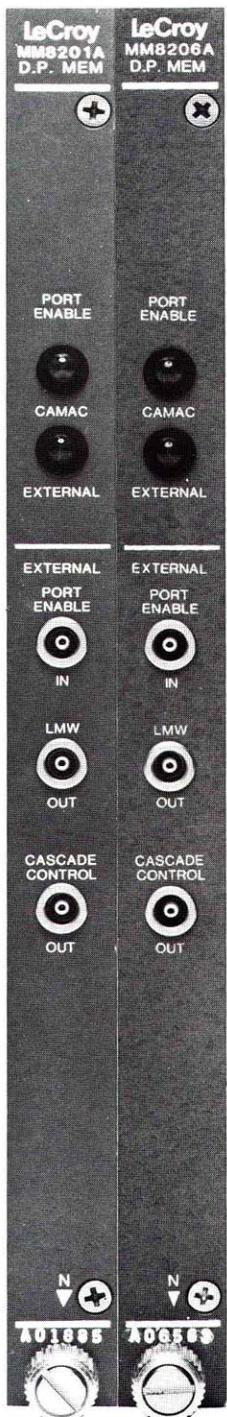
Q: A Q = 1 is generated in response to all valid F and A commands except for the following cases: 1) F(2)•A(0) when data is not valid (1st and 34th command for LG8252 and 1st and 18th command for LG8213); 2) F(8)•A(0) if internal LAM is not set; and 3) F(27)•A(0) if Continuous Scan mode is enabled.

L: In the single scan mode only, a Look-At-Me signal is generated after all inputs have been digitized unless previously disabled by F(11)•A(0). LAM is disabled for the duration of N and cleared by Z, C F(9)•A(0), or F(10)•A(0).

X: An X = 1 (Command Accepted) response is generated when a valid F, N, and A command is applied.

CAMAC FUNCTIONS

F(0)•A(i):	i = 0-15, read the data from input (i + 1). Requires N.
F(1)•A(i):	i = 0-15, read the data from input (i + 17). Requires N.
F(2)•A(0):	Read data in block transfer mode. First and last F(2)•A(0) commands respectively set up and terminate the mode (data transferred during these two cycles is not valid). A total of 34 (18) F(2)•A(0) commands must be issued to read all 32 (16) channels of the LG8252 (LG8213). Scanning is interrupted for the duration of the block transfer. Block transfer mode may be terminated early by use of Z, C, or F(9)•A(0). Q = 1 is returned if internal LAM is set.
F(8)•A(0):	Equivalent to Z or C.
F(9)•A(0):	Reset LAM (also terminates scanning).
F(10)•A(0):	Disable LAM.
F(11)•A(0):	Disables Single Scan mode and LAM. Enables Continuous Scan mode.
F(24)•A(0):	Initiates scanning of all inputs beginning with Channel 1. Requires N and S2. Required following Z, C, F(9), or F(24) to begin continuous scan. May be used to initiate Single Scan.
F(25)•A(0):	Enables Single Scan Mode and LAM. Disables Continuous Scan Mode.
F(26)•A(0):	Test Continuous Scan Mode. Q = 1 is returned if Single Scan mode is enabled.
F(27)•A(0):	
Scan Trigger:	Positive-going TTL-compatible pulse applied to front-panel LEMO-type connector initiates Single Scan of all inputs beginning with Channel 1. Input impedance, $510\ \Omega$. Pulse width should be greater than 100 nsec and less than $50\ \mu\text{sec}$. Inputs during scan will re-initialize scan beginning at Channel 1. Factory option allows use of complementary TTL pulses (input resistance is $2.7\text{ K}\Omega$ resistor pull-up to + 5V).
Mode Selection Switches:	Bipolar/Unipolar mode and offset binary/2's complement readout mode are selected by side panel switches.
Packaging:	In conformance with CAMAC standard for nuclear modules (ESONE Committee Report EUR4100 and IEEE #583). RF-shielded CAMAC #1 module.
Power Requirements:	750 mA at + 6 V 50 mA at + 24 V 50 mA at - 24 V



Models MM8201A and MM8206A Dual Port Memory Modules

- **High Capacity:** Choice of 16K words (MM8201A) or 64K words (MM8206A)
- **High Density:** Single-width CAMAC module
- **High Speed:** Better than 2.5 MHz Read/Write speed on External Port
- **Random/Sequential Access on CAMAC Port**
- **Sequential Access on External Port**
- **Simple Memory Cascading on External Port:** Up to 1 megaword of memory

The Models MM8201A and MM8206A Dual Port Memory modules provide 16K or 64K word memory densities in an economical CAMAC package. This packaging density allows a single CAMAC crate to hold almost 1.5 megawords of 16-bit memory.

The CAMAC Read and Write Port allows both random and sequential operation (for block transfers) with the Address Auto-Increment feature. The external port has sequential access in both read and write modes. The straightforward structure of the external bus simplifies interfacing of custom data sources to the convenient CAMAC standard. By simple interconnection, multiple memory modules can be cascaded to a total of sixteen modules of up to one megaword of memory. In addition, a two-module circular buffer can be configured to provide a simple CAMAC interface for continuous data sources, since the LAM generated when one memory module is filled can initiate a readout of that module, while the second module continues to store data. Other applications include local memory in a crate for the host processor, communications and data transfer points for multiprocessor CAMAC systems, and convenient source of data words to interface a control scheme to CAMAC.

Several specific data acquisition and control functions are implemented by LeCroy modules in conjunction with the Models MM8201A and MM8206A. These include:

- Multi-input, multichannel scaling or frequency logging (Models 3521 and 4433).
- Sequential recording ("List Mode") of data from Model 4204 TDC and Model 3512 ADC using the Model 3587 Data Router.
- Complex waveform generation (Model 8601).

SPECIFICATIONS

Models MM8201A and MM8206A

DUAL PORT MEMORY MODULES

MEMORY CHARACTERISTICS

General: Organized as a dual port memory with access by one port at a time. CAMAC commands determine which port is currently enabled. 16K × 1 bit (MM8201A) and 64K × 1 bit (MM8206A) Dynamic RAM IC's are used. Both the CAMAC and external ports operate in the auto-refresh mode. However, the external port may be operated in an access-refresh mode which permits higher access rates.

Speed: The CAMAC port will operate up to the maximum 1 MHz rate. The external port will operate in auto-refresh mode from DC to >1.0 MHz and in access-refresh mode from 75 kHz to >2.5 MHz.

CAMAC PORT

General: Utilizes CAMAC Dataway. CAMAC port permits both random and sequential access for either reading F(2) or writing F(16) of memory at the maximum CAMAC rate, 1 MHz.

Memory Read Operation: The CAMAC Memory read operation F(2) is buffered through an output register. This register is loaded at the time of an address write operation F(18), so the subsequent read operation F(2) reads out data from that location. In addition, the read operation causes the register to be updated. Consequently, the address auto-increment mode F(25) allows sequential access to the memory for block transfers of data. (Note: Such block transfers require one additional read operation F(2), following an address write operation F(18). Refer to manual).

Memory Write Operation: The CAMAC memory write operation F(16) writes directly into the current memory address. Address auto-increment mode F(25) provides for sequential access for block transfers.

EXTERNAL PORT

General: The external data bus is on a rear panel connector which mates with Model DC 8800 Data Cable. External port is a read or write sequential port (memory address auto-increment must be enabled). Memory strobe is assumed to be an external device on the data bus. The external port can be daisy-chain interconnected with other modules to achieve cascading of multiple memory modules. Memory control is then accomplished by connecting the Cascade Control output of a module to the External Port Enable input of the next module.

Data Bus Signals: Memory Strobe—50 nsec minimum width, TTL level. Strobed a positive-going edge.

R/W-TTL high to read, low to write.

—Refresh Control TTL low disables internal auto-refresh and enables access-refresh mode. Refresh control line is ignored when Refresh Enable side panel switch is in ON position.

—Data 16 bi-directional read/write lines. TTL high corresponds to a 1 or "True". Data is to be established no later than 50 nsec after the memory strobe for the write mode. Data is available 550 nsec after memory strobe for reading in the auto-refresh mode and 220 nsec after memory strobe for reading in the access-refresh mode.

Refresh Mode: The External port may be operated in either auto-refresh or access refresh modes when Refresh Enable side panel switch is the OFF position. The auto-refresh mode allows operation at rates from DC to >1 MHz. The access-refresh mode accomplishes refresh during read and write cycles resulting in allowable memory strobe rates of 75 kHz to >2.5 MHz. Switching between the two modes is controlled by the refresh-control line. The access refresh mode is only operative if the external port is in no way disabled. If the port is disabled for any reason, the auto refresh mode becomes operative. No memory strobe may occur within 330 nsec of the beginning or end of an access-refresh period.

LMW Disable: Module may be configured (Cascade side panel switch) to disable the external port when memory is full. The external port is then subsequently re-enabled by a positive-going TTL edge at the External Port Enable input or by enabling the external port from CAMAC F(11).

PORT ENABLE LED'S

CAMAC: Lights when CAMAC port is enabled.

External: Lights when external port is enabled. Note that either front panel disable or LMW Disable will extinguish the LED.

COAXIAL CONNECTERS

External Port Enable: TTL low level disables external port. Open input or TTL high level enables external port if external port has been enabled from CAMAC F(11) and if LMW Disable (Input) is not active. Transition from low to high at this input resets LMW Disable status.

>8 mA source current.

LMW (Output): TTL pulse, 500 nsec width, generated when memory is full. Drives 50 Ω.

Cascade Control (Output): TTL level, drives 50 Ω. Transition from low-to-high occurs when last memory word is addressed or under CAMAC Command F(27).

High-to-low transition occurs when External Port Enable receives positive-going TTL edge, or when External port is enabled, F(11). Output is intended to permit cascading of memory modules at the external port by connecting this output to the External Port Enable input of the next module.

GENERAL

Cascade Switch: Side panel switch set to ON causes external port to be disabled after last memory word has been accessed. Otherwise, subsequent external port memory operations access sequential memory addresses within the module beginning at zero. LNW Disable status is reset (port enabled) by a memory configuration of multiple modules. See manual.

Refresh Enable Switch: In the ON position, this switch allows only auto-refresh mode. The OFF position causes the refresh-control line of external port to determine refresh mode when external port is active.

External Port Clock Termination Switch: ON position terminates external port clock line in 100 Ω for improved performance for longer bus lines. For cascaded memory modules, only the last module should be terminated.

Packaging: In conformance with the international CAMAC Standard (European ESONE Report EUR 4100e and IEEE Std. 583-1975). RF-shielded, single-width CAMAC module.

Power Requirements: 500 mA at +6 V plus 50 (60) mA per bit word size for 16K word (64K word) version.

CAMAC COMMANDS

L: A LAM is generated when last memory word is accessed, if previously enabled by F(26)•A(0).

X: An X = 1 response is generated for any valid code.

Q: A Q = 1 response is generated in response to F(0), F(2), F(16), and F(18) operations if CAMAC port is enabled and to F(8) if LAM is set. Otherwise, Q = 0.

Z: INITIALIZE clears and disables LAM, and enables CAMAC port and address auto increment.

CAMAC FUNCTION CODES

F(0)•A(0): Read memory address register on lines R1-R14 (lines R1-R16 for MM8206A).

F(2)•A(0): Read data from memory at the address in the address register. If auto increment is enabled the address register will be subsequently incremented. Data buffered through Data Output Register.

F(8)•A(0): Test LAM. Q = 1 if LAM is set.

F(9)•A(0): Clear module. Sets memory address to zero, clears and disables LAM, and enables CAMAC port and address auto increment.

F(10)•A(0): Clear LAM.

F(11)•A(0): Enable external port.

F(16)•A(0): Write data to memory at the address in the address register. If auto increment is enabled, the address register will be subsequently incremented.

F(17)•A(0): Disable address auto increment.

F(18)•A(0): Load memory address register from CAMAC lines W1-W14. (W1-W16 for MM8206A).

F(19)•A(0): Disable external port.

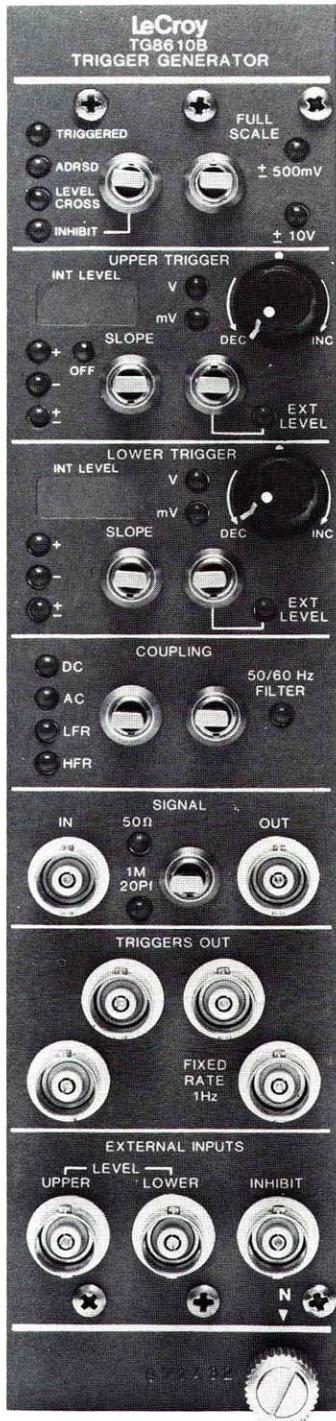
F(24)•A(0): Disable LAM.

F(25)•A(0): Enable address auto increment.

F(26)•A(0): Enable LAM.

F(27)•A(0): Set Cascade Control output to high state.

SPECIFICATIONS SUBJECT TO CHANGE



Model TG8610B Trigger Generator

- Window triggering
- Time variable region of interest monitoring
- Dual slope and single slope modes
- 8-bit resolution for trigger level settings
- 1 V and 20 V full-scale trigger level ranges
- Programmable and manually controllable
- Numeric LED display of control settings
- Flexible trigger signal coupling including 50/60 Hz notch filter
- Bridged signal input for trigger pickoff with minimal signal distortion
- 3 parallel trigger outputs
- Inhibit control

The Model TG8610B is a trigger generator designed to cover a wide range of input signal conditions and to give the user the flexible but simple controls needed to completely define the conditions under which a trigger pulse is generated. In addition to the normal single-level, slope-sensitive (+ or -) triggering over selectable full-scale input ranges (± 0.5 V and ± 10 V), a slope-independent mode (\pm) is included for generating a trigger when the slope of the signal is unknown.

A "window" trigger is implemented by providing two trigger circuits, each with fully independent controls, whose outputs are logically OR'd to produce the final trigger signal. The settings for the two trigger levels define the upper and lower voltage boundaries of the window so that size window may be positioned anywhere within the full-scale range. The slope settings at each boundary may then determine whether the trigger will be generated when the signal enters the window or when it leaves the window ("glitch" detection).

The external trigger level inputs make it possible to vary the trigger level in real time. By using an external analog signal for both levels, a time variable window can be controlled to monitor a varying region of interest.

The input is bridged for convenient trigger pickoff. Either impedance or 50Ω termination may be selected. Signal coupling choices to the trigger stage are DC, AC, AC LFR, and AC HFR. A 50/60 Hz notch filter may be selected to reduce sensitivity to line frequency signals.

The TG8610B provides for complete control of trigger setup from both the front panel and from the computer. Trigger status may be read by the computer at any time, while LED numeric readouts and indicators continuously display that status at the front panel. Three trigger outputs are available at the front panel. The trigger may generate an interrupt to the computer.

SPECIFICATIONS

Model TG8610B

TRIGGER GENERATOR

SIGNAL INPUT/OUTPUT

Impedance: The signal input and output are wire-bridged together. Impedance is $50\ \Omega$ or high Z (selectable). High Z impedance is $1\ M\Omega$, 20 pfd when on DC or AC, $15\ k\Omega$ on AC LF rej or AC HF rej.
 Coupling: DC, AC, AC LF rej, AC HF rej.
 Notch Filter: Approximately 30 dB attenuation at 60 Hz (Internally tunable to 50 Hz), independent of other coupling choices.

TRIGGER

Controls: Two independent sets (upper and lower) of level and slope controls allow window triggering. Turning off one set provides single level/slope trigger settings.
 Slope: +, -, and \pm . These slope selections will cause a trigger to be generated by a signal with a rising slope (at the selected level), a falling slope or either slope, respectively.
 Range: From +508 mV to -512 mV in 4 mV steps, or from +10.16 V to -10.24 V in 80 mV steps. Numeric LED readout of the three most significant digits (99.9 maximum). Upper and lower trigger levels are independent of each other (within the same range).
 Accuracy: CAMAC programmed trigger level settings, $\pm 1\%$ of full scale. Panel readout and manual setting accuracy, $\pm 2\%$. Temperature coefficient, $\pm 100\ \mu V^{\circ}C$.
 External Level: The voltage supplied to an External Level Input establishes the trigger level when EXT Level is selected. The full-scale range is +5 V to -5 V independent of the full scale selected for the signal generating the trigger. Analog bandwidth 1 MHz (3dB).
 Pulse Outputs: Three with simultaneous outputs. TTL levels, positive transition is trigger, approx. 80 nsec duration. Drives $50\ \Omega$.
 Fixed Rate Out: A single 1 Hz output can be used for setup convenience as an external start pulse to a transient recorder. TTL square wave output drives $50\ \Omega$.
 Inhibit: Triggers can be inhibited by manual control, CAMAC command, or by applying an inhibit signal to the front-panel connector. TTL level (+2 V to +5 V) inhibits. $50\ \Omega$ impedance.

LED'S

Triggered: Flashes when trigger pulse is generated.
 Addressed: Lights while being addressed by CAMAC.
 Level Crossed: Lights when upper/lower trigger level settings are inverted.

DATA FORMAT

CAMAC CONTROLS

L: A Look-At-Me (LAM) is raised when a trigger is generated if previously enabled by F(26)•A(0). Q = 1 is generated in response to F(8) if LAM is set, and to the read F(1) and write F(17) functions, A(0) through A(3). Otherwise, Q = 0.
 X: X = 1 is generated in response to all valid F and A codes.
 Z or C: Resets all status bits to 0 and trigger level DAC's to 0 V. Also resets LAM.
 I: Inhibit prevents trigger from being generated.

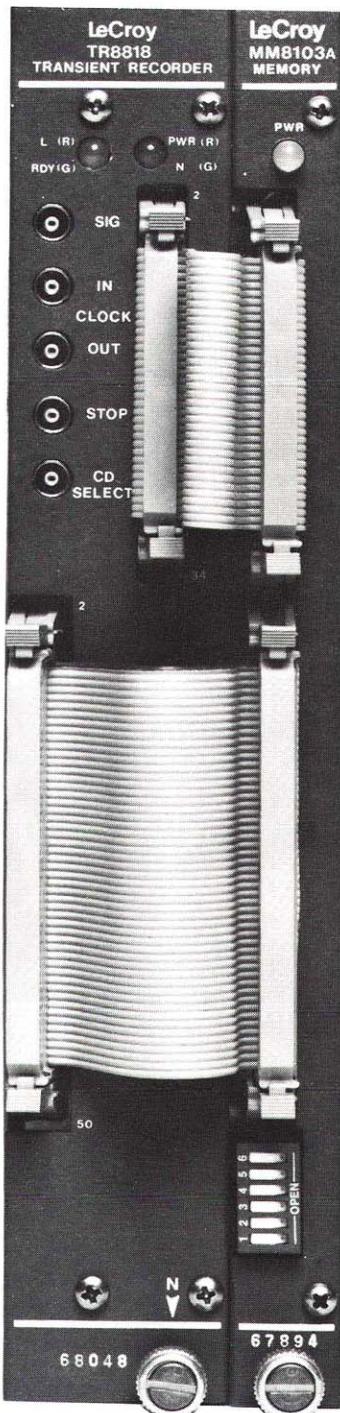
CAMAC FUNCTIONS

F(1)•A(0): Read Inhibit Status Register. LSB = 1 indicates trigger output is inhibited either by F(17)•A(0) or by front-panel switch.
 F(1)•A(1): Read Module Status Register. See F(17)•A(1).
 F(1)•A(2): Read Lower Trigger Level Register (R1-R8).
 F(1)•A(3): Read Upper Trigger Level Register (R1-R8).
 F(6)•A(0): Read Module Identifier. Returns the number 610 in binary code on R1-R10.
 F(8)•A(0): Test LAM. Q = 1 is returned if LAM is active, whether or not LAM is enabled.
 F(9)•A(9): Resets module. Equivalent to Z or C.
 F(10)•A(0): Resets LAM.
 F(17)•A(0): LSB = 1 sets the Inhibit Register, causing trigger output to be inhibited, and LSB = 0 clears the register.
 Bit assignments on both Read F(1)•A(1) and Write F(17)•A(1) are:
 Bit 1 Full-Scale Range: 0 = 1 V range, 1 = 20 V range.
 Bits 2-3 Signal Coupling: 00 = DC, 01 = AC, 10 = AC LF rej, 11 = DC LF rej.
 Bit 4 50/60 Hz Notch Filter: 0 = Disable, 1 = Enable.
 Bit 5 Signal Termination: 0 = high Z, 1 = $50\ \Omega$.
 Bits 6-7 Lower Trigger Slope: 00 = off, 01 = + slope, 10 = - slope, 11 = \pm slope.
 Bit 8 Lower Trigger Level Source: 0 = Int, 1 = Ext.
 Bits 9-10 Upper Trigger Slope: same as bits 6-7.
 Bit 11 Upper Trigger Level: Source as Bit 8.
 F(17)•A(2): Write Lower trigger Level Register (8-bit DAC) on W1-W8. Range from 0 to 255 (-128 to 127 for two's complement Data Format) corresponds to most-negative through most-positive trigger level. Conversion factor is 4 mV (80 mV) per LSB for 1 V (20 V) full scale.
 F(17)•A(3): Write Upper Trigger Level Register. Same format as F(17)•A(2).
 F(24)•A(0): Disables LAM.
 F(25)•A(0): Generates Trigger from module at S1 time.
 F(26)•A(0): Enables LAM.

GENERAL

Connectors: Coaxial BNC type.
 Controls: All controls can be set manually and can be programmed by computer. Control settings are continuously displayed by LED's and are computer readable.
 Packaging: In conformance with CAMAC standard for instrumentation modules (IEEE Standard 583, European Esone Report #EUR4100e, EUR46003) RF shielded CAMAC #3 width module.
 Power Requirements: 3 A at +6 V, 400 mA at +24 V, 150 mA at -24 V

SPECIFICATIONS SUBJECT TO CHANGE



Models TR8818 and MM8103A 100 Megasample/Second Transient Recorder

- 8-bit resolution
- Excellent dynamic accuracy
- 32-512 ksample, expandable memory
- Variable active memory size in 8 ksample steps
- DC to >100 MHz bandwidth
- Self-contained programmable clock
- 10 psec aperture uncertainty
- Pre-trigger recording
- Battery backup for stored data
- Digitally programmable signal offset
- Compact modular packaging

A major advance in the dynamic accuracy of high speed analog-to-digital converters is incorporated within the Model TR8818 transient recorder. The instrument can digitize a 50 MHz sinewave at 10 nsec intervals with 6.5 effective bit accuracy (resolution is 8 bits). Fast slew rate signals do not degrade these accuracies. A reconstructed, digitized full-scale signal will be accurate within the stated number of effective bits. The record length available for storing waveforms can be expanded from a minimum of 32,768 samples to a total of 512 ksample by using from 1 to 16 Model MM8103A Memory Modules. The amount of memory activated can be operationally varied from 8 ksamples up to the total size of installed memory in 8 ksample increments. By activating only the amount of memory needed for a particular application, data acquisition time, data transfer time, computer time and archiving storage space can all be minimized.

Both stored waveform data and control register settings are protected against power interrupt by internal batteries. The waveform recorder is fully programmable including an internal sampling clock and digital signal offset. A bandwidth of DC to >100 MHz (3 dB) fully supports the digitizer's 50 MHz Nyquist frequency. Variable pre-trigger recording allows storing all of a waveform even when a trigger is generated from the waveform itself.

Very fast, complex transient waveforms can now be recorded with confidence in the accuracy of even the highest slew rate portions of the signal. Rapid variations in the recorded waveform, even at amplitudes of only a few percent of full scale, can be recovered as usable data, rather than ignored as artifacts of poor ADC performance at high frequency. A wide variety of applications—including explosives tests, laser research, plasma physics, nuclear physics, power switching, and time-of-flight spectroscopy—can benefit from this important improvement in data quality. The modular architecture and low instrument cost make this unit especially attractive in those applications requiring long record length, simultaneous sampling of multiple inputs, high density, and maximum system flexibility.

The Model TR8818 is one instrument in LeCroy's extensive line of high performance, modular instruments intended to cover the range of signal measurement requirements from DC to near-gigahertz frequencies. Instruments range across the spectrum and include transient recorders, gated integrators, time interval meters, logic arrays, high speed data processors, and scanning DVM's together with support modules like trigger generators, counters, clocks, amplifiers, fiberoptic links, etc. The number of available instruments means that many specialized measurement requirements can be configured from a selection of off-the-shelf instruments while their modular nature ensures a flexible, expandable, and cost-effective solution. The modular standard used (CAMAC, IEEE Std 583-1975) provides RF-shielded enclosures, high speed communication (to 3 Mbytes per second), and computer-compatible architecture including interfacing to GPIB (IEEE Std 488-1978), and to most data acquisition computer buses.

SPECIFICATIONS

Models TR8818 and MM8103A

100 MEGASAMPLE/SECOND TRANSIENT RECORDER

ANALOG INPUT CHARACTERISTICS

Signal Range: 512 mV peak to peak (2 mV/code).
 Gain Accuracy: Within 2% of nominal.
 Temp. Stability: $\pm 0.04\%$ of F.S./°C max (less than 1 code change/10°C).
 Offset: $\pm \frac{1}{2}$ full scale in 256 steps (8-bit resolution) with 2% accuracy. The ± 256 mV offset range allows acceptance of 512 mV unipolar positive, unipolar negative, or bipolar inputs. The offset value can be computer programmed and read via F(19) and F(1). Manual control of the offset value is available by using a companion Model CD8828B Control and Display unit. A single CD8828B will control all TR8818s installed in the same crate.
 Bandwidth: >100 MHz (3 dB) for amplitudes up to the full 512 mV signal range. >50 MHz at 1 dB.
 Impedance: 50 Ω ± 3%.
 Overvoltage Protection: ± 500 V (≥ 50 Ω source) for 30 nsec, ± 100 V (≥ 50 Ω source) for 100 μsec, ± 2.5 V DC continuous.
 Overdrive Recovery: Recovers to within ± 1 LSB from $\times 2$ overdrive within 25 nsec.

ANALOG-TO-DIGITAL CONVERTER CHARACTERISTICS

Conversion Rate: DC to 100 megasamples per second.
 Conversion Clock: Internal crystal controlled oscillator; 10, 20, 40, 80, 160, 320 or 640 nsec clock periods, or External, are programmable and computer readable via F(16) and F(0). Manual control and visual reading of the clock period is available by using a companion Model CD8828B Control and Display unit. A single CD8828B will control all TR8818s in the same crate.
 Resolution: 8-bits (1 part in 256).
 Code: Offset binary.
 Aperture Uncertainty: ± 10 psec maximum.
 DC Accuracy: Less than ± 1.5 LSB's plus $\frac{1}{2}$ LSB quantizing error from best linear fit over entire range.
 AC Accuracy: A digitized pure sinewave has, compared to an ideal 8-bit ADC, a dynamic accuracy that is better than or equal to:

Signal-Noise Ratio	Effective Bits	Signal Frequency	Signal Amplitude (% of full scale)
39 dB	6.5	Up to 5 MHz	80%
37 dB	6.2	5 to 20 MHz	80%
35 dB	6.5	20 to 50 MHz	50%

Noise: The worst case RMS noise not including misconversions is less than 2 LBS's. The misconversion rate is less than 1 per 32 ksamples. Any conversion in error by more than 4 LSB's is a misconversion.

CONTROL AND DISPLAY

Computer: All Transient Recorder operating parameters can be computer programmed via the CAMAC dataway. Data and Status can be computer read.
 Manual: Use of a Model CD8828B Control/Display module allows control and readout access via the CAMAC dataway. One CD8828B can control and provide scope compatible display data for any selected TR8818 digitizer in the same crate by connecting one front panel cable to the CD Select input of the desired digitizer. The Control and Display module inserts into any CAMAC slot in crate. It is not effected by other CAMAC standard controllers installed in the crate as long as they are not generating commands while the CD module is in use.

MEMORY

Size: From 32 ksamples (32, 768 samples) to 512 ksamples of data memory can be installed by connecting from 1 to 16 Model MM8103A Memory modules.
 The amount of memory activated can be operationally varied from 8 ksamples up to the total size of memory installed in 8 ksample increments. By activating only the amount of memory needed for a particular application, data acquisition time, data transfer time, computer time, and archiving storage space can all be minimized. Active memory size can be computer programmed and read via F(16) and F(0). Manual control of the active memory size is available by using a companion CD8828B Control and Display Unit.
 Pre-trigger Samples: Memory can be divided into pretrigger and post-trigger sample storage in increments of 1/8 of the active memory. Range 0/8 thru 8/8 pre-trigger samples computer programmable and readable using F(16) and F(0). Manual control via companion CD8828B.
 Battery Backup: An internal replaceable battery becomes the power source for data in the memory and status registers if the line power is interrupted. Battery life is nominally 2 years.

FRONT PANEL CONNECTORS

Analog Input:	(See Analog Input Characteristics above).
Stop Trigger:	50 Ω accepts ECL pulses (jumper option for TTL), positive edge sensitive. Minimum duration, 8 nsec. Protected against 5 A transients for 1 μsec. Stops sampling after selected number of post-trigger samples have been stored.
Clock In:	50 Ω. ECL compatible (jumper option for TTL). Conversion initiated on positive going edge. Minimum duration, 5 nsec. Valid frequency, DC to 100 MHz. Protected against 5 A transient for 1 μsec. 16 clock pulses must be received after the last data sample in order to transfer the last 8 samples to memory
CD Select:	Accepts strobe inputs from CD8828B Control/Display module to provide local control and oscilloscope display. Quiescently high TTL level, clamp to ground forces equivalent of CAMAC N.
Clock Out:	Provides ECL clock pulses at the selected sampling frequency. Requires termination of 50 Ω to – 2 V.

FRONT PANEL INDICATORS

N/Power:	Dual LED; GREEN indicates a CAMAC cycle is being executed, RED indicates that all voltages are supplied in the module.
Ready/LAM:	Dual LED; GREEN indicates the clock has been enabled and unit is ready to digitize and store data (e.g., external Clock Input is enabled or internal clock started), RED indicates that a digitizing sequence has occurred and memory has valid data (i.e. internal LAM is set).

MODULE IDENTIFIER

Responds to computer inquiry with code to allow ready identification of configuration in systems. Eight bits can be used to assign a unique identification number to each unit and/or to identify module type. Read using F(3). The 8 bits are set by a switch register accessible through the bottom of the module.

POWER

Normal Operation:	CAMAC powers all circuitry under normal conditions (other than power fail). All functions of the digitizer and memories are operational. The TR8818 requires 440 mA at + 6 V, 7.35 A at – 6 V, 220 mA at + 24 V, 140 mA at – 24 V. Each MM8103A requires 2.5 A at + 6 V, and 1.8 A at – 6 V.
Battery Backup:	If CAMAC power is interrupted, an internal Lithium battery in each memory module and the TR8818 automatically becomes the power source for data in the memories and status registers. The digitizer cannot be operated nor can the memories or status registers be read under data backup power. When correct voltages reoccur after power failure, the unit automatically becomes fully operational. The lifetime of the Lithium battery is greater than 2 years in the backup mode. (Batteries are replaceable).

GENERAL

Connectors:	All signal and control connectors on the front panel of the TR8818 are coaxial Lemo type (compatible with LeCroy LE/LE-m and LE/BC-m signal cables).
Packaging:	TR8818: 221 mmH, 34 mmD, 292 mmW* (8.7 in × 1.4 in × 11.5 in) MM8103A: 221 mmH, 18 mmD, 292 mmW* (8.7 in × 0.7 in × 11.5 in). *Depth front to rear panel. Rear connector 13 mm (0.5 in.). Front panel controls approx. 20 mm (0.8 in).
	In conformance with the CAMAC standard for instrumentation modules (IEEE Standard 583, European Esone Report #EUR4100e) RF shielded CAMAC modules. TR8818 is #2 width. MM8103A is #1 width.
Temperature Range:	Ambient operating range to maintain analog specifications: + 15°C to + 35°C (Requires crate with sufficient air flow to maintain exhaust air temperature of 50°C.) Data retention guaranteed to + 50°C ambient.

CAMAC COMMANDS

X:	An X = 1 response is generated when a valid Function (F) command with A(0)•N is decoded. (X = 0 if Memory Power Fail is received.)
Q:	A Q = 1 response is generated (only if unit is not in Ready state) for all Read and Write functions except Q = 0 after last data word when using F(2). Also, if LAM is set, Q = 1 for F(8) if LAM is Enabled and for F(27) independent of LAM Enable.
L(LAM):	A Look-At-Me is generated at the end of the sampling sequence, if previously enabled by F(26).
Z:	Recommended after powerup or power interruption. LAM cleared and disabled. Does not affect any other memory so data is preserved.

CAMAC FUNCTION CODES (All respond to A(O) only)

F(0): Reads pre-trigger sample size (R1-R4), sampling period (R5-R7) and active memory size (R9-R14).

R4	R3	R2	R1	Pre-trigger Samples	R7	R6	R5	FREQ(MHz)	R14	R13	R12	R11	R10	R9	Memory Size
0	0	0	0	0/8 of memory	0	0	0	100	0	0	0	0	0	0	8K
0	0	0	1	1/8 of memory	0	0	1	50	0	0	0	0	0	1	16K
.	0	1	0	25	0	0	0	0	1	0	24K
.	0	1	1	12.5	0	0	0	0	1	1	32K
.	1	0	0	6.25
0	1	1	1	7/8 of memory	1	0	1	3.125
1	0	0	0	8/8 of memory	1	1	0	1.5625
					1	1	1	External	1	1	1	1	1	1	512K

F(1): Read single (last) sample taken (R1-R8) and input offset ± 256 mV (R9-R16, offset binary).

F(2): Read waveform data in 16-bit words, two samples at a time. The first word read following the issuance of an F(17) is a status word. Its LSB indicates which byte of the second word starts the data record. If LSB = 0, then R1-R8 of the second word is the first sample, R9-R16 of the second word is the second sample, etc. If LSB = 1, then R9-R16 of the second word is the first sample, R1-R8 of the third word is the second sample, etc. In either case, the first sixteen samples may have been overwritten and should be discarded from the data record. A Q = 0 is returned after the last data word.

F(3): Read module identifier (R1-R8).

F(8): Test LAM. Q = 1 is returned if internal LAM is set and enabled.

F(9): Set unit in Ready state, start digitizing, if using internal clock.

F(10): Clear LAM.

F(11): Digitize Single Sample

F(16): Write pre-trigger samples (W1-W4), sampling period (W5-W7) and active memory size (W9-W14) as defined under F(0) above. W15 and W16 must always be zero.

F(17): Enable Read Mode. Required just prior to reading the waveform data (F(2). Must be followed by F(2) or Z.

F(19): Write offset ± 256 mV (W1-W8, offset binary, 2 mV per LSB)

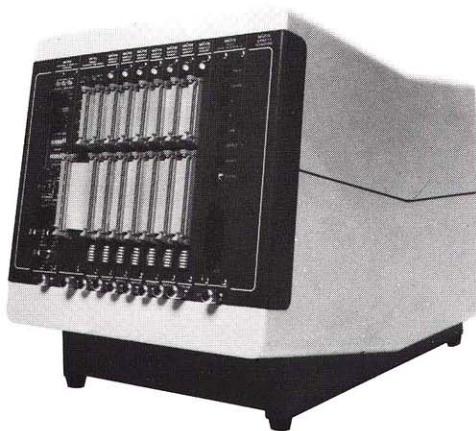
F(24): Disable LAM.

F(25): Computer Stop Trigger.

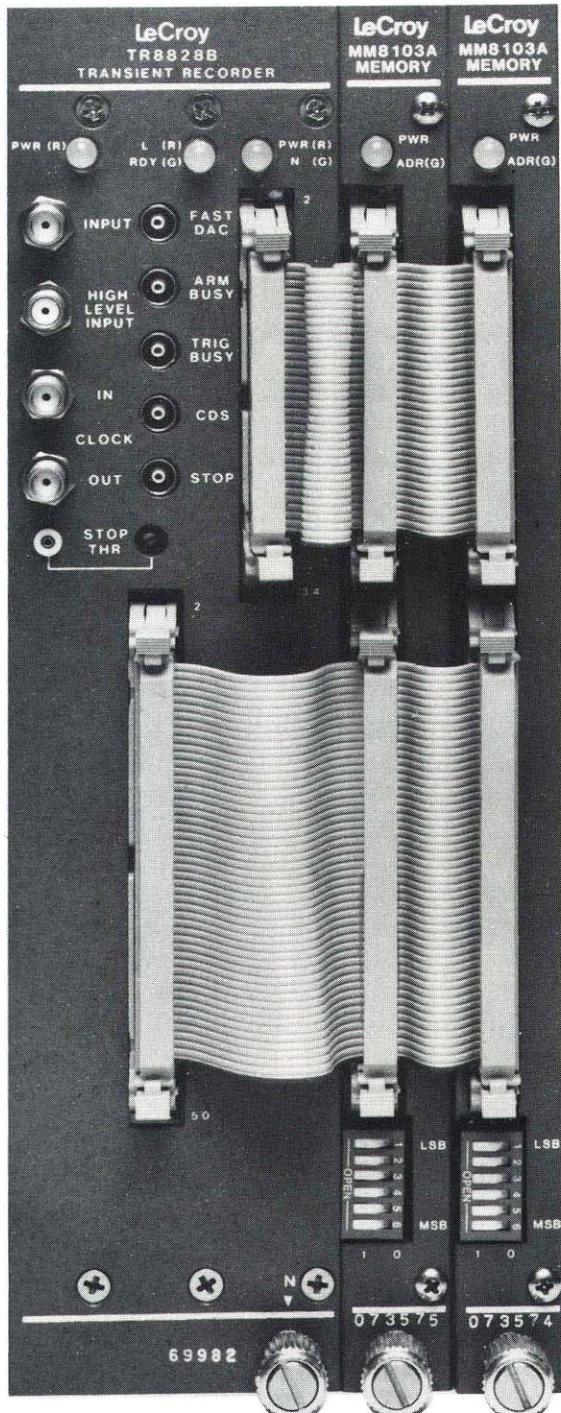
F(26): Enable LAM.

F(27): Test LAM. Q = 1 is returned if LAM is set, independent of LAM enable state.

SPECIFICATIONS SUBJECT TO CHANGE



Model TR8818s installed in the 8013 Minicrate
with a GPIB Interface.



Models TR8828B and MM8103A 200 Megasample/Second Transient Recorder

- 8-bit resolution
- Excellent dynamic accuracy
- 64-512 ksample, expandable memory
- Variable active memory size in 16 ksample steps
- DC to >100 MHz bandwidth
- Self-contained programmable clock
- 5 psec aperture uncertainty
- Pre-trigger recording
- Battery backup for stored data
- Digitally programmable signal offset
- Compact modular packaging

The TR8828B brings simplicity, accuracy, reliability, and affordability to 100 MHz analog bandwidth transient recording and waveform analysis. The TR8828B system consists of an ADC module which performs analog-to-digital conversion at rates up to 200 megasamples/sec, two or more memory modules, a CAMAC crate, and an interface to a computer and/or the Model CD8828B Control and Display Module. Because the data is converted real time rather than by equivalent time sampling, this recorder can be used for capturing single shot events, as well as, repetitive signals.

The unique new high speed analog-to-digital converter incorporated within the Model TR8828B Transient Recorder can digitize a 100 MHz sinewave at 5 nsec intervals with 5.0 effective bit accuracy (resolution is 8 bits). For lower signal frequencies the accuracy increases to 7.0 bits. A reconstructed, digitized full scale signal will be accurate within the stated number of effective bits. A bandwidth of DC to >100 MHz (3 dB) fully supports the digitizer's 100 MHz Nyquist frequency. Variable pre-trigger recording allows storing all of a waveform even when a trigger is generated from the waveform itself.

Very fast, complex transient waveforms can now be recorded with confidence in the accuracy of even the highest slew rate portions of the signal. Rapid variations in the recorded waveform, even at amplitudes of only a few percent of full scale, can be recovered as usable data, rather than ignored as artifacts of poor ADC performance at high frequency. A wide variety of applications can benefit from this important improvement in data quality. The modular architecture and low instrument cost make this unit especially attractive in those applications requiring long record length, simultaneous sampling of multiple inputs, high density, and maximum system flexibility.

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The digital data from the Model TR8828B Transient Recorder is stored real time in ultra high speed CMOS memory. A minimum of two Model MM8103A 32-ksample memory modules store 64 ksamples. Alternatively, one Model MM8104 may be used for 32 ksamples. The memory is expandable in 64-ksample increments to a total of 512 ksamples. Thus, transients on the order of milliseconds in duration can be fully resolved into sample points spaced 5 nsec apart. The memory is designed to retain digitized waveforms even if line power is lost. This makes the unit ideal for transient monitoring situations where the phenomena may interrupt power.

The instrument can be used either under program control via the CAMAC interface or by the optional IEEE 488 (GPIB) interface. It can also be used as a digital oscilloscope when accompanied by the CD8828B Control and Display unit. The CD8828B allows multiple modules in a CAMAC crate to be configured as one integral instrument with centralized display (using an oscilloscope) and manual control.

Because of its very long record length capability, the TR8828B is well suited for EW studies and communications signal acquisition. Data retention on power loss is a very useful feature for transmission line monitoring, explosives diagnostics, weapons effects testing, lightning research, and remote sensing. Full programmability means this transient recorder can be integrated into ATE applications, and into systems level multiple channel transient recording installations such as particle beam experiments, fusion research, accelerator diagnostics, and EMP research.

The Model TR8828B is one instrument in LeCroy's extensive line of high performance, modular instruments intended to cover the range of signal measurement requirements from DC to near-gigahertz frequencies. Instruments range across the spectrum and include transient recorders, gated integrators, time interval meters, logic arrays, high speed data processors, and scanning DVM's together with support modules like trigger generators, counters, clocks, amplifiers, fiberoptic links, etc. The number of available instruments means that many specialized measurement requirements can be configured from a selection of off-the-shelf instruments while their module nature ensures a flexible, and cost-effective solution. The modular standard used (CAMAC, IEEE Std 583-1975) means RF-shielded enclosures, high speed communication (to 3 Mbytes per second), and computer compatible architecture including off-the-shelf interfacing to GPIB (IEEE Std 488-1978), as well as, to most data acquisition computer buses.

SPECIFICATIONS Models TR8828B and MM8103A 200 MEGASAMPLE/SECOND TRANSIENT RECORDER

ANALOG INPUT CHARACTERISTICS

Inputs:	Signals connected to the two inputs are internally added before analog-to-digital conversion. A signal may be connected to either input, or to both simultaneously for added operation. The inputs are reverse isolated from each other by 30 dB for signals up to full bandwidth (signal from one input appearing at the other).
Signal Range:	512 mV peak-to-peak for normal input (2 mV/code). 5.12 V peak-to-peak for High Level Input.
Gain Accuracy:	Within 2% of nominal.
Temperature Stability:	± 0.04% of full scale/°C max (less than 1 code change/10°C).
Offset:	± 1/2 full scale in 256 steps (8-bit resolution). The offset range allows acceptance of unipolar positive, unipolar negative, or bipolar inputs. The offset value can be computer programmed and read via F(19) and F(1). Manual control of the offset value is available by using a companion Model CD8828B Control and Display unit. A single CD8828B will control all TR8828B's installed in the same crate.
Bandwidth:	DC to >100 MHz (3 dB). >50 MHz (1 dB). Both bandwidth figures are valid for amplitudes up to the full signal range.
Impedance:	50 Ω ± 3%.
Overshoot Protection:	± 500 V (≥50 Ω source) for 30 nsec, ± 100 V (≥50 Ω source) for 100 μsec, ± 2.5 V DC continuous for normal input (± 7.5 V DC continuous for High Level Input).
Overdrive Recovery:	Recover to within ± 1 LSB from × 2 overdrive within 25 nsec.

ANALOG-TO-DIGITAL CONVERTER CHARACTERISTICS

Conversion Rate:	3.125 to 200 megasamples per second.
Conversion Clock:	Internal clock periods of 5, 10, 20, 40, 80, 160 or 320 nsec, or External (must be 5 nsec) are programmable and computer readable via F(16) and F(0). Manual control of the clock period is available by using a companion Model CD8828B Control and Display unit. A single CD8828B will control all TR8828B's in the same crate.
Resolution:	8 bits (1 part in 256).
Code:	Offset binary, monotonic.
Linearity:	Less than ± 1/2 LSB (integral) plus 1/2 LSB quantizing error, or within one code from best linear fit.
Aperture Uncertainty:	± 5 psec maximum.
Accuracy:	A digitized pure sinewave has, compared to an ideal 8-bit ADC, a dynamic accuracy that is better than or equal to:

Effective Bits	Signal Frequency	Signal Amplitude (% of full scale)
6.5	Up to 5 MHz	80%
6.0	5 to 50 MHz	50%
4.5-5.0	50 to 100 MHz	50%

CONTROL AND DISPLAY

- Computer: All Transient Recorder operating parameters can be computer programmed via the CAMAC dataway. Data and Status can be computer read.
- Manual: Use of a Model CD8828B Control/Display module allows control and readout access via the CAMAC dataway. One CD8828B can control and provide scope compatible display data for any selected TR8828B digitizer in the same crate by connecting one front panel cable to the CD select input of the desired digitizer. The Control and Display module inserts into any CAMAC slot in the crate. It is not effected by other CAMAC standard controllers installed in the crate as long as they are not generating commands while the CD module is in use.

MEMORY

- Size: 32 ksamples to 512 ksamples of data memory can be installed in increments of 64 ksamples. One MM8104 Memory module = 32 ksamples and two Model MM8103A Memory modules = 64 ksamples (65,536). The amount of memory activated can be operationally varied from 16 ksamples up to the total size of memory installed in 16-ksample increments. By activating only the amount of memory needed for a particular application, data acquisition time, data transfer time, computer time, and archiving storage space can all be minimized. Active memory size can be computer programmed and read via F(16) and F(0). Manual control of the active memory size is available by using a companion CD8828B Control and Display Unit.
- Pre-trigger Samples: Memory can be divided into pre-trigger and post-trigger sample storage in increments of 1/8 of the active memory. Range 0/8 thru 8/8 pretrigger samples. Computer programmable and readable using F(16) and F(0). Manual control via companion CD8828B.
- Battery Backup: An internal replaceable battery becomes the power source for data in the memory and status registers if the line power is interrupted. Battery life is nominally 2 years.

FRONT PANEL CONNECTORS

- Input: SMA female connector, 50 Ω input impedance. Analog input for 512 mV peak-to-peak sensitivity.
- High Level Input: SMA female connector, 50 Ω input impedance. Analog input for 5.12 V peak-to-peak sensitivity.
- Clock In: SMA female connector, 50 Ω. ECL compatible. Valid frequency, 200 MHz. Termination to ground or – 2 V switchable via internal jumper.
- Clock Out: SMA female connector. ECL level requires 50 Ω termination. Provides the fixed internal frequency of 200 MHz ± 0.01% or, if selected, the external clock frequency. Termination can be to ground or – 2 V switchable via internal jumper.
- Stop Trigger: Lemo type connector, 50 Ω. Stop threshold monitored and adjusted from front panel. Termination to ground or – 2 V and slope switchable from the side panel. Minimum duration 8 nsec. Protected against 5-Amp transients for 1 μsec.
- CD Select (CDS): Lemo type connector accepts strobe inputs from a CD8828B Control/Display module to provide local control and oscilloscope display. Quiescently high TTL level, clamp to ground forces equivalent of CAMAC N.

FRONT PANEL INDICATORS

- N/Power: Dual LED; GREEN indicates a CAMAC cycle is being executed, RED indicates that all voltages are supplied to the right hand board in the module.
- Ready/LAM: Dual LED; GREEN indicates the clock has been enabled and unit is ready to digitize and store data (i.e., external Clock Input is enabled or internal clock started), RED indicates that a digitizing sequence has occurred and memory has valid data (i.e. internal LAM is set).
- Power: Single LED; RED indicates that all voltages are supplied to the left hand board in the module.

MODULE IDENTIFIER

Responds to computer inquiry with code to allow ready identification of configuration in systems. Eight bits are set by a switch accessible from the bottom of the module to assign a unique identification number to each unit and/or to identify module type. Read using F(3).

POWER

- Normal Operation: CAMAC powers all circuitry under normal conditions (other than power fail). All functions of the digitizer and memories are operational.
The TR8828B requires 500 mA at + 6 V, 8 A at – 6 V, 200 mA at + 24 V, 100 mA at – 24 V. Each MM8103A requires 2.3 A at + 6 V, and 1.8 A at – 6 V.
- Battery Backup: If CAMAC power is interrupted, an internal Lithium battery in each memory module and digitizer automatically becomes the power source for data in the memories and status register. The digitizer cannot be operated nor can the memories or status registers be read under data backup power. When correct voltages reoccur after power failure, the unit automatically becomes fully operational. The lifetime of the Lithium battery is greater than 2 years in the backup mode. (Batteries are replaceable).

GENERAL

- Packaging: TR8828B: 221 mmH, 51 mmW, 292 mmD* (8.7 in X 2.0 in X 11.5). Each MM8103A (minimum of two required): 221 mmH, 18 mmW, 292 mmD* (8.7 in X 0.7 in X 11.5 in).
- Temperature Range: Ambient operating range to maintain analog specifications: + 15°C to + 35°C (Requires crate with sufficient air flow to maintain exhaust air temperature of 50°C.) Data retention guaranteed to + 50°C ambient.

*Depth front to rear panel. Rear connector 13 mm (0.5 in.). Front panel controls approx. 20 mm (0.8 in.) in conformance with the CAMAC standard for instrumentation modules (IEEE Standard 583, European Esone Report #EUR4 100e) RF shielded CAMAC modules. TR8828B is #3 width. MM8103A is #1 width.

Power Requirements: TR8828B: 775 mA at + 6 V
 9.0 A at - 6 V
 220 mA at + 24 V
 175 mA at - 24 V
 MM8103A: 2.5 A at + 6 V
 1.8 A at - 6 V

CAMAC COMMANDS

- X: An X = 1 response is generated when a valid Function (F) command with A(0)•N is decoded. (X = 0 if Memory Power Fail is received.)
- Q: A Q = 1 response is generated for all Read and Write functions except when the unit is in the digitize or Ready state. In the Ready state, a Q = 1 is generated for F(25) only.
- L(LAM): A Look-At-Me is generated at the end of the sampling sequence, if previously enabled by F(26).
- Z: Recommended after power-up or power interruption. LAM cleared and disabled. Does not affect any other memory so data is preserved.

CAMAC FUNCTION CODES (All respond to A(O) only)

- Note: During the digitize or Ready state, all commands other than F(25) are ignored and Q = 0 is returned. Digitizing must be terminated via front panel stop or F(25) before other commands may be accepted.
- F(0): Read control register pre-trigger size (R1-R4), sampling period (R5-R7), active memory size (R9-R13), and user bits (R14-R16).

R9-R13	R5-R7	R1-R4
Memory Size	Sampling Period	Pre-trigger
0 16K	0 5 nsec	0 0/8 of active memory
1 32K	1 10 nsec	1 1/8 of active memory
2 48K	2 20 nsec	2 2/8 of active memory
*	3 40 nsec	3 3/8 of active memory
*	4 80 nsec	4 4/8 of active memory
*	5 160 nsec	5 5/8 of active memory
31 512K	6 320 nsec	6 6/8 of active memory
	7 EXT CLK	7 7/8 of active memory
	200 MHz only	8 8/8 of active memory

- F(1): Read offset register (R9-R16).
- F(2): Read the waveform data in 16-bit words. The two least significant bits of the first word, a status word, specifies which byte of the next two data words start the data record. If the status word is a 0, R1-R8 is the first data byte and R9-R16 is the second byte. If the word is 1, then R9-R16 is the first data byte, and R1-R8 of the next data word is the second data byte. If the status word is 2, the first data byte is R1-R8 of the second data word read. A status word of 3 indicates that the first data byte is R9-R16 of the second data word read. Q = 0 after the last data word is read. Due to memory organization, the first and last 16 data bytes may be inaccurate and should be discarded.
- F(3): Read module identifier (R1-R8).
- F(8): Test LAM. Q = 1 if LAM is set and enabled.
- F(9): Set unit in Ready State, clear LAM, and start digitizing if the internal clock is used. If the external clock is selected, enable the sampling clock. Q = 1 if not is Ready state.
- F(10): Clear LAM.
- F(16): Write to control register, pre-trigger size, sampling period, memory size, and user bits (W14-W16).

W9-W13	W5-W7	W1-W4
Memory Size	Sampling Period	Pre-trigger
0 16K	0 5 nsec	0 0/8 of active memory
1 32K	1 10 nsec	1 1/8 of active memory
2 48K	2 20 nsec	2 2/8 of active memory
*	3 40 nsec	3 3/8 of active memory
*	4 80 nsec	4 4/8 of active memory
*	5 160 nsec	5 5/8 of active memory
31 512K	6 320 nsec	6 6/8 of active memory
	7 EXT CLK	7 7/8 of active memory
	200 MHz only	8 8/8 of active memory

- F(17): Enable read mode. Sets address counter to beginning of data record so that F(2) will read data properly. Must be followed by F(2) or Z.
- F(19): Write to offset register. Use W1-W8 as binary input. With a grounded analog input, a code of 0 will produce an output sample of approximately 255. An offset code of 255 will produce a sample approximately equal to 0.
- F(24): Disable LAM.
- F(25): Computer stop trigger. Causes transient recorder to stop sampling after the selected number of post-trigger samples have been stored. Q = 1 when in Ready state.
- F(26): Enable LAM.
- F(27): Test LAM. Q = 1 is LAM is set independent of LAM enable.

SPECIFICATIONS SUBJECT TO CHANGE



Model TR8837F

32 Megasample/Second Transient Recorder

- 8-bit resolution
- Excellent dynamic accuracy
- 8K sample, internal memory
- Variable active memory size in 1K sample steps
- DC to >100 MHz bandwidth over entire input range
- Self-contained programmable clock
- 15 psec aperture uncertainty
- Pretrigger recording
- Battery backup for stored data
- Single-width CAMAC module
- Scope display output
- Front-panel LED display of status

State-of-the Art accuracy, low cost, comprehensive features and very high packaging density are combined in the LeCroy TR8837F Transient Recorder. The instrument has a 6.7 effective bit accuracy digitizing a 16 MHz full scale sinewave at a 32 megasample/sec conversion rate. Analog bandwidth exceeds 100 MHz (3 dB). The internal memory can be operated to store from 1024 to 8192 samples. By activating only the amount of memory needed for a particular application, data acquisition time, data transfer time, computer time and archiving storage space can all be minimized. A fraction of the active memory (0 to 7/8's) may be set to retain waveform data prior to the trigger. A selectable internal clock generates A/D conversions at rates from 32 megasample/sec to 500 kilosample/sec. Stored waveforms can be viewed via a scope display output. The TR8837F has internal battery backup to retain both stored sample data and all control settings if line power interrupts occur. All control settings are programmable.

This instrument makes it possible to directly record complex, fast transient waveforms in a very economical way. It is no longer necessary to depend on specialized signal conditioning or to depend on unverified assumptions about the waveform in order to extract the desired information. The modular architecture makes simultaneous recording of multiple inputs particularly simple and cost-effective. Application areas include plasma physics, nuclear and high energy physics research, medical ultrasound, time-of-flight spectroscopy, power switching, fault-monitoring, laser research and development, explosives, and general non-destructive test and automated test applications.

The Model TR8837F is one instrument in LeCroy's extensive line of high performance, modular instruments intended to cover the range of signal measurement requirements from DC to near-gigahertz frequencies. Instruments range across the spectrum and include transient recorders, gated integrators, time interval meters, logic arrays, high speed data processors, and scanning DVM's together with support modules like trigger generators, counters, clocks, amplifiers, fiberoptic links, etc. The number of available instruments means that many specialized measurement requirements can be configured from a selection of off-the-shelf instruments while their modular nature ensures a flexible, expandible, and cost-effective solution. The modular standard used (CAMAC, IEEE Std. 583-1975) means RF-shielded enclosures, high speed communication (to 3 megabytes/sec), and computer-compatible architecture including off-the-shelf interfacing to GPIB (IEEE Std. 488-1978) as well as to most data acquisition computer buses.

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SPECIFICATIONS

Model TR8837F

32 MEGASAMPLE/SECOND TRANSIENT RECORDER

ANALOG INPUT CHARACTERISTICS

Signal Range:	512 mV p-p (2mV/code).
Gain Accuracy:	Within 2% of nominal.
Temp. Stability:	$\pm 0.04\%$ of F.S./°C max (less than 1 code change/10°C).
Offset:	The input signal offset is adjustable via a front-panel potentiometer. The offset range is ± 256 mV, allowing acceptance of 512 mV unipolar positive, unipolar negative, or bipolar inputs. Front-panel test point has voltage range of 0 V to +8 V nominally corresponding to offsets from -256 mV to +256 mV.
Analog Bandwidth:	DC to > 100 MHz (3 dB) for full scale input.
Impedance:	50 Ω ± 3%.
Overdrive Recovery:	Recovers to within ± 1 LSB from × 2 overdrive within 25 nsec.
Overvoltage Protection:	± 500 V (≥ 50 Ω source) for 30 nsec, ± 100 V (≥ 50 Ω source) for 100 μsec, ± 2.5 V DC continuous.

ANALOG-TO-DIGITAL CONVERTER CHARACTERISTICS

Conversion Rate:	DC to 32 megasample/sec.
Conversion Clock:	Internal clock frequency of 32, 16, 8, 4, 2, 1 or 0.5 MHz, or External are computer programmable and readable via F(16) and F(0). Manual control is available by using a companion Model CD8828B Control and Display unit. A single CD8828B will control all TR8837F's in the same crate.
Resolution:	8 bits (1 part in 256).
Code:	Offset binary, monotonic.
Aperture Uncertainty:	± 15 psec max.
DC Accuracy:	Less than ± 1 LSB plus 1/2 LSB quantizing error from best linear fit over entire range.
AC Accuracy:	A digitalized pure sinewave has, compared to an ideal 8-bit ADC, a dynamic accuracy that is better than or equal to:

Signal-Noise Ratio	Effective Bits	Signal Frequency	Signal Amplitude (% of full scale)
42 dB	7.0	Up to 5 MHz	80%
40 dB	6.7	5 to 16 MHz	80%

MEMORY

Size:	The amount of memory activated can be operationally varied from 8K samples down to 1K sample increments. By activating only the amount of memory needed for a particular application, data acquisition time, data transfer time, computer time and archiving storage space can all be minimized. Active memory size can be computer programmed and read via F(16) and F(0). Manual control of the active memory size is available by using a companion CD8828B Control and Display Unit.
Pretrigger Samples:	Memory can be divided into pretrigger and post-trigger sample storage in increments of 1/8 of the active memory. Range 0/8 thru 7/8 pretrigger samples. Computer programmable and readable using F(16) and F(0). Manual control via companion CD8828B.
Battery Backup:	An internal replaceable battery becomes the power source for data in the memory and status registers if the line is interrupted.

FRONT-PANEL CONNECTORS

Analog Input:	(See Analog Input Characteristics above.)
Stop Trigger:	50 Ω accepts ECL (TTL Jumper option) pulses, positive edge sensitive. Minimum duration, 10 nsec. Protected against 5 A transients for 1 μsec. Stops sampling after selected number of post-trigger samples have been stored.
Clock In:	50 Ω, ECL compatible (jumper option for TTL). Conversion initiated on positive going edge. Minimum duration, 15 nsec. Valid frequency DC to 32 MHz. Protected against 5 A transients for 1 μsec.
Clock Out:	Provides ECL clock pulses at the selected sampling frequency. Requires termination of 50 Ω to – 2 V.
Display Out:	Provides DAC output for displaying stored signal on oscilloscope. Output rate is 500 kHz.
Display Trigger:	Provides trigger for scope display. An internal jumper option converts this to a TTL input for synchronizing displays of multiple TR8837s.
CD Select:	Accepts strobe inputs from CD8828B Control/Display module to provide local control. Quiescently high TTL level, clamp to ground forces equivalent to CAMAC N.

FRONT-PANEL INDICATORS

N:	LED indicates a CAMAC cycle is being executed.
Ready:	LED indicates the clock has been enabled and unit is ready to digitize and store data (e.g., external clock input enabled or internal clock started).
Pretrigger Sample:	Three LED's indicate 1/8s of memory reserved for pretrigger samples.
Memory Size:	Three LED's indicate usable memory size.
Clock Frequency:	Three LED's indicate clock frequency.

CONTROL

Computer:	All Transient Recorder operating parameters can be computer programmed via the CAMAC dataway. Data and Status can be computer read.
Start/Stop:	Front-panel switch provides Start digitizing and Stop Trigger functions to allow manual control of digitizing cycle.
Manual:	Use of a Model CD8828B Control/Display module allows control via the CAMAC dataway. One CD8828B can control any selected TR8837F digitizer system in same crate by connecting one front-panel cable to the CD Select input of the desired digitizer. The Control and Display module inserts into any CAMAC slot in the crate. It is not affected by other CAMAC standard controllers installed in the crate as long as they are not generating commands while the CD module is in use.

MODULE IDENTIFIER

Responds to computer inquiry with code to allow ready identification of configuration in systems, 8 bits are set by a switch accessible from bottom of the module to assign unique identification number to each unit and/or to identify module type. Read using F(3).

POWER

Normal Operation:	CAMAC powers all circuitry under normal conditions (other than power fail). All functions of the digitizer and memories are operational. 2.3 A at + 6 V 150 mA at + 24 V 1.1 A at – 6 V 15 mA at – 24 V
Battery Backup:	If CAMAC power is interrupted, an internal Lithium battery in each memory module automatically becomes the power source for data in the memories and status register. The digitizer cannot be operated nor can the memories or status registers be read under data backup power. When correct voltages reoccur after power failure the unit automatically becomes fully operational. The lifetime of the Lithium battery is greater than two years in backup mode. (Batteries are replaceable).

CAMAC COMMANDS

- X: An X = 1 response is generated when a valid Function (F) command with A(0)•N is decoded.
A Q = 1 response is generated (only if unit is not in Ready state) for all Read and Write functions except Q = 0 after last data word when using F(2). Also, if LAM is set, Q = 1 for F(8) if LAM is Enabled and F(27) independent of LAM Enable.
- L(LAM): A Look-At-Me is generated at the end of the sampling sequence, if previously enabled by F(26).
- Z: Recommended after power up or power interruption. LAM cleared and disabled. Does not affect any other memory so data is preserved.

CAMAC FUNCTION CODES (All respond to A(0) only)

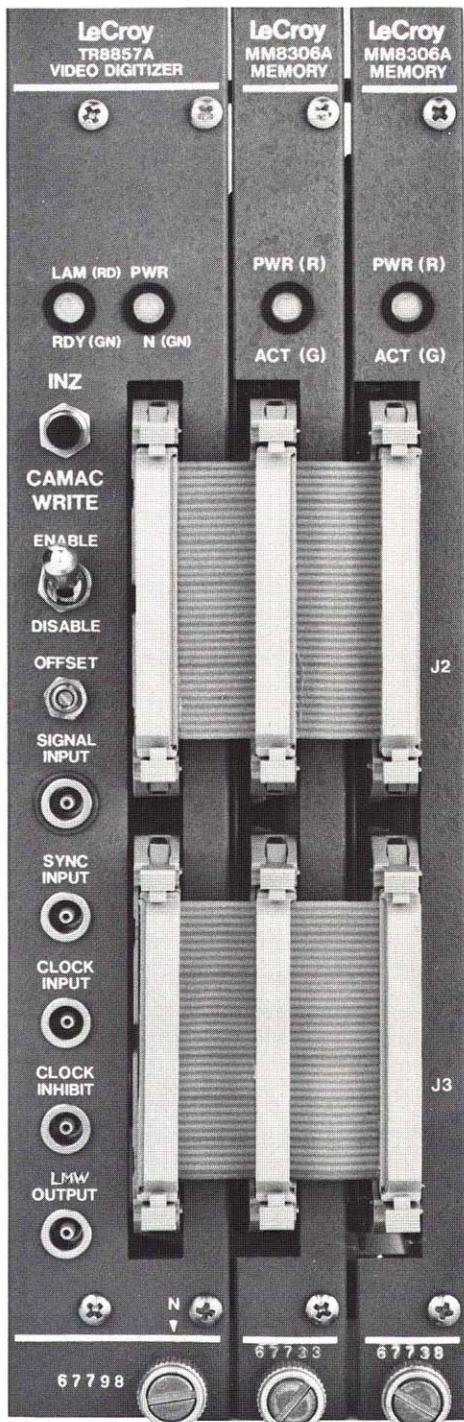
- F(0): Reads pretrigger sample size (R1-R3), sampling frequency (R5-R7) and active memory size (R9-R11):

R3	R2	R1	Pretrigger Samples	R7	R6	R5	FREQ(MHz)	R11	R10	R9	Memory Size
0	0	0	0/8 of memory	0	0	0	32	0	0	0	1K
0	0	1	1/8 of memory	0	0	1	16	0	0	1	2K
0	1	0	2/8 of memory	0	1	0	8	0	1	0	3K
0	1	1	3/8 of memory	0	1	1	4	0	1	1	4K
1	0	0	4/8 of memory	1	0	0	2	1	0	0	5K
1	0	1	5/8 of memory	1	0	1	1	1	0	1	6K
1	1	0	6/8 of memory	1	1	0	0.5	1	1	0	7K
1	1	1	7/8 of memory	1	1	1	External	1	1	1	8K

- F(1): Read single (last) sample taken (R1-R8)
F(2): Read waveform data (R1-R8). Q = 0 is returned after last word.
F(3): Read module identifier (R1-R8).
F(8): Test LAM. Q = 1 is returned if internal LAM is set and enabled.
F(9): Set unit is Ready state, Start digitizing if using Internal Clock.
F(10): Clear LAM.
F(11): Digitize Single Sample.
F(16): Write pretrigger samples (W1-W3), sampling frequency (W5-W7) and active memory size (W9-W11) as defined under F(0) above.
F(17): Enable CAMAC Read mode, disable display mode (W lines not used).
F(18): Enable Display mode, disable CAMAC readout mode (W lines not used).
F(24): Disable LAM.
F(25): Computer Stop Trigger.
F(26): Enable LAM.
F(27): Test LAM. Q = 1 is returned if LAM is set, independent of LAM enable state.

GENERAL

- Connectors: All front-panel connectors are coaxial Lemo connectors (compatible with LeCroy LE/LE-m and LE/BC-m signal cables).
- Packaging: 221 mmH, 18mmW, 292 mmD* (8.7 in x 0.7 in x 11.5 in).
*Depth front to rear panel. Rear connector 13 mm (0.5 in.) Front-panel controls approximately 20 mm (0.8 in.).
In conformance with the CAMAC standard for instrumentation modules (IEEE Standard 583, European Esone Report #EUR4100e) RF-shielded #1 CAMAC module.
- Temperature Range: Ambient operating range to maintain analog specifications; 15°C to + 35° (Requires crate with sufficient air flow to maintain exhaust air temperature of 50°C.) Data retention guaranteed to + 50°C ambient.



Models TR8857A and MM8306A Memory 50 Megasample Per Second Video/Waveform Digitizer

- **High-speed digitizing:** 50 megasample/sec
- **High resolution:** 8-bit digitizer with greater than 42 dB signal-to-noise ratio for standard video signals (0-5 MHz)
- **Manual control:** Compatible with Model 8658A Video Display
- **CAMAC (IEEE-583) packaging:** Allows interfacing to most computers
- **Modular high density non-volatile memory:** Expandable to 1 megasample (8 standard TV fields at standard resolution)
- **9th "sync" bit:** For tagging of events or for encoding video sync without using excessive dynamic range of the ADC
- **Direct Read/Write memory:** Permits redisplay of processed video data

The TR8857A, combined with the MM8306A Memory, comprises a video recording system capable of capturing successive fields or frames from either a standard video camera or specialized high scanning rate cameras. Because the entire composite video signal is digitized for redisplay, non-standard cameras may be used. This system may be operated manually with the Model 8658A Video Display or may be controlled via computer interface (CAMAC). Operating at full speed, the computer interface permits a full 128K sample field of high resolution data to be accessed in only 65 μ sec. Since the recording memory is randomly accessible for writing as well as reading, data may be read out, processed, and reloaded for display.

The Model MM8306A Memory contains 64K, 9-bit data words. A minimum of two units are required for each TR8857A and memory may be expanded in increments of 128K words to 1 megasamples. Data is written into and read from the MM8306As via a front-panel bus under control of the digitizer and separate access from CAMAC is not required.

The system's digitizing rate is determined by a clock signal applied to a front-panel connector. In video applications, the Model 8658A provides clocking for standard video rates, synchronization and generation of video frames for display on a TV monitor.

The TR8857A and its associated memory can be used for general purpose transient recording when pretrigger sampling and internal clock are not required. Applications include laser diagnostics, very long record length transient recording, automatic alignment of accelerator beams, streak camera digitization and ultrasonics.

SPECIFICATIONS

Model TR8857A and Model MM8306A

50 MEGASAMPLE/SEC VIDEO DIGITIZER AND MEMORY

ANALOG INPUT

Signal Range:	512 mV p-p anywhere within input offset range; both monopolar and bipolar signals accommodated.
Offset:	A front-panel potentiometer permits offsetting signal input with an internally generated 0 to ± 300 mV DC level. Mid-range makes the input bipolar from + 256 mV to - 256 mV; at extremes, supports monopolar signals from 0 to - 512 mV (0 is 255 counts) or 0 to + 512 mV (0 is 0 counts); nominally 30 mV/turn.
Bandwidth:	DC to 100 MHz (3 dB) for full scale input amplitudes
Impedance:	50.8 Ω $\pm 2\%$ over bandwidth
Protection:	± 25 V against 1 μ sec transients at 10 Hz rate; ± 2.5 V DC
Overload Recovery:	Output recovers to $< \pm 1$ LSB within 25 nsec for $\times 2$ overdrive.
Gain:	Accurate to within 2% of the nominal 2 mV/code. Stability is $< \pm 0.04\%$ of full scale/ $^{\circ}$ C or < 1 code/ $^{\circ}$ C.

CONVERSION CHARACTERISTICS

Rate:	A full scale conversion is complete within 20 nsec and unit may make successive conversions at any rate from DC to 50 MHz. Variable rates are not recommended.		
Resolution:	8 bits. The input signal range is divided into 256 two-millivolt steps.		
Aperture Uncertainty:	Less than 10 psec		
Dynamic Accuracy:	The ADC, sampling at 50 MHz, has the following accuracy when a reconstructed 80% full scale sinewave is compared to that produced by an ideal 8-bit ADC:		
Signal Frequency	Signal-to-Noise Ratio	Effective Bits	
DC to 5 MHz	42 dB	>7.0	
5 MHz to 12.5 MHz	40 dB	>6.7	
12.5 MHz to 25 MHz	39 dB	>6.5	

MEMORY

The Model TR8857A operates in conjunction with a minimum of two Model MM8306A Memory modules or one TV field of 512 \times 256 (416 \times 240 effective) pixels or 128K samples. The full composite video is digitized for reproduction by a model 8658A display. Capacity can be expanded in increments of two modules up to 16 memories or 8 TV fields (1 megasample). All memory management and control of the MM8306A is provided by the Model TR8857A via front-panel cables. In addition, the memory may be written into via computer (CAMAC) for storing or redisplaying processed data.

CONTROLS AND CONNECTORS

SIGNAL INPUT:	Lemo connector. See Analog Input Section for characteristics.
SYNC INPUT:	Logic level applied to this Lemo connector is stored as a 9th bit with each sample digitized. This bit may be accessed via computer or may be used automatically by the Model 8658A Video Display to generate an enhanced sync pulse. Logic options are jumper selectable to TTL or ECL with 50 Ω $\pm 5\%$ to either ground or - 2 V.
CLOCK INPUT:	An external clock (positive going transition) applied to this Lemo connector causes digitization and storage provided digitizing is enabled and Clock Inhibit is not asserted. 0 to 50 MHz clocking rates are permitted; see Sync Input for logic options.
CLOCK INHIBIT:	Logic level applied to this Lemo connector disables or enables the Clock Input. See Sync Input for logic options.
LMW OUTPUT:	ATTL output pulse is provided at the end of digitization and memory is full; for use with Model 8658A Video Display; Lemo connector.
External Display Port:	On rear panel. Provides sequential memory access, one sample at a time, for display purposes; compatible with Model 8658A. The display clock is applied to this connector (but not during data acquisition) to step through the memory. Display rates of up to 8 MHz are permitted. Format is 9 bits TTL.
Front-Panel LED's:	The External Port is automatically enabled following digitization, on power up, or via computer control. Disabled via computer control or when digitizing is enabled. PWR/N: Lit RED when all voltages are sensed (excluding internally generated references), although not necessarily within tolerance; pulsed GREEN to indicate module is addressed via N line. RDY/LAM: Lit GREEN when ready to digitize; Lit RED when conversion is complete and LAM is asserted.

INZ pushbutton:	Provides manual control of the TR8857A. Only active when CAMAC WRITE front-panel switch is in "disable" position. When used with 8658A, depressing INZ followed by manually ARMing the 8658A automatically acquires and displays video (i.e. full manual control of video recording and playback).
CAMAC WRITE ENABLE/DISABLE:	Enables or disables the capability of modifying memory contents via computer (CAMAC) control. When disabled, INZ is active and Q = 0 is generated for prohibited commands.
CAMAC CONTROL	
Readout:	Readout may proceed at the fastest read permitted by CAMAC (about 1 megaword/sec or 2 megasamples/sec) after digitization has completely filled the memory.
Data:	Offset binary plus sync bits. Each data word represents two samples. See Read Data, and Read Formatted Data below under Function Commands.
Common Control:	CAMAC provides several common busses for controlling instruments. These lines are implemented as follows: Clear Line (C): Not used. Inhibit Line (I): Not used Z Line: Receipt of a CAMAC Initialize "Z" in conjunction with the S2 strobe has the same effect as power-on-reset: LAM is cleared and disabled, and display mode is enabled. Data Memory is not cleared.
Status:	CAMAC provides several means of detecting an instrument's status. These are implemented as follows: LAM: If enabled, a Look-At-Me level is generated at the end of the sampling sequence or as a consequence of issuing a Disable Digitize command. This maskable signal may be detected directly or indirectly via function commands to determine whether new data is ready for readout. LAM is cleared by function command or by re-enabling digitization. X: As an acknowledge, X = 1 is generated as a response to function commands which are "recognized" but not necessarily enabled for this instrument. Q: As an indicator that the intended operation has been successful, a Q = 1 is generated in response to function commands which are both acknowledged and enabled. This status indicator may also be used in conjunction with a specific function command to determine the internal state of an instrument (e.g. the status of LAM may be tested using the function command F(8)•A(0)).
FUNCTION COMMANDS	
Read Status and ID:	F(0)•A(0) reads a 16-bit word (least significant bit is R1, etc.) consisting of the status of the digitizer system and the jumper programmable ID bits. R1 = Digitizer Ready Status (1 = Ready) R2 = Display Status (1 = Enabled) R3 = Power Status (1 = Failure) R4 = CAMAC WRITE Disable Status (1 = Disabled) R9-R16 = 8-bit module ID set by internal jumpers.
Enable Digitize:	F(9)•A(0) enables unit to accept clock pulses (READY to digitize); should be preceded by Set Write Address.
Disable Digitize:	F(25)•A(0) stops the digitizing sequence, disables the digitizer (clears READY) and sets the LAM. Once the system is enabled, unless digitizing completes, this is the only way to regain control of the digitizer.
Read Current Address:	F(1)•A(0) reads the current system address for memory access. For Data Write operations, this address is the address of the next memory location to be written. For Data Read operations, the address returned is the address for the next read plus the constant "5" (since read operations are pipelined four deep). The address is returned on R1 to R19. Note addressing is by words, or pairs of samples.
Set Read Address:	F(16)•A(0) enters the starting address and enables Read Mode. Uses W1 to W19. This command should be preceded by Disable Video Display.
Read Data:	F(2)•A(0) reads an 18-bit data word at the current system address and then increments the address by one. Two 8-bit samples plus two "sync" bits are packed together in the following way: R1-R8: 8-bit digitized result for sample 2n(n = 0,1,2 . . . memory size/2). R9-R16: 8-bit digitized result for sample 2n + 1 (i.e., 1,3,5 . . .). R17: Sync bit for sample 2n above (corresponds to data on R1-R8). R18: Sync bit for sample 2n + 1 above (corresponds to data on R9-R16). Requires Set Read Address prior to execution. Q = 0 is returned if the system address has advanced beyond installed memory.
Read Formatted Data:	F(3)•A(0) is used to compress the format described above (Read Data) into 16 bits for convenience in 16-bit computer systems. Sample appear in R1-R8 and R9-R16 as above but the code "0" is reserved to indicate the sync bit was set. Underflows, normally represented as "0" are represented by "1". A sync bit value of 0 will not affect the corresponding ADC data, therefore the dynamic range of the ADC is not reduced significantly (from 256:1 to 255:1). The first operation of this type must be preceded by issuing Set Read Address.

Set Write Address:	F(17)•A(0) enters the starting address and enables Write Mode. Uses W1 to W19. This command should be preceded by Disable Video Display.
Write Data:	F(18)•A(0) writes W1-W18 at current address. The current address is automatically incremented after each write operation. The first operation of this type must be preceded by a Set Write Address.
Enable Video Display:	F(19)•A(0) causes the digitizer to enter display mode.
Disable Video Display:	F(11)•A(0) causes the digitizer to quit Display Mode.
Enable LAM:	F(26)•A(0) enables the Look-At-Me.
Test Internal LAM:	F(27)•A(0) may be executed at any time to determine the status of LAM (i.e., independent of LAM enable/disable).
Clear LAM:	F(10)•A(0) clears Look-At-Me register.
Disable LAM:	F(24)•A(0) disables Look-At-Me.
Test LAM:	F(8)•A(0) will check status of Look-At-Me Line. Q = 1 is returned if external LAM is on (i.e., LAM both set and enabled).

GENERAL

Power:	TR8857A: 1.6 A at + 6 V; 1.8 A at - 6 V; 0.2 A at + 24 V; 0.1 A at - 24 V. MM8306A: 2A at + 6 V. In the event that CAMAC power is interrupted, memory circuits on the MM8306A are automatically battery backed up. A long life Lithium Thionyl Chloride battery is used. This battery provides more than two years of battery backup and has shelf life greater than five years. Data is retained, but cannot be accessed, nor can the digitizer be operated, under data back-up power. When correct voltages reoccur after power failure, the unit automatically becomes fully operational. Power-on-reset insures that the digitizer wakes up in the "Display" mode.
Packaging:	TR8857A: CAMAC #2 module. MM8306A: CAMAC #1 module. Operating ambient air Temperature Range is 15°C to + 35°C (data retention guaranteed over this range). Sufficient airflow must be provided by the CAMAC crate to ensure the exhaust air temperature is below 50°C.

SPECIFICATIONS SUBJECT TO CHANGE

Multichannel Analysis And Nuclear Spectroscopy Concepts

Multichannel Analyzer Systems

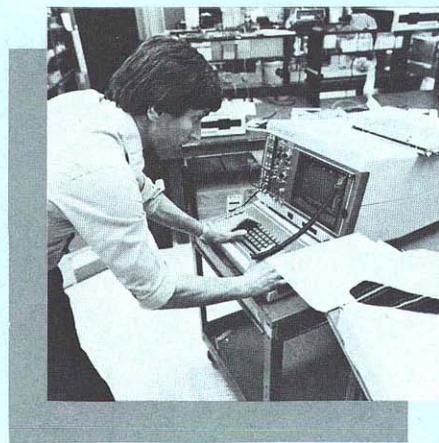
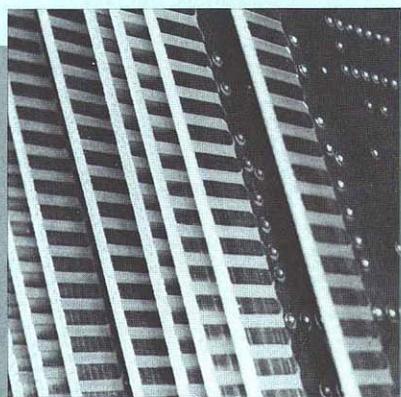
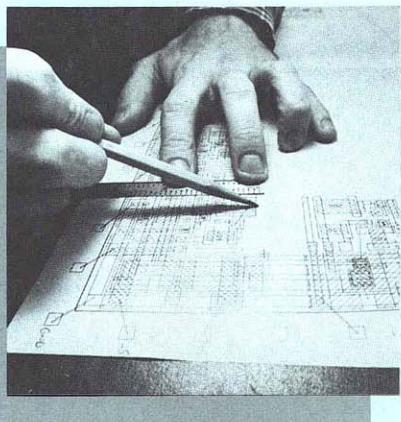
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Multichannel Analyzer Systems

Introduction

A multichannel analyzer system is a special purpose computer with dedicated facilities for acquisition of data from a variety of input sources; storage of that data in a random access memory; display of memory contents on a graphics CRT for visual interpretation of data; analysis functions to smooth, add, strip, and overlay data; functions to permit expansion of the memory display for detailed examination of individual channels or regions of memory; and, finally, a means for providing hard copy outputs of the analyzed and stored data. A multichannel analyzer is an essential part of experimental systems that are used for measuring event energies from alpha, beta, gamma, and X-ray sources, for analyzing time distribution events, and for recording changing count rates. The principal advantage of a multichannel analyzer in these counting applications is the ease and convenience of accessing and outputting data. During data acquisition, the data can be observed on a display to monitor the experiment as well as to change setup parameters. The versatility of a multichannel analyzer lends itself to a variety of experiments in pulse height analysis, time interval analysis, and time versus count rate analysis. These are the three principal multichannel analysis modes and require the use of three distinct types of input modules to convert input data to the proper form for memory storage and display.

Pulse Height Analysis

Nuclear spectroscopy pulse height analysis is one of the most common applications of a multichannel analyzer. In gamma spectroscopy applications, the gamma-emitting ra-

dionuclide can be identified by its characteristic discrete energy line or lines. Gamma emission is detected by a sodium iodide or germanium detector whose output is amplified and shaped such that the characteristic gamma energy or energies will produce an output current pulse proportional to the detected energy of the event. The current pulse is digitized by a spectroscopy analog-to-digital converter (ADC) to generate a digital word whose value is proportional to the energy of the event. The digital conversion becomes an address to a unique memory location (channel) in the multichannel analysis system. Each event addresses a channel location and increments the contents of the location by one. When measuring a statistically significant number of such events, a spectrum corresponding to the energy distribution from that radionuclide is accumulated in memory. Count values in each channel represent the total number of events of energy corresponding to that channel value. Figure 1 shows the spectrum of Cesium 137 detected by a sodium iodide de-

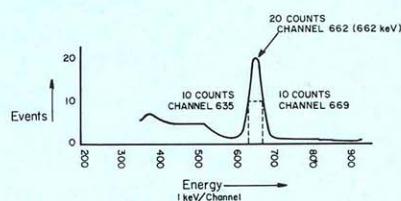


Figure 1

tector. Cesium has a characteristic gamma energy of 662 keV, but the detection process produces statistical distribution of digital addresses around the address corresponding to the primary energy. This is mainly due to photoelectron response variations within the photomultiplier tube itself. The lower energies characterize the Compton edge and back-scatter peak, which are due to Compton interactions within the sodium iodide crystal. These exhibit a

continuum of energies rather than a single energy such as produced by a photoelectric interaction within the crystal. The width of the Gaussian distribution corresponding to the photopeak is a measure of the resolution of the detector. Typically, for a 3 x 3 inch sodium iodide detector, the expected resolution of the photopeak is approximately 7-8%. The 7-8% figure derives from a measurement of the full width of the photopeak at half maximum as a percentage of the peak value. In this example, the center of the photopeak is at Channel 662, while the full-width-half-maximum values lie at Channels 635 and 689, respectively. The difference is 53 channels, which is 8% of 662 channels. If the energy scale is calibrated such that a 1000 channel display represents 1 MeV of energy (1 keV/channel), one could easily identify other photopeak energies falling within this range by determining the centroid value of each peak. From that information, the radionuclide present in the sample could be identified.

Time Distribution Measurement

Many multichannel analyzer applications require the measurement of time distributions between a START event and a STOP event. There are two ways to obtain this information; one is to use a time-to-time converter in which the START event begins the charging of a capacitor and each STOP event stops the charge. The amount of charge stored in the capacitor is then proportional to the time interval. The peak value of the capacitor output is then digitized by an ADC, and addressed to a channel corresponding to the amplitude of the input. Each pair of START/STOP events is thus digitized and histogrammed in the multichannel analyzer memory. The result is a distribution of the time interval be-

tween the START and STOP event.

Another way to achieve the same result is with a time-to-digital converter, which essentially contains a time-to-amplitude converter and an analog-to-digital converter. The advantage is lower cost and often higher START/STOP acceptance rates. Figure 2 shows a sample time distribution from a fixed time difference pulser.

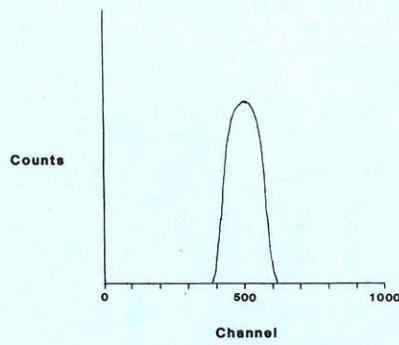


Figure 2

The result is a histogram of this time interval. The START pulse time corresponds to Channel 0, while the centroid of the STOP pulse distribution corresponds to Channel 500. In this example, the full scale range of 1000 channels is calibrated to 1 msec, and the distribution of the STOP signal has a centroid at Channel 500, or 500 nsec.

Multichannel Scaling Measurements

A multichannel scaler is essentially a fast counter. The multichannel analyzer memory stores the number of events counted during some specified period. Each channel in the MCA memory acts as a separate counter with a preset time (dwell time) selected by the user consistent with the experimental requirements. For each counting interval, the count acquired by the MCS module is transferred to that channel location. The next channel address is then selected to accept count data from the next time interval.

This process continues until all memory channels have been addressed and a single sweep has been completed. The result is a time histogram of count rates at the MCS input. The distribution will appear like the digital equivalent of an analog strip chart recording from a time rate meter with some fixed time span. In multichannel scaling operations, three parameters are of prime importance: first, the maximum acceptance count rate; second, dwell time (shorter dwell time means better resolution); and finally, the deadtime between channels. Zero deadtime is described so that counts are not lost when switching from one channel to another. A useful feature in MCS applications is the ability to scan from Channel 0 to the maximum channel, then return to 0 and scan a second time to increase the statistics of the scan. In this application, it is necessary that the START signal (Channel 0) be synchronized to the input source so that equivalent data is stored in each channel on successive sweeps. Another useful feature is the ability to scan from Channel 0 to the maximum channel, then reverse the scan from the maximum channel back to Channel 0. This is called saw tooth or RAMP UP/RAMP DOWN scanning. Multichannel scaling finds application where the input count rate is changing relative to time as in measurements of the decay rate of short-lived isotopes, Mossbauer spectroscopy, or single-ion counting applications.

Analysis Functions

Analysis functions available with MCA's include add, strip, normalize, overlay, smoothing, background subtraction, calibration, and peak search.

The Add function adds two memory groups or Regions of Interest (ROI's) and displays the result, while the Strip func-

tion subtracts any two ROI's with the differences displayed. The Normalize function permits one spectrum to be normalized by some ratio, then stripped or subtracted from another spectrum. Normalize is useful in comparing two spectra that have at least one identical peak and one or more unknown peaks. Identical peaks are references upon which a ratio is determined based on the peak count. By multiplying all channels of one spectra by this ratio, the spectra will be equivalent in count value when a strip or subtract operation is performed. The result is that the reference peak, upon which the ratio is determined, will be subtracted from the resultant spectrum, and only those peaks not present in both spectra will be part of the result. The Overlay function provides a means of comparing two spectra by direct visual comparison. The Smooth function is used in applications where insufficient data has been acquired to optimize statistics in each channel. Smoothing averages over a specified number of channels (3, 5, 7, or 9) and displays the average in the middle channel of the range. Every channel is progressively averaged in this way to smooth or average out statistical variations.

In typical pulse height analysis counting applications, the distribution of counts over the full spectrum has a background content due to cosmic rays, radiation emanating from the shielding of the detector, or spurious counts within the detector itself. During quantitative analysis of special data, it is necessary to subtract background constituents to permit more precise determination of the activity of samples of interest.

Calibration

Calibration is the technique of assigning a desired unit value to each channel over some range of channels for

direct reading of the calibration unit instead of channel number. Calibration is typically expressed in units of energy, time, or distance. Once a memory group is calibrated, every channel in that memory group will be displayed in its calibrated unit to simplify interpretation of the experimental results.

Peak Search

Pulse height analysis experiments routinely require location of all peaks in a spectrum for isotope identification. This is done by expanding the spectrum and manually searching for the peaks. As each peak is searched, a Region of Interest can be defined around it for later recall or output.

LeCroy provides an automatic peak search facility in its 3500 MCA System. This unique system automatically searches the spectrum for peaks based on some criteria, defines a region of interest about the peak, subtracts background from the peak, and produces a report which defines the peak number, the centroid value, the left and right cursor values, the peak count, the full-width-half-maximum, the total area, and the net area. In addition, the report contains the relative abundance of each peak as a ratio of that peak's net area to that of all peak areas. The peak search facility enables the user to enter the desired significance of peaks relative to background and enter the expected peak width. By entering these values, the user can exclude insignificant peaks and backscatter peaks. For each valid peak found, the background constituent of the peak is calculated based on fitting the background level to a quadratic function, then subtracting this total peak area to determine the net peak area. On completion of a peak search operation, a report can be automatically generated on either of two LeCroy hard-copy devices or on a standard line-printing device.

Regions of Interest

In multichannel analysis applications, experimenters are often interested in only specified portions of the energy or time spectrum accumulated in memory. These special regions are typically called regions of interest. In an MCA, it is useful to define regions of interest for purposes of expansion of the spectrum encompassing that region, analysis of that region with respect to other regions, and finally, output of only that data within the region of interest. System 3500 has the ability to define up to 256 separate regions of interest. Each region is defined by setting a cursor to the lower channel limit of that region and a separate cursor to the upper limit of the region, then depressing a pushbutton. This operation expands those channels within the region to cover the full horizontal axis of the CRT display and also assigns a number to that region. When multiple regions are assigned, the region number is indexed in the order of the assignment. Regions can be of any size up to the limits of the size of the memory group. They can overlap one another, or lie within one another.

User Analysis Programming

With the advent of micro-computer-based analyzers, such as the System 3500, multichannel analyzers can now be configured to operate as completely programmable general purpose computers, with minimal added hardware.

Multichannel Analyzer Components

Introduction

A typical MCA system consists of an Analog-to-Digital Converter, Memory, Control, Video Display, and Remote Storage. Storage media include hard copy printout and magnetic disc and tape storage.

Analog-to-Digital Converters

An integral part of all MCA systems is a spectroscopy Analog-to-Digital converter (ADC). Each input signal from the detector is digitized by the ADC to generate a digital word whose value is proportional to the amplitude and, therefore, proportional to the energy of the event.

The resolution of an ADC is the number of digital values into which a range of values can be divided. For instance, LeCroy's Model 3511 has a 0-to-8-V input range which can be digitized into up to 8000 separate digital values. Therefore, each digital value (or channel address) corresponds to a 1 mV difference in input amplitude. Another important parameter of the spectroscopy ADC is conversion time; the time that it takes to digitize the analog input and make the digital word available for transfer to memory. Since only one event can be accepted for digital conversion at a time, a shorter conversion time sooner frees the ADC to accept a subsequent event.

A useful feature of an ADC is a coincidence, anti-coincidence gating capability in which the peak detector is disabled unless a gate input is coincident with the signal. Another is a strobe capability in which a slowly varying AC or DC level input to the track-and-hold circuit can be periodically strobed to convert the level being tracked at the time to a strobe input.

It is convenient to have the ability to cascade several ADC's to reduce overall system dead time. Cascade operation requires provision for data transfer only when an ADC is ready. For instance, LeCroy's 3511 includes a BUSY output which provides a signal to a front-panel connector as well as to an associated deadtimer module.

Two ADC specifications important in high resolution pulse height analysis are integral and differential nonlinearities. From previous discussions, it can be seen that there is ideally a linear relationship between the energy of the event, the output amplitude from the amplifier, and the digital address derived in the conversion process from this amplitude. For example, if Channel 8000 of memory represents 8 MeV, and Channel 0 represents 0 MeV, there is a linear relationship between energy and channel number with each channel corresponding to one keV of energy. The input voltage range to the ADC is 0 to 8 V. There is, similarly, an overall relationship to 1 keV per mV per channel. Any deviation from this straight line relationship is a measure of integral nonlinearity. Integral nonlinearity is an important specification because it affects the centroid position of spectral peaks. If a complex radionuclide spectrum is being analyzed for identification of the constituents of this spectrum, poor integral nonlinearity specification may cause an error in the energy identification process.

Differential nonlinearity is defined as the maximum variation of channel width from one channel to another. To satisfy the rigid differential nonlinearity requirements of high resolution spectroscopy applications, LeCroy's technique, as characterized by the Model 3511, is to employ a sliding scale which essentially adds an analog offset to the signal of the ADC circuit and subtracts the digital equivalent of that analog voltage from the conversion result. The analog input offset is supplied by a Digital-to-Analog Converter (DAC) which is successively incremented and decremented over a range of 0 to 383. The DAC output consequently has a range of 0 to 383 mV, any value of which can be added to each input signal to the ADC.

The digital equivalent of this analog offset is then subtracted from the digital output of the ADC. The digital value of the ADC is sequentially changed so that each conversion has a different analog offset added to the input with the equivalent offset subtracted from the output. This sliding scale averaging technique enables the Model 3511 to provide better than $\pm 1\%$ differential nonlinearity over the upper 99% of a 50 mV to 8 V input range.

MCA Memory

As previously described, the memory of the multichannel analyzer stores the data in one of two ways depending on the output. In one case, the input data is a single count which is added to a channel location determined by the analog-to-digital conversion or a time-to-digital conversion. In a multi-channel scaling application, however, the addressing of channels begins at Channel 0 and sequences through all channels in memory according to dwell time selection. The count value acquired by the multichannel scaling module during each dwell time is the data which is added to the channel location currently addressed.

The process of storing data in memory consists of several steps. For pulse height analysis or time distribution operations, the first step is the transfer of the address from the module to an interface board which then reads the count value in that memory address. Next, the count value at that address is incremented. Finally, the modified count value is written back into the same memory location. Initially, all bits in memory are set to zero by a Clear Data Memory operation. This operation requires redundant steps to prevent accidental erasure of memory.

For transfer of data in multi-channel scaling operations, the count value for the channel currently being addressed is read from memory (this value is initially 0), the new count value acquired during the dwell time is added to that count value and the new count value is written into that address location of memory.

Video Display

The display is used for providing a digital representation of data stored in the histogram memory in a two-dimensional plot of counts versus channel number. Count axis is the Y-axis while channel number is the X-axis. Depending upon the type of input, the X-axis or channel number of the memory selected for the display can represent energy, time, or distance. If a time-to-digital converter is processing input from a position-sensitive detector, the X-axis would represent distance.

Figure 3 shows a typical display of two graphs in which the upper graph is a region of interest from the memory group or input displayed on the lower graph. Each graph has a title which identifies the ROI and the experiment or input. The title is entered by the user for record keeping purposes. In this example, the region of interest contains the same title as the memory group but, in addition, defines the upper graph as a region of interest and has an assigned ROI number.

In the LeCroy 3500's display system, each graph has a set of left and right cursors and a marker, as well as vertical minimum and maximum and horizontal minimum and maximum values. In addition, a time display is provided which monitors elapsed time of the experiment in one second intervals up to 100 hours. The location and count value of the marker on each graph is displayed just beneath the X-axis.

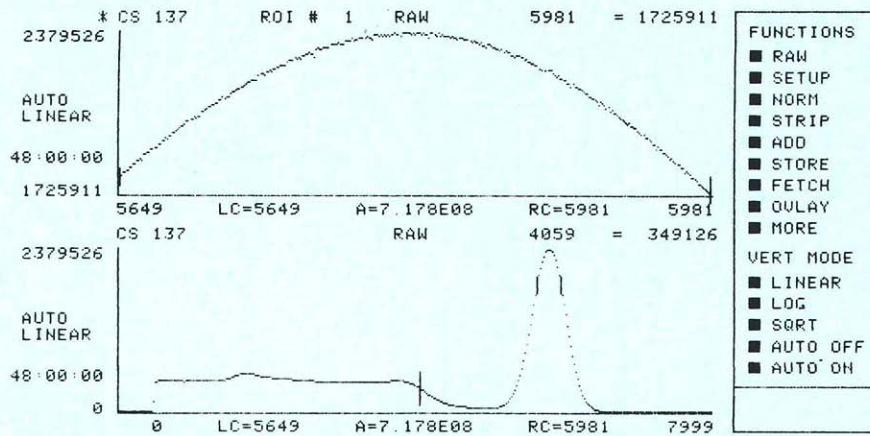


Figure 3

A vertical display mode is also displayed. Display mode choices include log, linear, and square root, with selected auto scaling in each mode. Auto scaling of the vertical axis sets the vertical maximum value to correspond to the maximum count value of all channels in that display. The vertical maximum value can display over 16,000 counts with all intervals proportionally scaled between this maximum value and the 0 value in the linear mode.

During accumulation of data, the display is active and continually updates counts in all channel locations. Once acquisition has been terminated, either manually or by preset selection, contents of the selected memory area are retained on the display for visual interpretation and analysis of the data.

In situations where two separate pulse height analysis spectra have been acquired, they can be displayed simultaneously, one appearing on the upper graph and one on the lower, to permit addition of two spectra, stripping one from the other, or overlaying one on the other.

Hard Copy Output of Channel Contents

An MCA system can output to several kinds of hard copy printers. A dot-matrix printer with both graphics and alphanumeric capability can provide

a "Screen-Dump" to preserve everything displayed on the monitor.

A digital strip-chart recorder can plot every channel, point-by-point, providing a log, linear, or square-root display with the X-axis drawn to any length. Such recorders also have alpha-numeric capability.

Magnetic Data Storage

Storage of both experimental data and the associated equipment settings, such as conversion gain and time duration used to take the data, is easily done with either magnetic diskettes or 9-track reel-to-reel tapes. Large quantities of data can be compactly filed for later retrieval, reduction and analysis.

Uniquely Appropriate Applications for Modular MCA System

Introduction

The following section contains a small sampling of the many uses of the multichannel analyzer. More detailed information concerning any of these applications is available on request from LeCroy Research Systems.

Multi-Energy Gamma Ray Automated Scanning System

The CAMAC-based, gamma

ray scanning system is used to measure the transmission through stacked attenuators of up to 16 different gamma rays, ranging in energy from 77 to 2614 KeV. These transmission measurements produce a set of linear equations which may be solved for either the thickness or the density of the discrete attenuators comprising a given stacked assembly.

The assembly of attenuators is moved in a direction perpendicular to the detector-source line by a stepping motor that is controlled by the data acquisition system (see Figure 4). At each stop, data from the source is collected by an ADC and histogrammed and stored in the multichannel analyzer.

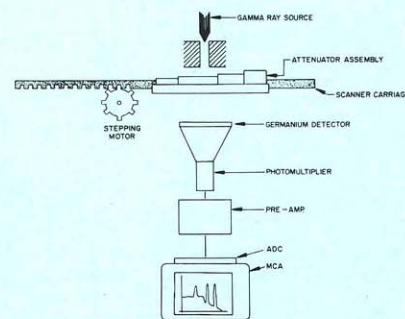


Figure 4

Each of these graphs has photopeaks (up to 16) corresponding to the various gamma ray energies of the source. After data at all the desired positions of the attenuator assembly is taken and stored, the MCA determines the area (minus background) under each peak and produces a graph like the one in Figure 5 for each gamma ray energy. This information plus knowledge of the appropriate attenuation coefficients is sufficient to set up a system of linear equations from which can be determined the densities or thicknesses of the components of the attenuator assembly.

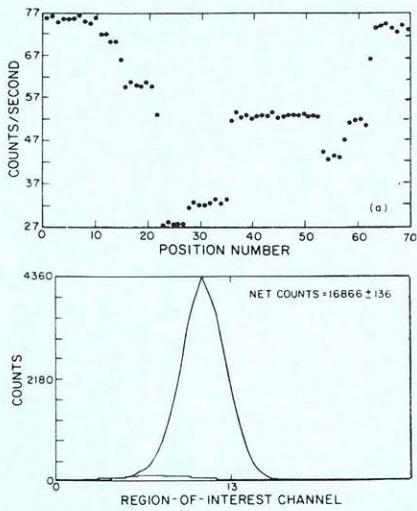


Figure 5

Gamma Camera Testing

A gamma camera is a device which gives an image of the spatial distribution of gamma rays falling on its "eye," that is, on a large diameter NaI crystal that is "watched" by an array of photomultipliers placed in concentric rings (see Figure 6). The signals from the photomultipliers are coded and combined so that four electrical signals, X, Y, W, and Z, are produced. X and Y are proportional to the x and y coordinates of the impact point of the gamma ray (the center of the "eye" is the origin of this coordinate system), W is proportional to the event's energy, and Z is a logical signal produced by a single-channel analyzer receiving W as input.

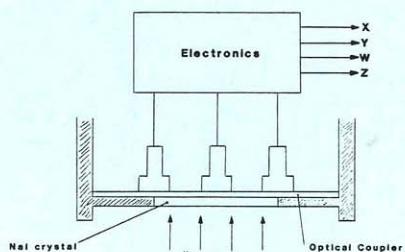


Figure 6

A multichannel analyzer can be used to test several properties of the camera.

1. Intrinsic energy resolution characterizes a gamma

camera's ability to identify and distinguish photopeaks. The W signal is sent through an ADC to a multichannel analyzer, producing a histogram characteristic of the gamma ray source being used. The full width at half maximum of the peak (or peaks) is determined, yielding a measure of the camera's energy resolution.

2. Intrinsic flood field uniformity is a measure of the uniformity of response of the camera as a function of x, y position. The X and Y signals are sent to separate ADC's, the digital outputs of the ADC's are combined into one 16-bit word, and the result is histogrammed in the MCA. The resulting graph contains one channel for each x, y position defined. The counts in each channel can be analyzed to determine the flood field uniformity.

3. Intrinsic spatial resolution characterizes the position determination accuracy of the camera. A screen called a "phantom" is placed over the camera's "eye." The screen consists of a series of narrow, parallel slits. Again, the X and Y signals are sent to ADC's, combined, and histogrammed. The widths of the resulting series of peaks produce a measure of the intrinsic spatial resolution of the camera.

Area-Imaging Proportional Counter for X-Ray Diffraction

An area-imaging proportional counter measures the energy and x, y position of an incident X-ray. The counter consists of planes of parallel wires biased at 4 to 5 kV (see Figure 7). When an X-ray photon passes through the detector, it ionizes a xenon-methane gas mixture and produces an electrical pulse on one pair of wires. This pulse in-

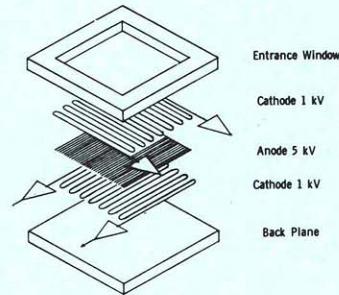


Figure 7

puts to the electronics shown in Figure 8, producing signals proportional to the x, y position and energy of the incident photon.

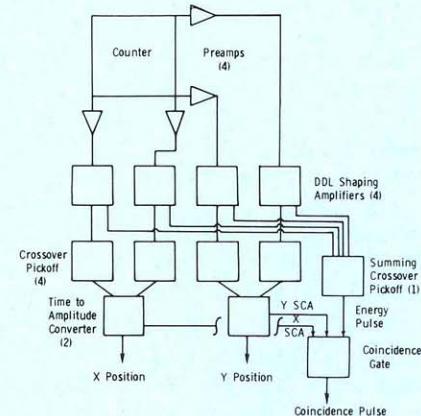


Figure 8

The x and y signals are sent to two ADC's, the outputs of which are juxtaposed to form one 16-bit word. A multichannel analyzer histograms and stores these words. Each section of the resulting graph represents one "slice of constant y" of the input data.

Plutonium Storage Vault Monitoring

Research is constantly in progress to develop methods for monitoring radioactive materials in storage. One method employs a 5×5 array of ^3He neutron detectors mounted in the ceiling of a plutonium storage vault. Each detector sends a signal to a dedicated multichannel scaler (see Figure 9). The data from all 25 scalers is sent to a multichannel analyzer where it is histogrammed and analyzed. The resulting count rate pattern is sensitive to such

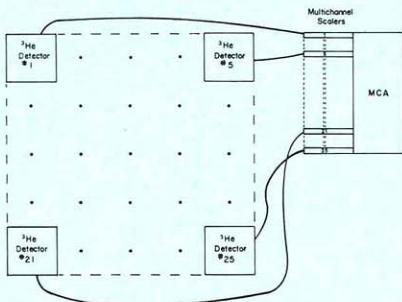


Figure 9

things as the presence of a person in the vault, the opening or closing of the vault door, and the relocation of as little as 1 kg (out of 2500 kg) of ^{240}Pu .

Coded Aperture Image Analysis

It is sometimes desirable to image (i.e., determine the shape of) radioactive sources, such as are found in nuclear waste, without opening the container. A pinhole aperture in front of a gamma-imaging device is sufficient if count rates are high enough. (This is analogous to a pinhole camera, the gamma-imaging device acts as the film.) If count rates are low, however, the image from a single pinhole may be lost in noise. To circumvent this problem, a coded aperture is used.

A coded aperture consists of many pinholes through which a source producing small amounts of radiation can cast numerous shifted images on

the imaging device. Data from the gamma-imaging device is fed to a multichannel analyzer which decodes the data and displays a true image of the source (see Figure 10).

Nuclear Waste Identification

Identification of the contents of drums and crates containing radioactive material is possible without opening these containers. One method is to bombard the drums with 8 MeV gamma rays, causing photofissioning in the nuclear material (see Figure 11). This bombardment produces neutrons whose

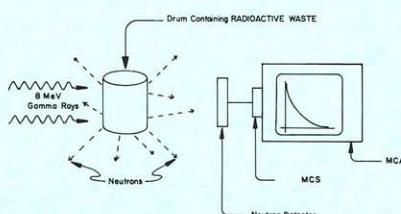
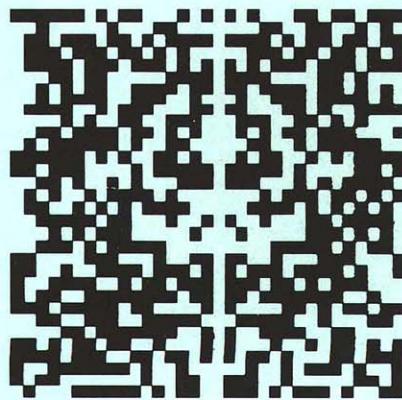
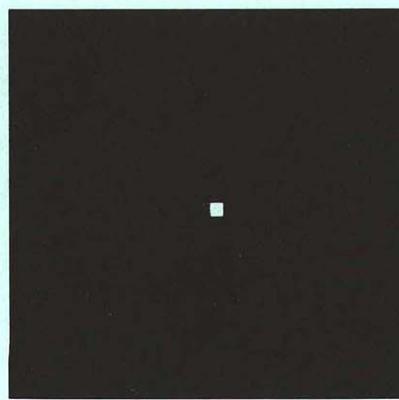


Figure 11

quantity dies away at characteristic rates. A neutron detector sends its signal to a multichannel scaler, the output of which is sent to a multichannel analyzer. The MCA stores the count rate data in histograms and calculates, from these graphs, the die away times. These are compared with known die away times and the radioactive materials are identified.



Coded Image of Simulated Point Source.



Decoded Image of Simulated Point Source.

Figure 10

Quick Reference Chart/Page Guide for Spectroscopy-Related Products

The 3512/87/88 form a High Performance Time Resolved Spectroscopy System									
Model	3511	3541	3542	3512	3587	3588	3521A	4201	4204
Function	Spectroscopy ADC	Dual ADC Deadtimer	ADC Multiplexer and Router	Buffered ADC	Time Slice Data Router	Histogramming Memory	Multichannel Scaling	Time Interval Metering (Time to Digital Converter)	Time Interval Metering (Time to Digital Converter)
No. of Inputs/Channels	1	2	8	1	1	1	1	1	16
Rate or Conversion Time	5 μ sec per 8 K Channel	N/A	18 KHz/Channel	5 μ sec/Channel	1 MHz	1 MHz	100 MHz	<1 μ sec	<1 μ sec
Capacity	8-13 Bits	N/A	13 Bits with 3511	8-13 Bits	20 Bits	24 Bits/1 per CH 16384 Channels	24 Bits	16 out of internal 24 bits	24 out of internal 32 bits
Size	1	1	3	2	2	2	1	1	2
Input Levels	0 to \pm 8 V	From 3511 or 3512	0 to \pm 8 V	0 to \pm 8 V	Compatible with 3512	Compatible with 3512	NIM/TTL	-1.5 to +1.5 V or ECL	-1.5 V to +1.5 V or ECL
Internal Buffer	NO	N/A	NO	YES	N/A	N/A	YES	YES	YES
External Memory Compatible	YES	N/A	N/A	YES	YES	N/A	YES	NO	YES
Module Compatibility	3542	3511, 3512	3511	3587, 3588	3588, 3512	3512, 3587 4204	8202	N/A	3588
Features	Peak detection or strobed sample modes	Preset time, programmable from 1 msec to 9×10^6 sec.	Two 3542s can be connected for 16 channels	List mode data for multi-parameter applications.	Programmable dwell intervals for Time Resolved Spectroscopy.	Multiple histogram setup.	<5 nsec deadtime.	Programmable offset, 157 psec resolution and overflow time and action	16 Channel multisource ECL input, programmable offset, 157 psec resolution and overflow time and action
Page	459	471	473	463	475	477	469	165	167

Also see Section I: ADC's, page 38
 Scalers, page 38
 Time Measuring Instruments, page 39

Section II: Transient Recorders/Signal Averagers, page 345

Product Guide for Multichannel Analysis and Nuclear Spectroscopy

qVt® NIM MULTICHANNEL ANALYZER
 2301, 3001, 3155, 3157, DPP-7

CAMAC MULTICHANNEL PULSE HEIGHT AND TIME ANALYZER SYSTEM
 3512/15, 3521A, 3587, 3588 (Also see 4204, page 167)

BENCHTOP CAMAC-BASED MULTICHANNEL ANALYZERS
 3500M, 3500MP, 3511/14, 3521A, 3541, 3542
 (Also see 4201, page 165)

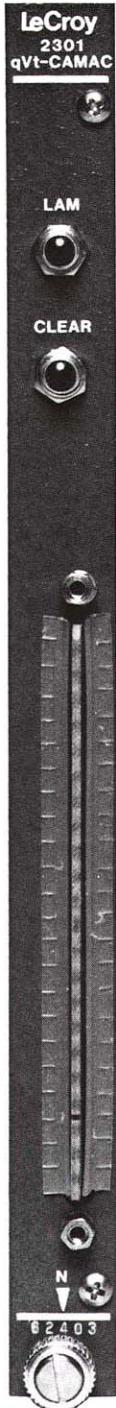
CAMAC CRATES AND INTERFACING
 CAMAC: 8013, 8901 (Also see 1434, page 73)

3500MP CAMAC Data Acquisition System
 Accessories: 3500-25, 3500-35, 3500-38
 Peripherals: 3921, 3931A, 3965
 Software: 3910-2B, 3910-15 (Also see page 479)

NIM: See 1403, page 71

TECHNICAL DATA

LeCroy



CAMAC Model 2301 Interface for qVt° Multichannel Analyzer

LeCroy's CAMAC Model 2301 qVt Interface has been designed to allow spectrum transfer to computer or to allow data transfer to the Model 3001 Multichannel Analyzer for display or histogramming. The Model 2301 allows the qVt to be used for calibration and setup as well as for display during the operation of an experiment.

The 3001 may be used to set gain and timing of hodoscope or calorimeter elements. When the first order high voltage and cable delay parameters are set, the information may be transferred to the computer for straightforward analysis *before the systems software is fully operational*. In this way, an array of gains and timing parameters may be evaluated for second order corrections.

Just as in many commonly-used minicomputers, data in the 3001 is organized into 16-bit words. The Model 2301 allows this memory to be written into from the CAMAC Dataway. The data loaded into memory is then *automatically displayed* without the need for expensive storage display or the requisite CPU time required to refresh a standard CRT.

An increment feature allows any channel of the 3001 to be incremented by 1. This feature allows use of the analyzer as a *histogram* and *display* module without significant core usage for data storage or software. Since the display is continuously active, the experimenter may watch the spectrum accumulate without significant CPU overhead.

The Model 2301 contains an Incrementing Address Register which may be loaded from the CAMAC Dataway. The value contained in the register is used to address memory for both read and write operations. After the read or write operation is performed, the register is incremented by 1. Using this scheme, data may be transferred to or from the qVt memory at the rate of 1 word per CAMAC cycle.

September 1982

SPECIFICATIONS

CAMAC Model 2301

INTERFACE FOR qVt MULTICHANNEL ANALYZER

Inputs and Outputs:	44 on a single front panel edge connector. Pin-for-pin identical to the <i>qVt</i> rear I/O connector. Mates with AMP connector 582777-1.
LAM Button:	A front-panel pushbutton sets the L level to true. Intended to allow a manual interrupt.
CAMAC Commands:	<p>Q: A Q = 1 response is generated in recognition of an F(2), F(16), F(17), or F(25) command only if a valid address (0 to 1023) is contained in the Internal Address Register. A Q = 0 response applies for all other function codes.</p> <p>X: An X = 1 (Command Accepted) is generated when a valid F and N is received.</p> <p>L: An L = 1 Look-At-Me signal is generated by pressing the front-panel LAM Button. The condition persists until an F(2) is received.</p>
CAMAC Function Protocol:	<p>F(2) Read <i>qVt</i> data. Requires N, S1 and S2. Loads <i>qVt</i> data from the channel whose address is in the Incrementing Address Register to Dataway lines R1 to R16. Advances the Incrementing Address Register by one.</p> <p>F(9) Clear <i>qVt</i>. Requires N, S1 and S2; clears all 1024 memory locations in the <i>qVt</i>.</p> <p>F(16) Write into <i>qVt</i>. Requires N, S1 and S2. The data contained on the Dataway lines W1 to W16 are written into the memory channels whose address is in the Incrementing Address Register. Advances the Incrementing Address Register by one.</p> <p>F(17) Write into Incrementing Address Register. Requires N, S1 and S2. The data contained on the Dataway lines W1 to W10 are written into the Incrementing Address Register.</p> <p>F(24) Stop <i>qVt</i>. Requires N, S1 and S2. Issues a <i>STOP</i> command to the <i>qVt</i>.</p> <p>F(25) Increment <i>qVt</i>. The data in the address contained in the Incrementing Address Register is incremented by 1.</p> <p>F(26) Start <i>qVt</i>. Requires N, S1, and S2. Issues a <i>START</i> command to the <i>qVt</i>.</p>
Packaging:	In conformance with CAMAC standard for nuclear modules (ESONE Committee Report EUR4100e). RF shielded CAMAC #1 module.
Current Requirements:	+6 V at 500 mA.

SPECIFICATIONS SUBJECT TO CHANGE

TECHNICAL DATA

qVt®



LeCroy

NIM Model 3001 Multichannel Analyzer

The Model 3001 is a research grade multichannel analyzer which provides exceptional versatility at relatively low cost. The Model 3001 features:

- **3-Mode Analysis**—Charge (Q, area) and voltage (V, peak) analog-to-digital conversion and time-to-digital conversion (T, start/stop) modes mean direct compatibility with photomultiplier anodes and elimination of charge-sensitive preamps and time-to-amplitude converters (TAC's).
- **High Sensitivity**— $Q = 0.25 \text{ pC}$ sensitivity in charge mode, $V = 1 \text{ mV}$ resolution in peak mode (0 to 1 or 0 to 10 volt inputs), and $T = 100 \text{ psec}$ resolution in time mode mean direct compatibility with low-level signals from a variety of sources and the ability to precisely measure short time intervals.
- **Segmentable Memory**— 4×256 (quadrants) or 1×1024 (full scale) gives the flexibility to accumulate, display, and compare up to four different spectra or to display quadrants of a full 1024-channel spectrum.
- **High Count Capacity**— $2^{16} - 1$ (65,535) counts capacity permits enough data accumulation to satisfy applications including cosmic ray and high energy experiments and many nuclear spectroscopy and Mossbauer applications.
- **Nanosecond Logic Functions**—Internal triggering mode permits the 3001 to be used as a stand-alone device, while the external modes permit either internal gate generation upon application of an external trigger, or direct application of an external gate signal.
- **Choice of I/O**—Interfaces, through accessory modules, to an X-Y plotter, line printer, or the CAMAC dataway.
- **Compact Packaging**—Complete 1024-channel analyzer, compactly packaged in a #2 NIM-standard module, gives greater portability, lower cost, and enhanced reliability.
- **Versatile Display**—Highly accurate digitally derived logarithmic and linear display permits viewing the memory content at optimum amplitude resolution.
- **Drives Any X-Y Scope**—The use of the 3001 with any external X-Y scope in your lab means smaller basic analyzer size, greater mobility, and saves you the expense of a built-in scope which you may already have available.

February 1983

GENERAL DESCRIPTION

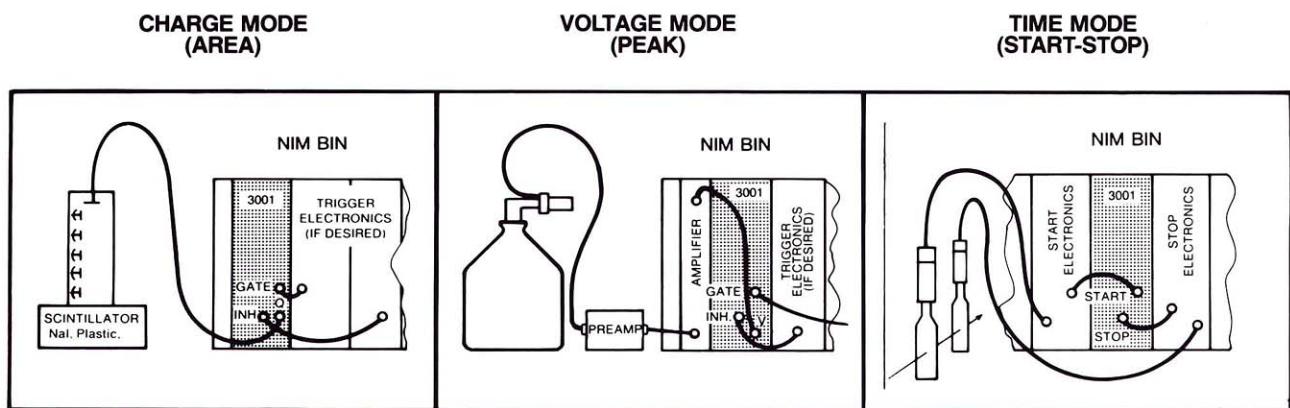
The Model 3001 is a new, low cost, 1024-channel multichannel analyzer offering three analysis modes: charge (area), voltage (peak), and time (start/stop). Packaged as a double-width NIM module, it is significantly more compact than even the smallest analyzers previously available. Each of the 3001's 1024 channels has a count capacity of 16 bits (65,535). The contents may be displayed in log/linear fashion on any X-Y oscilloscope. The display is active on a time-available basis, thus affording display during data accumulation. A front-panel switch selects intensification of every tenth or fiftieth channel. Data may be accumulated and displayed in selected 256-channel quadrants or in the full 1024-channel memory. In addition to both an internal and external trigger capability with variable gate width, the 3001 provides external gate and inhibit inputs, which are also used as start and stop inputs in the time mode.

Rear-panel digital outputs are supplied to allow for data transfer to interface options including a readout device (e.g., printer) or a CAMAC Dataway. The output connector may also be used to load or increment any one of the 16-bit words in memory. This feature allows the 3001 to be used as an additional 1024 words of memory and to act as a histogram display module.

The 10-bit ADC used for the Q (charge) mode has a sensitivity of 0.25 pC/channel, directly compatible with photomultiplier anodes pulses, thus obviating the need for a charge-sensitive preamplifier. In the Q mode, the input current is integrated for a duration ranging from 10 nsec to 1 μ sec. A front-panel-adjustable internal gate is generated by either an internal or an external trigger, or an external gate pulse may be directly applied to the MCA. Operating in the Internal mode, the Model 3001 is a stand-alone device, possessing an internal discriminator of 1 mV minimum threshold. The Q input is terminated in 50 Ω and all analog circuitry is dc-coupled, thus eliminating the need for dc restoration instrumentation.

The 10-bit TDC used for the T (time) mode of the Model 3001 digitizes time intervals by the start-stop technique and stores their spectra. Full-scale time intervals are 102 nsec and 1024 nsec, offering respective resolutions of 100 psec/channel and 1 nsec/channel. The start and stop inputs are leading edge triggered, responding to fast NIM (negative) signals. Uses of the T mode include time of flight, counter timing, and delay measurement, β - γ time correlation spectra, and drift chamber calibration.

In the V (voltage) mode, the output of any voltage source, e.g., a charge-sensitive preamplifier, may be analyzed. The maximum (peak) voltage (of signals > 50 nsec risetime) applied to the input during the gating interval is digitized, thus making external stretching circuits unnecessary. The full-scale input in the V mode is +1 volt (+10 V is switch selectable), offering a resolution of 1 mV (10 mV) consistent with that of a Si(Li) detector. The internal gate may be extended to 5 μ sec in this mode.



For direct digitizing of photomultiplier anode current pulses. No charge-sensitive preamp is required, permitting high counting rates and pile-up elimination.

For use as a conventional Pulse Height Analyzer. Accepts positive voltage signals or dc levels.

For Start-Stop timing measurements. Not multiscaling. No TAC necessary.

SPECIFICATIONS

NIM Model 3001

qVt MULTICHANNEL ANALYZER

GENERAL OPERATIONAL CHARACTERISTICS

Analysis Modes:	Q: Current integrating (charge sensitive); integration interval 20 nsec to 1 μ sec; full scale, 256 pC \pm 10% sensitivity, 0.25 pC/channel.
	V: Peak voltage; input signal risetime, \geq 50 nsec; full scale, + 1 volt or + 10 volt \pm 10%; resolution, 1 mV or 10 mV/channel; external gate width, 100 nsec minimum to 1 μ sec or switch selectable 5 μ sec maximum.
	T: Time interval (Start/Stop); full scale internally switch-selectable, 102 or 1024* nsec \pm 10%; resolution, 100 psec and 1 nsec respectively.
Number of Channels:	1024 (10-bits); 256 (8-bits) in quadrants; overflow counts are stored in the last address of the selected memory segment.
Memory Size:	16 bits – 1 per channel (65,535 counts).
Digitizing Time:	12 μ sec + 0.05 μ sec/channel.
Temperature Stability:	\pm .03% of full scale/ $^{\circ}$ C.
Long-Term Stability:	\pm 0.2% of full scale/week, maximum.
Integral Non-linearity:	\pm 0.25% of reading \pm 2 channels.
Display:	100 sweeps/second
Channel Intensification:	Every 10th or 50th channel, front-panel selectable.

PHYSICAL CHARACTERISTICS

Packaging:	#2 width, RF-shielded NIM-standard module, conforming to specifications outlined in AEC Report TID-20893.	
Voltages Used:	\pm 24 volts, \pm 12 volts (Note: a rear-panel switch permits operation from \pm 6 volts (if available) instead of \pm 12 volts.)	
Current Requirements:	+ 24 V at 24 mA + 12 V at 06 mA + 6 V at 1.35 A	- 24 V at 125 mA - 12 V at 127 mA - 6 V at 510 mA
	Note: \pm 6 V requirements add to \pm 12 V requirements when \pm 6 V option is unused.	
Front-Panel Connectors:	BNC.	

INPUT CHARACTERISTICS

Analog Input (Q and V Modes):	Direct-coupled; impedance, 50 Ω optionally, 93 Ω in V mode; protected to \pm 100 volts for 1 μ sec; linear range, 0 to -1 volt in Q mode, 0 to + 1 volt in V mode.	
External Gate/External Trigger/Start/Internal Gate View:	One Common front-panel connector; functionally controlled by trigger mode switch; requires -600 mV signal into 50 Ω . Q and V Modes: In External Gate (EXT. GATE) mode, the gate width is equal to the duration of the gate pulse applied to this connector. In External Trigger mode (EXT. TRIG), the internal gate is triggered by the leading edge of a fast NIM signal applied to this connector (min. trigger width, 10 nsec). In Internal (INT) mode, the internally-generated gate may be viewed at this connector. Amplitude \sim 100 mV. Q Mode: Usable gate duration, 20 nsec to 1 μ sec. V Mode: Minimum duration, 100 nsec. Maximum duration, 5 μ sec. (Gate must enclose peak of input signal to be measured.) T Mode: The leading edge of Start input begins the start-stop time measurement; minimum pulse width, 10 nsec. External trigger mode only.	
Inhibit/Stop:	One common front-panel connector; requires -600 mV into 50 Ω . Q and V Modes: Conversion is inhibited by application of a NIM inhibit signal. This level must be established before, and persist at least 20 nsec after the leading edge of the gate trigger. Inhibit is ignored after conversion is begun. T Mode: Leading edge of stop pulse terminates the interval measurement; minimum pulse width, 10 nsec.	

FRONT PANEL CONTROLS

Gate Width

Front-panel multiturn gate width control for Internal and External Trigger mode operation with range of 20 nsec to 1 μ sec (5 μ sec switch-selectable in longer time range). Setting stability \pm 1% or 1 nsec, whichever is greater. Output monitors permit switch-selectable viewing of internal gate pulse for precise adjustment. Lower level discriminator triggers internal gate.

* Range 120 to 1120 nsec.

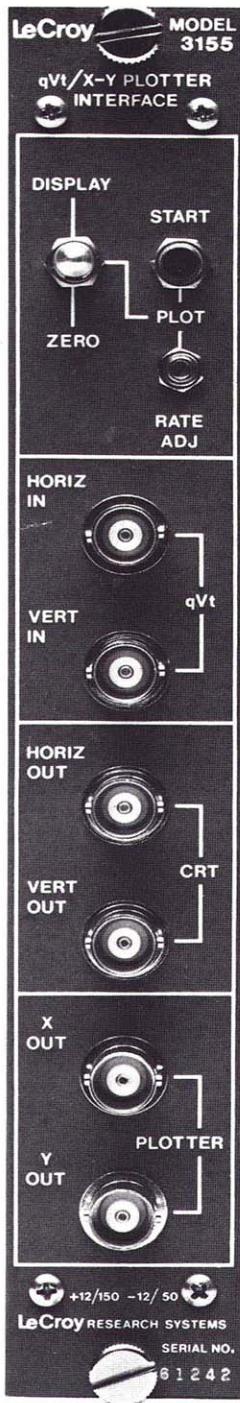
Threshold:	Front-panel screwdriver-adjustable potentiometer determines threshold setting in internal trigger (INT) mode. Range, -1 mV to -15 mV in Q mode, +1 mV to +15 mV in V mode. Front-panel monitor point gives output voltage equal to 1000X actual threshold setting. Threshold stability < 0.2%/°C over 20°C to 60°C operating range.			
Operating Mode:	One of the three analysis modes (Q, V, or T) is selected by a 3-position switch.			
Trigger Mode:	A 3-position switch selects internal trigger operation (INT), External Trigger operation (EXT TRIG), or operation via an externally-applied gate pulse (EXT GATE).			
Continuous/Stop at Overflow:	A 2-position switch either permits continuous data collection and display or limits each channel to a full scale capacity.			
Intensify:	Either every 10th or every 50th channel is intensified on the display, determined by a front-panel 2-position switch.			
Display LIN/LOG:	Selects linear or logarithmic display.			
Start/Stop:	Front-panel two-position, spring-return toggle switch. Start position initiates new measurement cycle after a Stop or Clear. Stop position stops measurement cycle.			
Clear:	Front-panel spring-return toggle clears all memory and register. Start/Stop switch must be simultaneously placed in stop position.			
Memory Select: Full-1/4-2/4-3/4-4/4	In the Full position, all 1024 channels accept and display input data. In the 1/4 position, the first quadrant (256 channels) accepts and displays input data. Full-scale range settings remain the same (i.e., 256 pC, +1 volt, and 102 or 1024 nsec); similar for 2/4, 3/4, 4/4.			
Vertical Gain:	In LIN (linear) mode, an 8-position switch selects a maximum number of counts to be displayed per channel, between 512 and 65 k.			
FRONT PANEL INPUTS				
Q Input:	Analog input; 50 Ω impedance; dc coupled. Accepts input charge of 0 to 256 pC. Protected to ± 100 volts.			
V Input:	Analog input 50 Ω impedance (93 optional). Accepts input voltage of 0 to +1 V (with switch selection 0 to 10 V range). Protected to ± 100 volts.			
Gate Input/Output:	Multifunctional connector. Acts as trigger or gate input/output in Q or V mode. Acts as start input in T mode. Input impedance 50 Ω. Accepts NIM fast signals. (See detailed specifications.)			
Inhibit/Stop	Accepts fast NIM signals. Acts as inhibit in Q or V mode and stop input in T mode. Impedance 50 Ω.			
FRONT PANEL OUTPUTS				
Threshold Test Point:	Reads 1000X preset threshold value in Internal mode operation.			
Internal Gate View:	Internally generated gate is available for oscilloscope monitoring on the Gate Connector when Internal Trigger is selected. Amplitude: -100 mV.			
Internal Gate Test Point:	Internally-generated gate is available for oscilloscope monitoring when Internal or External Trigger mode is selected. Amplitude: -200 mV.			
Busy:	TTL low level output during conversion time.			
Horizontal Out:	Horizontal deflection voltage for CRT proportional to channel number; 0-5 volts for full or quadrant display. Minimum load impedance 1 kΩ.			
Vertical Out:	Vertical deflection voltage for CRT proportional to number of counts. Linearity ± 0.2% of full scale. Full-scale output of 5 volts corresponds to 200 db/volt in the log mode. Minimum load impedance 1 kΩ.			
REAR PANEL OUTPUTS				
Connector Type:	44-contact card-edge connector; mates with AMP 582358-2 (hood number 530087-4).			
Memory Overflow (22):	A high TTL level* indicates channel overflow. Available during memory load only.			
External Enable (4):	Low TTL level* enables external functions accessed by the rear connector.			
External Memory Address Latch (R):	The trailing edge of a positive-going TTL-compatible* pulse of minimum duration 200 nsec. latches the address applied to the 10 Memory Address lines (A,B,C,D,E,F,G,H,J,K,L), corresponding to 2 ⁰ to 2 ⁹ respectively.			
Memory Enable (21):	TTL-Compatible high level* causes the contents of the memory address latched in lines A-L to be loaded into the internal incrementing register. A low level permits loading of the 16-External Data Input levels** into the Incrementing Register.			
*Pin 6 : 2 ⁰ Pin 10 : 2 ⁴ Pin 14 : 2 ⁸ Pin 18 : 2 ¹² 5 : 2 ¹ 9 : 2 ⁵ 13 : 2 ⁹ 17 : 2 ¹³ 7 : 2 ² 11 : 2 ⁶ 15 : 2 ¹⁰ 19 : 2 ¹⁴ 8 : 2 ³ 12 : 2 ⁷ 16 : 11 ¹¹ 20 : 2 ¹⁵				
External Load (N):	A low level* latches the Internal Incrementing Register. Data must be quiescent during load interval. Minimum duration 200 nsec.			
External Read/Write (M):	Causes data to be read from the memory to the Internal Incrementing Register or written in memory from the Internal Incrementing Register. Low for read, high for write.*			
Incrementing Register (P):	Leading edge of positive-going TTL level causes the contents of the incrementing register to be incremented by 1.			

*TTL levels Low: -0.8 V; High - 2.0 V

SPECIFICATIONS SUBJECT TO CHANGE.

TECHNICAL DATA

LeCroy



NIM Model 3155

X-Y Plotter Interface for *qVt*® Multichannel Analyzer

The LeCroy Model 3155 is designed to mate with the Model 3001 *qVt* Multichannel Analyzer and serves as an interface between the 3001 and an x-y plotter.

The Model 3155 slows the 3001 display signals down to a rate which is appropriate to drive an x-y plotter, provides a switch to allow one to set up the plotter origin, and isolates the plotter from the 3001 outputs when it is not plotting and the display is in the fast sweep mode. The horizontal sweep plotting rate is adjustable from 2 to 6 points/sec via a 10-turn screwdriver potentiometer on the front panel. Parallel CRT signals are available on two front-panel connectors which allow a flickerless CRT display of acquired data when the 3155 is not in the plot mode. The unit is packaged as a #1 NIM module and may be operated in any standard NIM bin.

October 1982

SPECIFICATIONS

NIM Model 3155

X-Y PLOTTER INTERFACE FOR 3001 qVt MCA

Inputs:

Two front-panel connector cables from the CRT outputs of the Model 3001 qVt; plus one rear-panel 44-pin card-edge connector cable, pin-for-pin identical to the rear digital connector of the 3001 qVt. The rear-panel connector mates with AMP connector #582777-1 or equivalent.

Outputs:

Two front-panel BNC connectors to drive an x-y plotter; plus two front-panel BNC connectors to drive an external display scope. The x-y plotter and display scope output ranges are 0-5 volts for both the horizontal and vertical signals, with a minimum load impedance of 1 k Ω .

Controls:

Mode Select (three-position switch) selects operating mode to be either Display, Plot, or Zero.

Start Plot (pushbutton switch) initiates plotting sequence, beginning with the data of the first channel selected for CRT display from the 3001 qVt.

Rate Adjust (10-turn screwdriver potentiometer) varies the plotting rate from a minimum rate of 2 points/sec to a maximum rate of 6 points/sec.

Packaging:

In conformance with NIM standards. RF-shielded #1-width module.

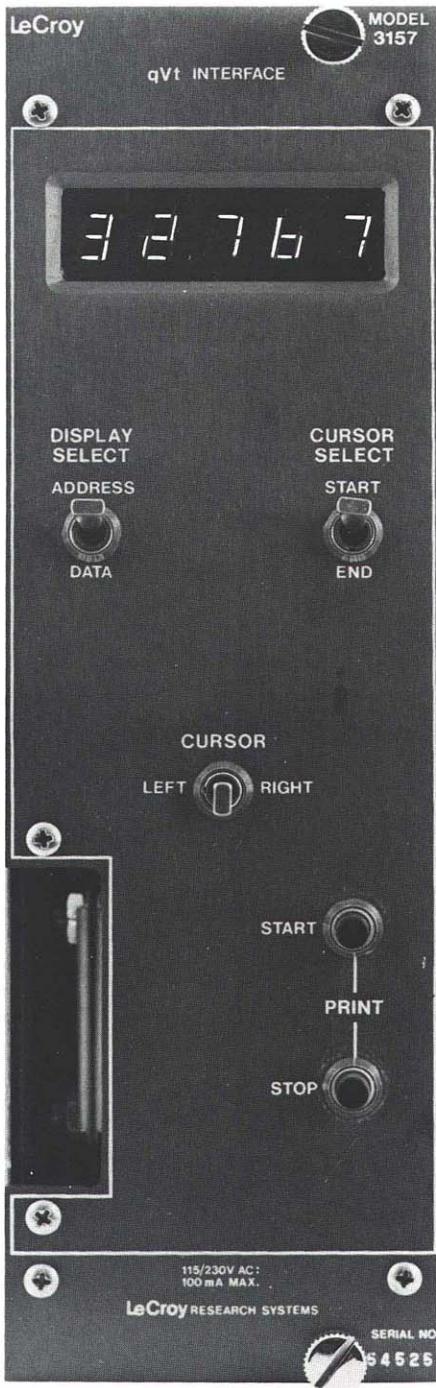
Power:

± 12 V at 100 mA.

SPECIFICATIONS SUBJECT TO CHANGE.

TECHNICAL DATA

LeCroy



NIM Model 3157

Printer and Display Interface for *qVt*[®] Multichannel Analyzer

The LeCroy Model 3157 is designed to mate with the Model 3001 *qVt* Multichannel Analyzer and is used to provide decimal *display* and *hard copy* readout of the 3001 memory data.

Two Cursors are generated by the Model 3157. These are used to set Start and End channel addresses for printing, and the address or the associated data of either Cursor can be read from a front-panel LED display. Choice of Start or End Cursor control and option of Address or Data display is provided with front-panel switches. Position control of the selected Cursor is done with a Left/Right Cursor control switch. If an oscilloscope display is being used with the 3001, the addresses set into the Start and End Limits are intensified on it. The rear of the 3157 has a 44-contact card-edge I/O connector for interfacing with the 3001 Analyzer.

The unit is compatible with a variety of ≥ 6 column line printers which accept parallel TTL inputs (e.g., Datel DPP-Q7 and Syracuse 14/12-TH). Printing is initiated by a front-panel button. An address is printed after each ten data lines. On those printers which suppress leading zeros, such as the Datel DPP-Q7, channel address is zero suppressed and data is not. On printers for which zero suppress is not an option, an asterisk in the leftmost column is used to indicate channel address. Only the data between the Start Limit and Stop Limit are printed. The unit is packaged in a #2 NIM module and may be operated in any standard NIM bin.

February 1981

SPECIFICATIONS

NIM Model 3157

PRINTER AND DISPLAY INTERFACE FOR 3001 qVt MCA

Inputs:	44-pin card-edge on rear panel, pin-for-pin identical to the Model 3001 qVt rear digital connector. Mates with 44-position connector with 0.156-inch centers or LeCroy Model DC44/2 Data Cable.
Outputs:	Two 34-pin headers on printed circuit board (with front panel access for cables) are directly compatible with Datel DPP-Q7 and Syracuse 14/12-TH printers. Mates with two 34-position flat cable headers or, for DPP-7 Printer use, with LeCroy Model DPP-DC34 Dual Data Cable.
LED Display:	Displays decimal value of Address or Data at the selected Cursor position.
Controls:	Display Select (two-position switch) selects option of Address or Data of selected Cursor. Cursor Select (two-position switch) selects Start or End Cursor to be controlled and displayed. Cursor Position (momentary, center-off lever switch) provides the ability to move the selected Cursor. Momentary contact will move the Cursor by one channel; continuous contact will begin automatic stepping.
	Start Print pushbutton initiates printout, starting at Start Address and stopping at End Address.
	Stop Print pushbutton provides means for manual termination of print operation.
Power Requirements:	Requires 115 VAC (50-400 Hz), or +6 volts, switch-selectable; via standard NIM bin power connector. Draws 1.35 A current. Caution: When powered by AC line voltage, the 3157 should be placed at least three NIM slots away from the 3001 to avoid noise transfer from the 3157 transformer to the sensitive 3001 analog circuitry.
Packaging:	In conformance with NIM standards. RF-shielded double-width module.

DATEL DPP-Q7 Printer*



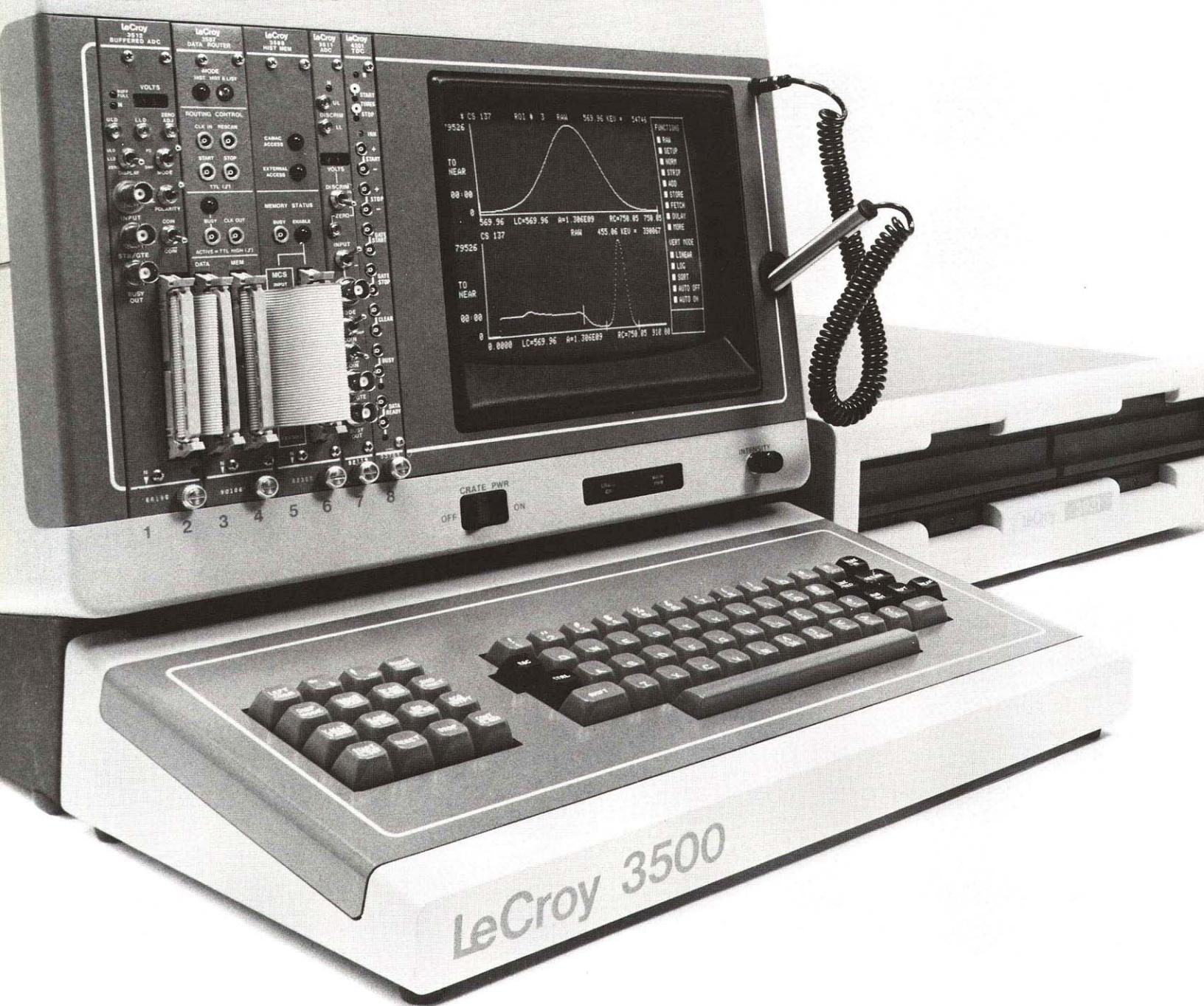
The Datel Model DPP-Q7 Printer operates with the LeCroy Model 3157 Printer and Display Interface to provide 7 column hard copy data on an inkless thermal paper. Maximum printing rate is 4 lines per second, with a capacity of approximately 9000 lines per roll. The self-contained printer mounts panel-meter style in a 4.50" x 2.72" cutout and is secured by four screws. Power is applied via standard A.C. line cord and plug, and BCD data from the 3157 is applied via the LeCroy Model DPP-DC34 Dual Data Cable to a printed circuit connector at the rear of the printer.

*Physically and electrically interchangeable with earlier DPP-7.

System 3500 Multichannel Analyzer

September, 1984

LeCroy 3500



LeCroy Research Systems Corporation

Introduction

The System 3500 is available in two powerful versions: the Model 3500MP, which includes the floppy disc accessory and extensive software to provide a fully programmable MCA; and the Model 3500M, a non-programmable firmware based system, requiring only acquisition modules for high performance MCA operation. Both configurations perform pulse height analysis, time analysis, and multichannel scaling with more input channels and at higher acquisition rates than any other commercially available instrument.

Expandable Inputs and Memory

Each input module can address up to 8k channels of histogramming memory for maximum energy and time resolution without digital offsetting techniques. For experiments requiring more than 8 inputs, an external CAMAC crate can be added for expansion to over 20 simultaneous ADC, TDC, or MCS inputs with a 1 MHz overall data transfer rate.

CAMAC Based

System 3500 employs two IEEE interface bus standards (CAMAC and Multibus).^{*} CAMAC is the widely used I/O standard for research grade measurement instruments. Only System 3500 has CAMAC built in, making it immediately compatible with over 600 modules. ADCs, TDCs, DACs, amplifiers, discriminators, transient recorders, SCR drivers, stepping motor controllers, computer interfaces, digital I/O modules, relay drivers and data loggers are but a few of the devices available. Through CAMAC the 3500 can monitor critical parameters and control experiments. The addition of a LeCroy transient recorder converts System 3500 into a fast signal digitizer or data logger. Only System 3500 affords this exceptional flexibility.

User Programmable

The Multibus crate houses a complete microcomputer that interfaces directly to an inexpensive floppy disc accessory which includes a disc operating system and full facility for programming in assembler, FORTRAN, or BASIC. Three microprocessors are included (main, arithmetic, and display); and 64k bytes of computer memory, a graphics display, and an ASCII keyboard are all standard.

Unlike other microprocessor-based MCAs, System 3500's microprocessors are accessible both by firmware and software programs creating an especially useful and unique facility called User Analysis. A user written FORTRAN program

can be embedded in the 3500 memory like resident firmware and executed as an MCA function. This feature enables a user to customize the system to perform display, analysis, and I/O operations unique to his experiment. Upgrading System 3500 to a software programmable MCA means only adding the inexpensive floppy disc accessory. Upgrading other MCAs to software capability usually means adding a computer, interface, and peripherals frequently costing more than the MCA.

Adapts to a Variety of Applications

System 3500 is equally suitable for single input high rate pulse height analysis experiments or multiple input PHA, time of flight, or single photon/ion counting experiments. In its standard configuration the 3500 is a complete system yet it offers exceptional expansion capability through module or peripheral building blocks to accommodate complex multiple input acquisition, analysis, and control experiments or even multiple concurrent experiments. An added benefit is 3500's computer terminal facility which enables communication with a host computer in either full or half duplex modes. Alternatively, the main computer or separate terminal can remotely operate and control all functions of System 3500.

Extensive Data Manipulation Capability

Consistent with its high performance and multiple input advantages, System 3500 provides powerful MCA firmware programs to support system and module setup, and collection, display, manipulation, analysis and output data. Dedicated programs guide setup of the system and provide real time display of multiple inputs. Add, strip, overlay, normalize, smooth, calibrate, peak search, and key stroke programming functions are representative of the facilities available for analyzing and comparing energy or time distributions. Linear, log, and square root display modes, each with autoscaling, combined with multiple regions of interest and spectra expansion facilitate data interpretation. Hard copy outputs of tabular listings as well as graphic display representations are both supported. With the floppy disc accessory, storing and recalling complete data and experiment files is an especially convenient process using simple light pen instructions. In addition, powerful software for data analysis, such as an Isotope Library and Identification Package are available on floppy disc.

Description

System 3500 is a microprocessor-based, firmware-controlled multichannel analyzer containing complete facilities for data acquisition, display, storage, analysis, control, programming and input/output in a single compact unit. The functional components of System 3500 include:

- 1 One to eight user-selected CAMAC acquisition modules.
- 2 8-slot CAMAC minicrate and dataway.
- 3 Nine inch, raster-type CRT display.
- 4 ASCII keyboard.
- 5 16 button, 23 function control pad.
- 6 Interactive light pen.
- 7 Multibus computer crate which houses all system component boards.
- 8 System power supply providing ± 12 , ± 24 , ± 6 , and ± 5 volts dc.

The Multibus computer crate, and system boards, comprising the heart of System 3500, provide CAMAC interfacing and control, central processing, display processing and control, DMA data storage and histogramming, and serial and parallel input/output to peripherals and other computers.

The Multibus crate consists of an enclosure and a backplane and connector assembly that houses and interfaces to the system boards. Seven system boards constitute the standard System 3500. Eleven more positions are provided on the bus for system expansion to peripherals, external CAMAC crates and added histogram memory. With most system components contained on just seven boards, all readily accessible through a large rear door, system trouble-shooting and repair by the user is efficiently provided through a responsive factory board exchange program. Standard System 3500 boards include:

Central Processor

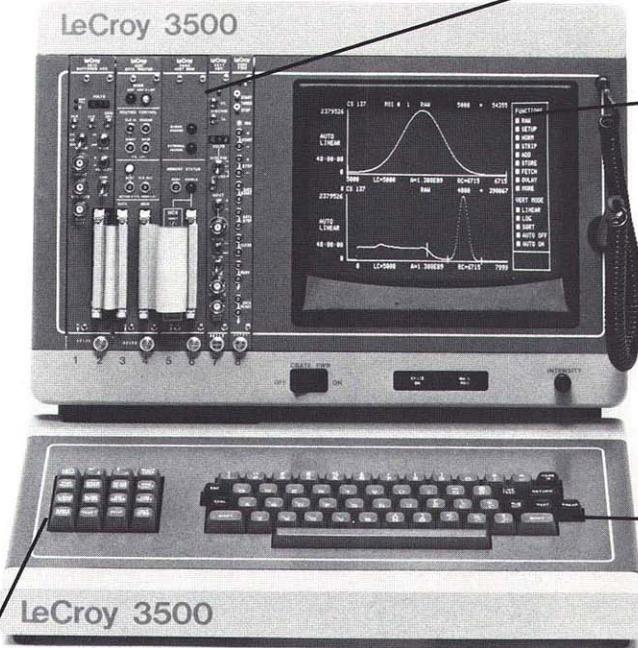
The CPU board contains an 8085A microprocessor, 30k bytes of ROM containing standard MCA firmware programs, and 1k byte of CMOS static non-volatile random access memory for retention of system and module setup parameters. The CPU also includes a built-in EIA RS-232-C serial port with baud jumper selections ranging from 75 to 19,200. The port is cabled to a standard D connector on the rear panel.

CAMAC Controller

The controller board interfaces the CAMAC dataway and CAMAC acquisition modules to the Multibus and to data memory for writing control words to the module and reading data from the module.

*Conforms to IEEE CAMAC Standards 583, 595, 596 and IEEE Multibus Standard 796.

Description



Control Pad

Simple and convenient setup and operation is provided by this 16-key, 23 function control pad. Control functions for acquisition, I/O, region of interest selections, vertical mode and range selections, data clearing, and scrolling through memory groups, regions of interest, and setup status pages are contained in this one control cluster.

DMA Interface

The DMA board interfaces the CAMAC Controller directly to the histogramming data memory board by an external bus to enable data transfers at the maximum CAMAC bandwidth of 1 MHz. This board also contains the dwell time clock for the multichannel scaling module. DMA acquisition can be enabled or disabled through the CAMAC dataway without CPU intervention to free the CPU for other tasks and provide more responsive acquisition control.

Histogramming Data Memory

The standard data memory board includes 8192 channels of 24-bit (16,777,215) count capacity per channel. Up to 7 additional data memories can be added, for a total of 64k x 24 bits. The high count memory accommodates System 3500's high resolution and high rate acquisition modules offering im-

proved counting statistics without memory overflow concerns. The memory is dual port to permit data acquisition and histogramming through the DMA port with concurrent non-destructive readout through the computer port for display updating, data analysis and interpretation, and data output to a printer, data storage device, or external computer.

Display Memory and Timing

The display memory and timing board provides 128k by 1-bit words of memory for display which corresponds to the 256 by 512 picture elements on the raster-type CRT. Fixed display programs such as MCA graphics are stored in 8k bytes of ROM and 8k bytes of RAM. In addition to driving the built in display, this board provides a composite video output to drive an external video monitor or video printer.

Display Processor and APU

The display processor and APU board includes an 8085A microprocessor ded-

CAMAC Minicrate

Built-in 8-module minicrate is compatible with any CAMAC module. Up to 8 ADC, MCS or TDC inputs can be accepted with DMA data transfer to memory at 1 μ sec/input. With a Model 4501 CAMAC-to-NIM adapter, the minicrate can also power NIM front-end modules.

CRT Display

The 9-inch CRT provides an interactive display of input data, setup parameters, and program listings. A live graphics display of ADC, MCS or TDC input data from one or two inputs is provided, or display from a single input memory group and an expanded region of interest in the memory group can be displayed simultaneously. During setup, a separate status page is displayed for system, module, and auto analysis programming. In software programmable systems, program listings are displayed.

Light Pen

The light pen permits interactive operations with the display for setup programming, data display manipulations, and data analysis functions.

ASCII Keyboard

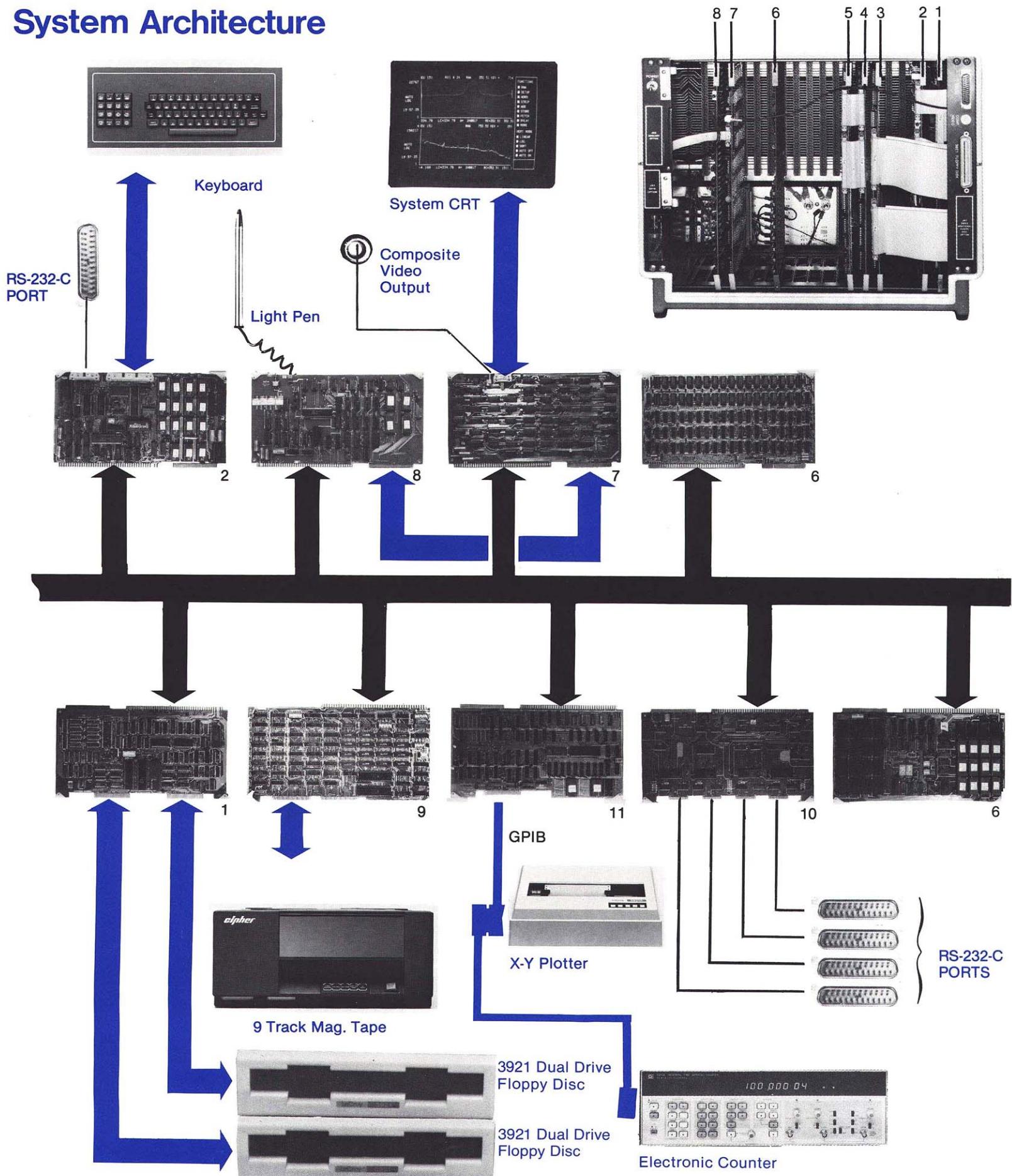
The keyboard used for defining setup parameters, cursor and marker locations, vertical and horizontal graph ranges, and for FORTRAN, BASIC, or Assembler programming.

icated to display operations. The separate processor makes possible faster display updates and manages cursor, marker, and light pen operations. An Arithmetic Processor Unit (AM 9511) is provided for hardware-executed multiply, divide, and transcendental operations required in vertical auto-scaling of data and log and square root display scaling to further speed display updating and scaling operations. In software programmable systems, an APU software library is supplied for linking to FORTRAN or BASIC programs to substantially reduce the execution time of programs containing extensive arithmetic operations.

Computer Memory

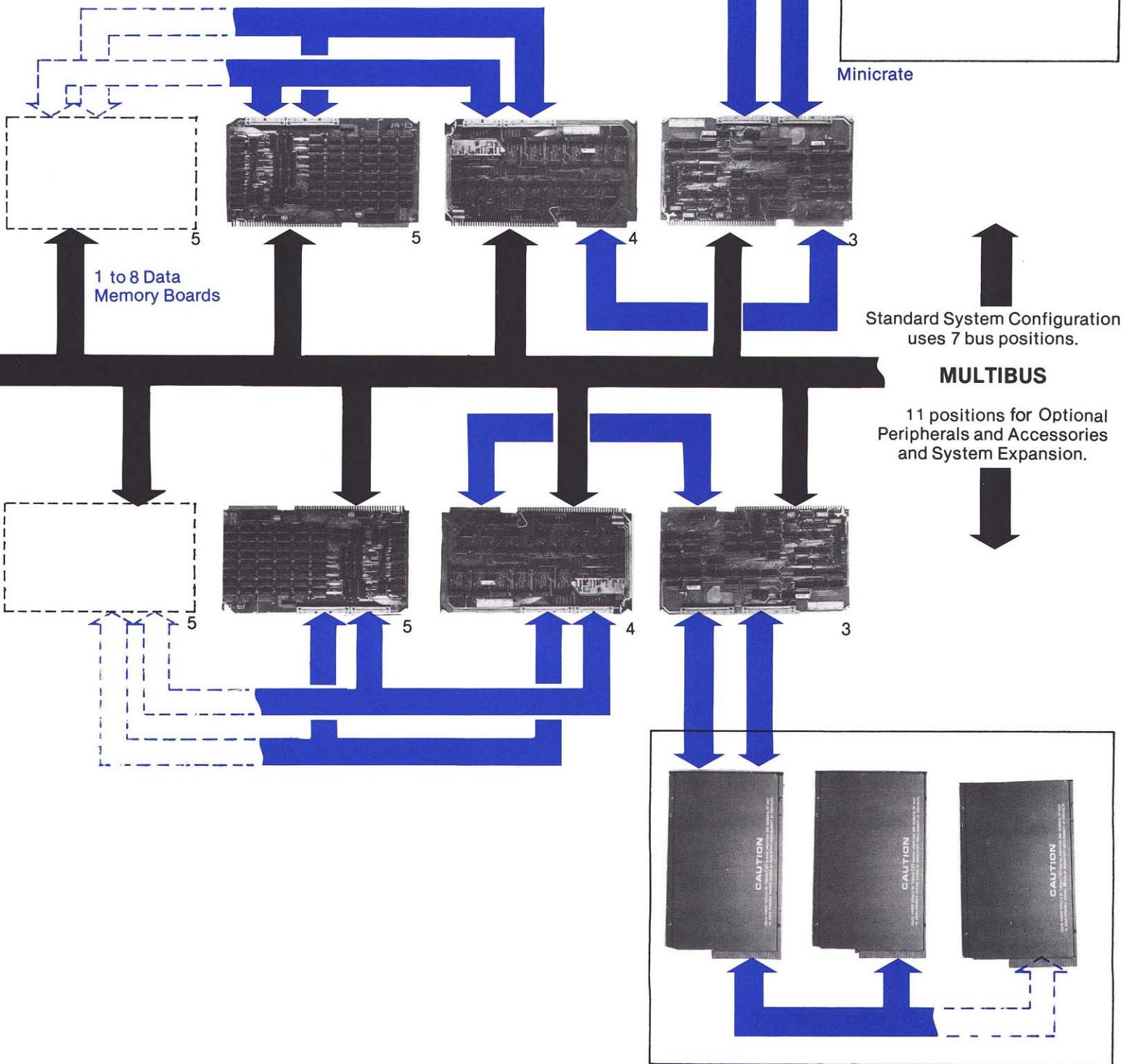
The computer memory board contains 64k bytes of static random access memory for executing data display, analysis and output functions. In software programmable systems, the disc operating system resides in 8k of memory, with up to 24k available for high level user-defined programs.

System Architecture



Standard and Accessory System Boards

1. Model 3500-8 Disc Controller (optional accessory)
2. Model 3500-1 Central Processing Unit
3. Model 3500-5 CAMAC Controller
4. Model 3500-6 DMA Interface
5. Model 3500-2 Histogramming Data Memory
6. Model 3500-7 PROM Extender
7. Model 3500-3 Display Memory and Timing
8. Model 3500-4 Display and Arithmetic Processor
9. Track Tape Controller (optional accessory)
10. Model 3500-35 Quad RS232 Port (optional accessory)
11. Model 3500-38 GPIB Controller (optional accessory)



Data Acquisition

System 3500 offers unprecedented data acquisition flexibility and capacity in both MCA and general acquisition experiments. MCA acquisition front ends include pulse height analyzers, time analyzers, and multichannel scalers.

With these inputs, the data-to-memory transfer rate is 1 MHz in a hardwired direct memory access (DMA) mode from dedicated acquisition modules. In the software programmable system, any CAMAC module is directly software and hardware compatible affording exceptional flexibility in selecting acquisition and control electronics for specific experimental requirements.

With DMA acquisition, many other MCA operations such as display updating, data analysis, hard copy output or even communication with other computers can be performed simultaneously without interrupting acquisition. Start/stop control of acquisition can be manual through the control pad, remote through the serial communication port, or under the 3500's Auto-Analysis control. Automatic preset stop time selections for each input range from 1 second to 100 hours, controlled by a built-in timer.

20 DMA Inputs

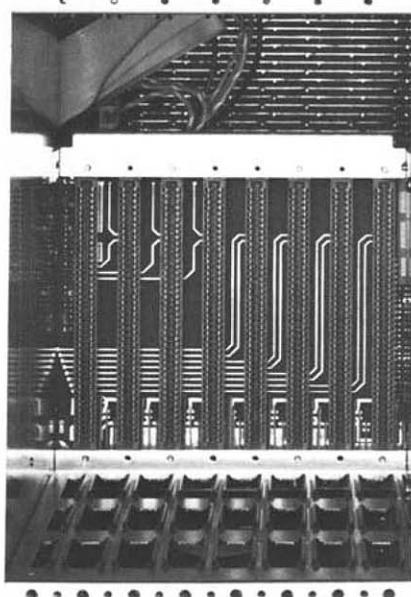
System 3500 accommodates several times the number of input channels of conventional MCAs without deadtime-producing routers. Up to 8 independent ADC, TDC, and MCS acquisition modules can be supported in the standard system with simultaneous acquisition and multiplexed data transfer to memory at a 1 μ sec/word rate. With the addition of an external CAMAC crate, over 20 DMA input modules can be supported simultaneously. Special interface cabling and memory addressing is not required. The CAMAC dataway provides a reliable, standardized hardware connection while 3500 firmware interacts with the operator to direct light-pen configuration of the system.

Memory Expandable to 64k Channels

Up to 64k channels of dedicated 24-bit histogramming memory are available for storage of all data from each of 8 inputs. Other MCAs with limited memory require digital offsetting which stores only a segment of a spectrum at the full resolution of the input module. System 3500 stores all data from an experiment, allowing the user to first analyze, then later discard unnecessary data.

The standard 3500 includes a single histogramming data memory module, implemented in a Multibus compatible board of 8192 channels by 16,277,215 count capacity/channel. Adding memory simply involves plugging in up to 7 additional boards. Firmware is built into the standard system to support the full complement of memory, and DMA-to-memory bus cabling is supplied with additional memory boards to match the configuration specified by the user.

Each 8k memory board is segmentable under 3500 firmware control in binary step of 8192, 4096, 2048, 1024, 512 and 256-channel memory groups. The memory size is determined by the time or energy resolution required of each DMA module in the experiment. Any combination of memory group sizes can be selected for each memory board up to 8K channels.



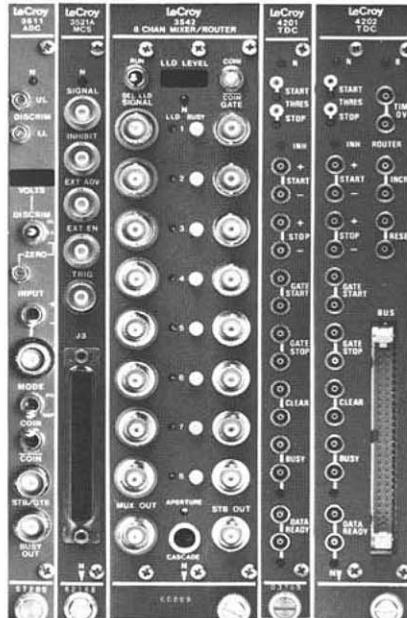
CAMAC Minicrate Houses up to 8 PHA, MCS, or TDC Acquisition Modules.

Spectroscopy Analog-to-Digital Converters

The 3500 is compatible with two high performance ADC's: the Model 3511 offers 13-bit resolution and 5 μ sec conversion time, and the Model 3514 which converts 12 bits in one μ sec.

Both ADC's operate in either peak detect mode, with coincidence or anticoincidence gating, or strobed sample mode for sampling d-c or slowly varying a-c signals. A unique self-strobing feature precludes external electronics and permits sampling the input signal from 100 nsec to 35 μ sec after triggering the lower level discriminator. Both bipolar and monopolar, positive or negative, d-c coupled inputs in the range of 50 millivolts to 8 volts can be accepted with risetimes of 300 nsec to 20 μ sec.

Upper and lower discriminators and zero adjust are precisely set by 22-turn potentiometers with settings read on an LED display. An ADC prompt or delayed busy output can be provided to a dead-timer module (Model 3541) for conversion deadtime measurements, to enable successive 3511 ADCs, or for external timing or control.



Some of the many CAMAC modules that can be used in the System 3500's minicrate.

Data Acquisition

Model 3521A Multi-channel Scaling Module

The Model 3521A employs a double buffered scaling input to provide 100 MHz input rate capability with 1 μ sec minimum dwell time per channel and negligible (< 5 nsec) interchannel deadtime. Count capacity is up to 24 bits-1 (16,777,215) counts per dwell period into the 3500's data memory. It is the ideal instrument for applications having high input rate and fast rate change conditions. Examples include ion counting measurements from mass spectrometers and laser scattering and luminescence decay time measurements having fast, single event counting requirements.

Both single and continuous sweep modes are provided with ramp-up/ramp-down sweep capability or ramp-up and return to zero. Model 3521A counts input logic pulses (either NIM or TTL levels) from a single-channel analyzer, discriminator, or other logic pulse generator.

Synchronization between the Model 3521A and external equipment is bi-directional i.e., the 3521A can generate synchronization signals or be synchronized by an externally-generated signal. In single sweep mode an external trigger initiates each sweep for synchronization. Channel advance can be controlled by System 3500 with dwell time from 1 μ sec to 4296 seconds or externally controlled at any time increment down to 1 μ sec. The channel address can be input or output through a front-panel connector to synchronize the sweep with the experiment or to initiate sweeps at any channel location for multiplexing many detector inputs.

Internal counters and registers allow programming the number of channels per scan, the number of scans per run, address offset for direct memory access (DMA) storage in 256 to 8192 channels of data memory, and a choice of ramp-up and return to start or ramp-up-down address scanning.

Model 3541 Deadtimer

The 3541 is a 1-wide CAMAC module containing two independent channels of live/real time preset control and percent deadtime measurement for operation with two 3511s. Alternatively, each channel can provide time control and overall deadtime measurement for multiple ADCs. Preset live or real time for each channel are program selected for operating convenience. Preset time selections of 1 millisecond to 900,000 seconds are provided in two hardware selected ranges.

Separate 2-digit LED displays read out percent deadtime for each channel. Percent deadtime is derived by calculating the duty cycle of the ADC's busy signal with the 10 MHz clock. Deadtime percent can be read from both channels to become part of the data file of an experiment.

Model 3542 8-input ADC Multiplexer/Router

The substantial PHA input capacity of System 3500 can be significantly increased with the Model 3542 accessory. The 3542 is a 3-wide CAMAC module which accepts 1 to 8 asynchronous 0- to 8-volt analog inputs for multiplexing and routing to a single ADC and provides 8- to 12-bit resolution for each. The overall data throughput rate is 350 kHz, and better than 40 kHz average for each of 8 inputs. A 3542 effectively doubles the input capacity within the built-in 3500 minicrate and reduces the cost per channel by over 70% versus use of eight individual ADCs. For low to high resolution, medium rate, multiple input experiments, a 3542 offers an efficient, economical solution.

Each channel includes an independent gate and an independent lower level discriminator adjustable from 0 to 8 volts and selectively monitored on a single 3-digit LED readout. After each conversion, System 3500 automatically routes data to that input's pre-assigned 250- to 8,000-channel data memory location. Each input can be labelled on the graphic display for convenient input identification.

Model 4201 Time-to-Digital Converter

The 4201 is a fast encoding TDC offering unprecedented time resolution, precision, data rate, and dynamic range. Upon receiving a start/stop pulse pair, 4201 converts the time difference to 24-bit (± 1 LSB) precision with a time resolution as low as 156 picoseconds, programmable to 3276 nsec in 16 steps. The maximum full scale time range is 1667 μ sec encoded in 24 bits, with shorter times programmable through System 3500. The conversion time ranges from 0.6 to 1 μ sec, depending on the time resolution selected, permitting a start/stop data rate at the 1 MHz data transfer rate of System 3500.

Input pulses can be differential or single sided in the range of -1.5 volts to +1.5 volts. Individual thresholds adjustable by front panel potentiometers to ± 20 mV precision are provided for both start and stop inputs. Individual start and stop gate inputs are also provided with minimum time windows down to 10 nsec.

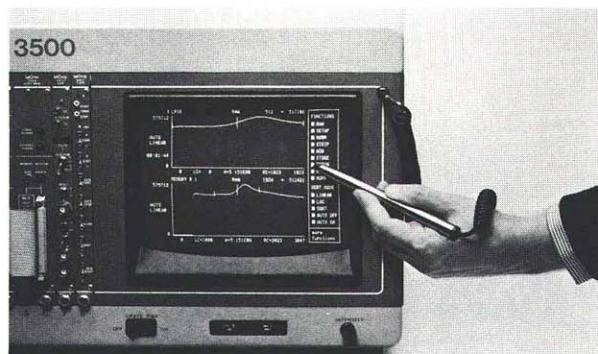
Time analysis experiments requiring short time resolution, high throughput rate, and high precision are ideal applications of the 4201. Examples include X-ray crystallography or mass spectrometry experiments using sensitive delay-line detectors, and time of flight and fast decay measurement experiments.

Model 4204 Extended Fast Encoding TDC

Model 4204 has the same basic features as the Model 4201, with the addition of an extended 32-bit time range, 24 bits of which are readable. An externally controllable routing system has been included to permit shifting of the acquired data over the 24 readout bits by an amount fixed in a 16-bit register. Finally, the data are presented on a front panel auxiliary bus for interconnection to an external histogramming memory, such as the LeCroy Model 3588.

Setup/Display/Analysis/Output Capabilities

All system 3500 multichannel analyzer setup, display, analysis, and output functions are firmware supported. The user interacts with system firmware to control setup and operation through a 23-function control pad, an ASCII keyboard, and an exclusive display interactive light pen. Operation of System 3500 is straightforward and understandable through use of the functionally-labelled pushbuttons, interactive display menus, and display prompting.



Light pen offers a convenient and interactive method of performing display and analysis operations.



Setup

Setup consists of installing and cabling front-end acquisition modules, turning on power, and programming the system's hardware configuration and acquisition module parameters. When line power is on, a Main Menu with up to seven selections is displayed requesting a light pen or keystroke selection of the display page desired. For standard MCA operations, System Architecture is the initial selection.

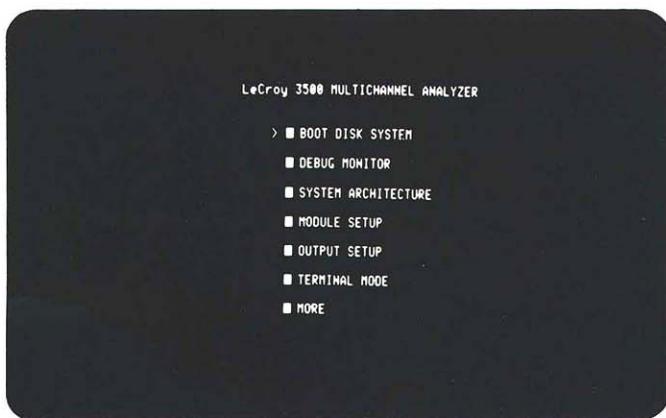
Acquisition, Output and Display Status Operations are provided by the 23 function Control Pad, while the ASCII keyboard permits numerical entries and edits and executes programs.

System Architecture

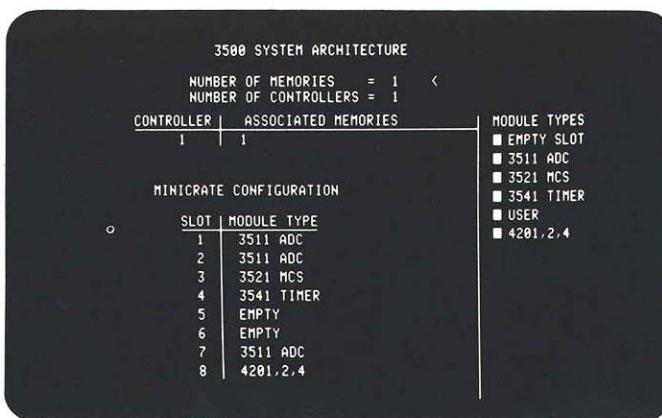
The System Architecture page enables the user to define directly and conveniently the hardware configuration of the 3500. The number of histogram memory and CAMAC controller boards is entered via keystrokes and the input modules are assigned by the light pen to the slot corresponding to their physical location in the CAMAC minicrate.

Module Setup

A setup page is displayed for each module assigned to a CAMAC slot. Up to eight pages are provided in the standard system while over 20 pages can be sequentially displayed if the system includes an external CAMAC crate option. To identify the



Main Menu.



System
Architecture.

Setup

acquired and stored data associated with any of the input modules, space is provided for entitling the experiment. The title is displayed with the data and becomes part of the experiment's file when hard copy, disc, or magnetic tape files are output. In addition to the ADC live/real preset time control provided by the deadtimer all input modules

have access to individual preset real time control with time selections of 1 second to 100 hours. Alternatively, the timer can be set to infinity to monitor elapsed time of the experiment under manual or external stop control.

Analog-to-Digital Converters

All analog input gating selections are provided on the front panel of the ADC, while conversion gain, memory location, and acquisition timing and mode selections are under program control. A memory map greatly simplifies assignment of memory to a module by displaying all unassigned

memory in blocks corresponding to the selected conversion gain. In the illustration, 2k conversion gain is selected which divides memory into four 2k blocks. The 3511 has been assigned to memory channels 0 to 2047, and the remaining 6k of memory is available for other modules.

Model 3541 Deadtimer

Keyboard entries define the slot numbers of all ADCs to be timed by each channel of the 3541 and select the preset live or real acquisition time for those inputs. Time selections are 1×10^0 to 9×10^5 milliseconds or seconds and are directly entered as powers of 10.

Model 3521A Multi-channel Scaler

Programming of numerical parameters for the 3521 such as dwell time and number of scans is by convenient keyboard entries. Dwell time selections range from 1 μ sec to 4296

seconds and the number of scans or sweeps can be 1 to 65,535 or infinity. Triggered or continuous scanning modes are also a programmable selection.

Models 4201/4204 Time-to-Digital Converters

Keyboard entries of time resolution, number of channels, memory location, and whether negative time is permitted are made using the simple setup page illustrated. Again, a memory map indicates these portions of memory which are available for module assignment.

All system and module setup parameters are stored in non-volatile memory to prevent erasure during a power interruption and module setup parameters are also output with data files to a disc or hard copy device.

LeCroy 3511 ADC PARAMETERS (MINICRATE SLOT 3)

TITLE ADC 3511
ACQUISITION DURATION = 01 30 00
(HH MM SS OR "INFINITE")
CONVERSION GAIN = 2
DWTM MODE (0=ADD,1=SUB) = 0

MEMORY MAP

LeCroy 3541 DUAL DEAD TIMER PARAMETERS (MINICRATE SLOT 4)

#1 ADCS: 1 2 3 = 2E5
TIME = 2E5
LIVE/REAL TIME SELECTION = 0
(0=LIVE,1=REAL)
ACTIVE/INACTIVE SELECTION = 0
(0=ACTIVE,1=INACTIVE)

#2 ADCS:
TIME = 1E4
LIVE/REAL TIME SELECTION = 1
(0=LIVE,1=REAL)
ACTIVE/INACTIVE SELECTION = 1
(0=ACTIVE,1=INACTIVE)

Setup Page for Model 3511/3514 Analog-to-Digital Converter.

LeCroy 3521 MCS PARAMETERS (MINICRATE SLOT 4)

TITLE MCS 3521
ACQUISITION DURATION = 12 34 56
(HH MM SS OR "INFINITE")
DWELL TIME IN SECONDS = 1.000E-6
NUMBER OF SCANS = 2000
(0=INFINITY)
NUMBER OF CHANNELS (1-4) = 4
RAMP (0=UP DOWN 1=SAWTOOTH) = 1
MODE (0=TRIGGERED 1=CONTINUOUS) = 1

MEMORY MAP

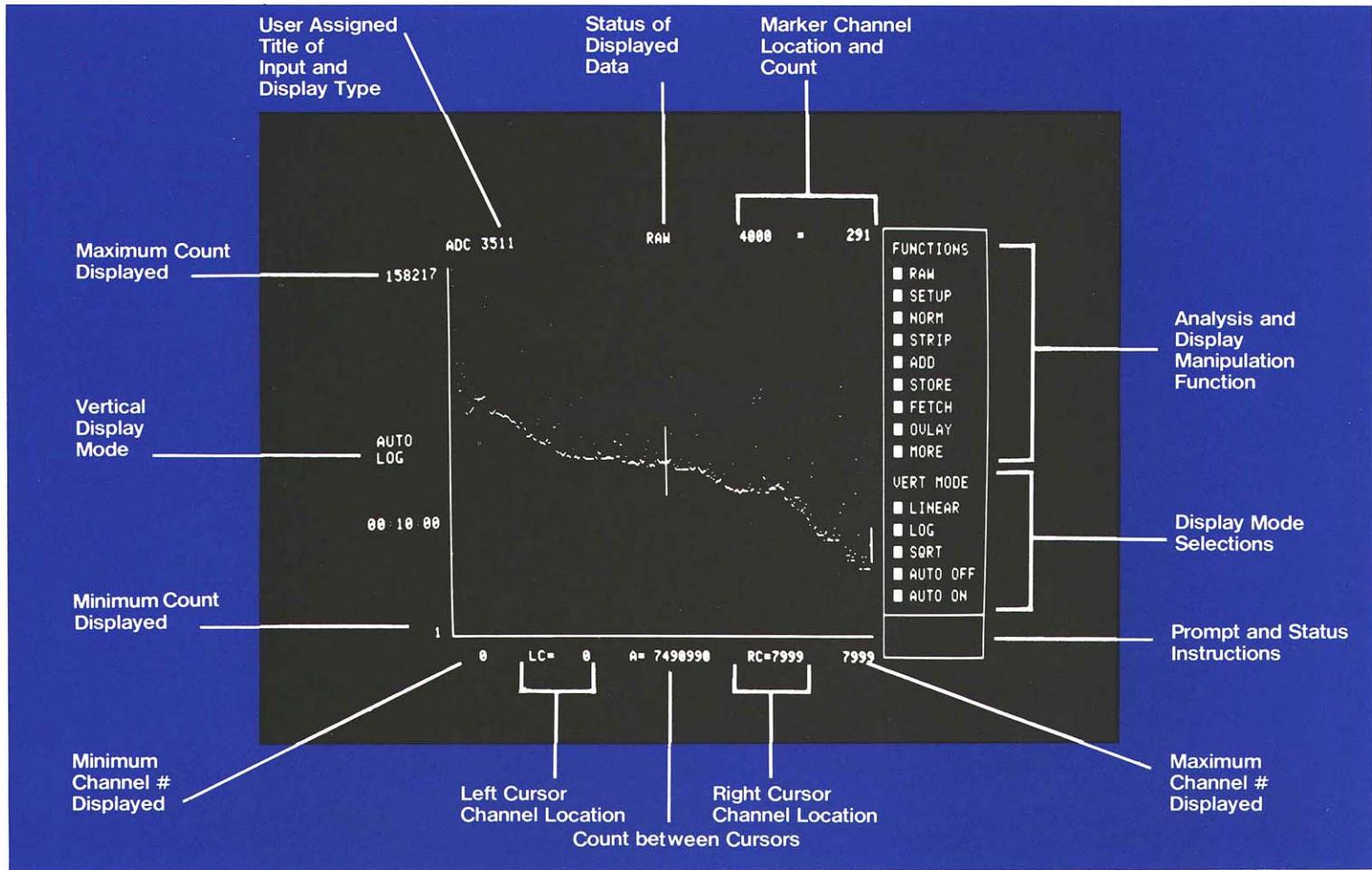
LeCroy 4284 TDC PARAMETERS (MINICRATE SLOT 8)

TITLE LRS8
ACQUISITION DURATION = INFINITY
(HH MM SS OR "INFINITE")
RESOLUTION = 1
1 156 ps 5 2500 ps 9 48 ns 13 648 ns
2 312 ps 6 5 ns 10 88 ns 14 1288 ns
3 625 ps 7 10 ns 11 160 ns 15 2560 ns
4 1250ps 8 20 ns 12 320 ns
NUMBER OF CHANNELS = 1K
ROUTING (1=YES,0=NO) = 0

Setup Page for
Model 3521A Multichannel
Scaler.

Setup Page for
Model 4201/4204
Time-to-Digital Converter.

Display



Single Graph Data and Alphanumeric Display

System 3500 provides exceptional flexibility with and accessibility to data for display and manipulation. The 9-inch CRT has a 256 vertical by 512 horizontal picture element display which is continually updated during acquisition by a dedicated 128k by 1 bit display memory and processor. The graphics display consists of single or dual x-y plots of counts versus channel number and annotating alphanumerics defining display scales, cursor and marker location, and display status. The right hand column lists a menu of display manipulations and analysis functions all of which are conveniently selected by the light pen. In addition to data updating, the marker, area, and maximum count values are also updated continually during acquisition to visually monitor an experiment. Over 20 inputs can be displayed simultaneously on one or two x-y graphs or one or two separate inputs of up to 8k channels each can be displayed.

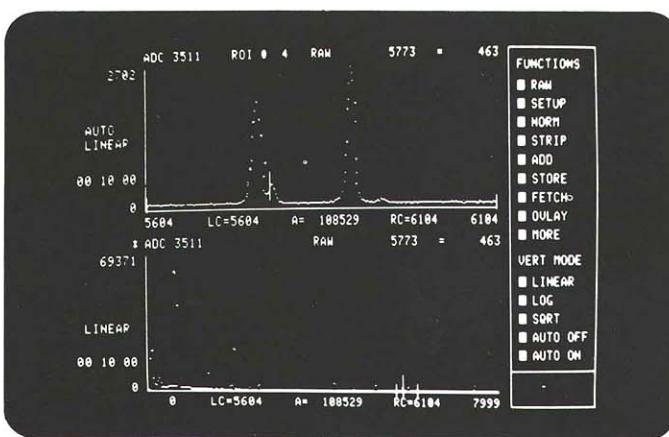
Dual graph display of memory group and expanded region of interest.

Memory and Regions of Interest

The memory assigned to each input module is a memory group. A user-assigned title for the module is displayed with the associated memory group for easy identification of that input's data. A memory group can be from 256 to 8192 channels, depending on the memory assigned to that module. When multiple inputs and associated memory groups are defined, the arrow keys on the

control pad sequentially scroll through all memory groups for convenient display selection of any input's data.

Multiple regions of interest can be defined within each memory group up to a total of 255. Regions of interest can be any number of channels, to the maximum of the memory group, and can overlap or lie within one another. Regions of interest are defined by positioning the left and right cursors to channel locations encompassing the spectral region of interest. Then, a single pushbutton selection on the control pad defines and sequentially numbers each region. The bidirectional arrow keys position the cursors and accelerate positioning when held down. Alternatively, a channel number can be entered on the keyboard to position cursors rapidly.



Display

Regions of interest are expanded on the upper graph of a dual graph display while the lower graph displays the complete memory group in which they were defined. The channel numbers of the left and right cursors defining the regions of interest become the horizontal scale minimum and maximum values on the upper graph. With multiple regions

of interest defined, the arrow keys on the control pad permit rapid scrolling through each region of interest. The location of each region of interest within a memory group is defined by left and right cursors on the lower graph for convenience in locating region-of-interest-defined energy peaks within the total spectrum.

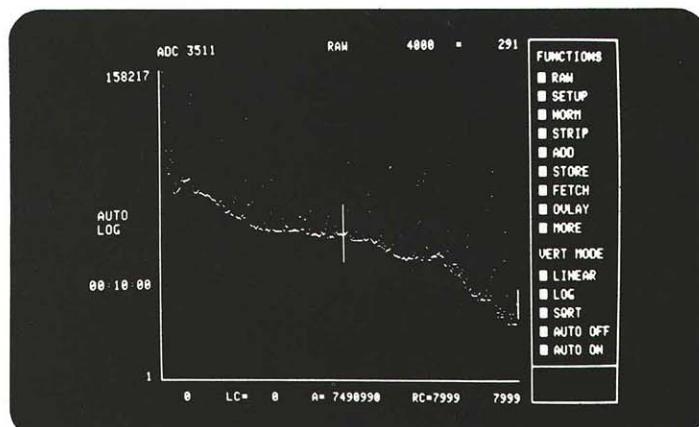
Linear, Log, and Square Root Display

To increase vertical display resolution as an aid in examining multiple spectral peaks with a wide range of count values, System 3500 provides both log and square root vertical display scaling modes in addition to linear scaling. In all modes, the maximum and minimum values can be set to any desired count value, or autoscaling can be selected to automatically set vertical maximum to the highest channel count value in the display. Autoscaling is especially useful during acquisition as it always uses the full vertical display resolution for the range of count values in memory.

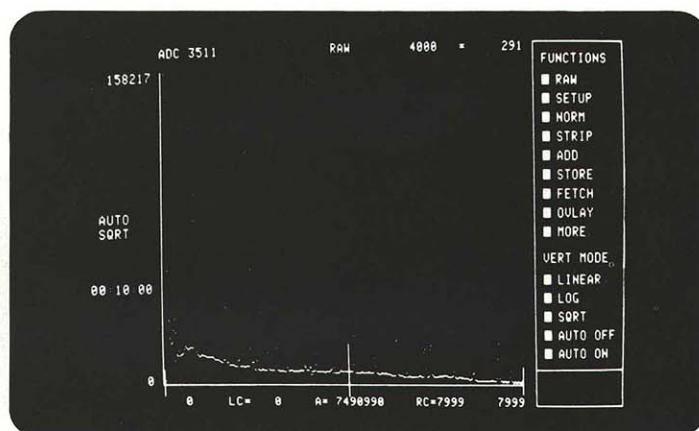
Spectra Scan™

In examining data displays of high resolution energy spectra, it is often useful to expand the display for examination of narrow energy ranges of the spectrum. Expansion of the spectrum helps resolve multiple peaks to permit precise setting of regions of interest for peak area calculation and readout. The 3500 provides a unique Spectra Scan feature which permits detailed examination of the spectrum by allowing the user to move a window of selectable size along the lower graph, representing a memory group, and scan the contents of the window in the upper graph. The window is moved by use of the bi-directional arrow keys, and as a peak of interest enters the window, it can be defined as a region of interest. Spectra Scan is an exceptionally convenient means of rapidly defining multiple regions of interest in a complex high resolution spectrum.

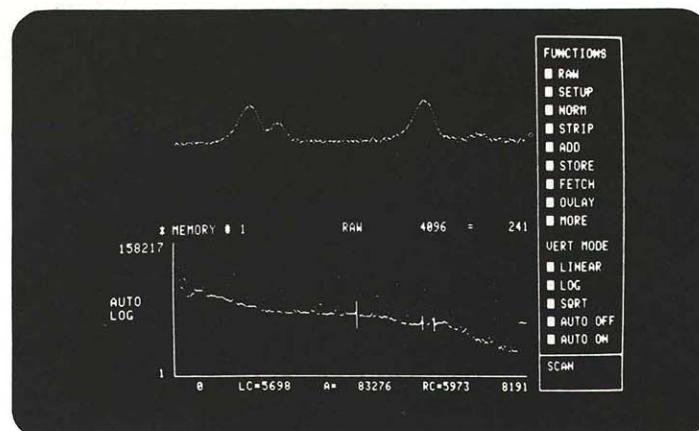
Spectra Scan is a trademark of LeCroy Research Systems Corporation.



Log display mode with vertical autoscaling.



Square root display mode with vertical autoscaling.



Spectra Scan aids examination of high resolution, multiple peak spectra.

Data Analysis

A set of firmware is included in the standard 3500 for processing and manipulating data both during acquisition and prior to data readout. Functions are included for adding or subtracting two graphs, normalization including base line subtraction of a graph, overlaying two graphs, and storing a spectrum in a section of memory for later recall. Choosing and executing any of these functions is a simple light pen selection

from the menu of functions displayed on the right hand side of the graphics display.

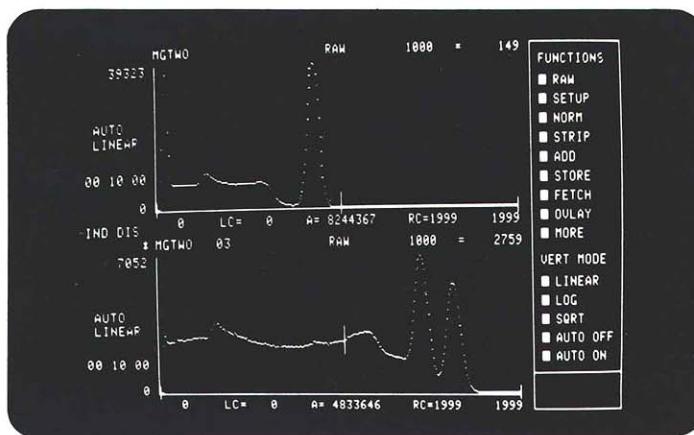
When a function is executed, the raw function legend at the top of each graph will change to the name of the function selected so that the state of all displayed data is always known. Some operations such as add and subtract require two graphs for implementation. Typically, the two graphs selected

for analysis or manipulation will be two memory groups or two regions of interest within either the same or different memory groups. Display manipulations do not alter the raw data stored in histogramming memory. Each time a function is selected it is executed rather than replacing the raw data with the processed data. This permits multiple analyses to be performed on the same raw data for convenient and exacting data processing.

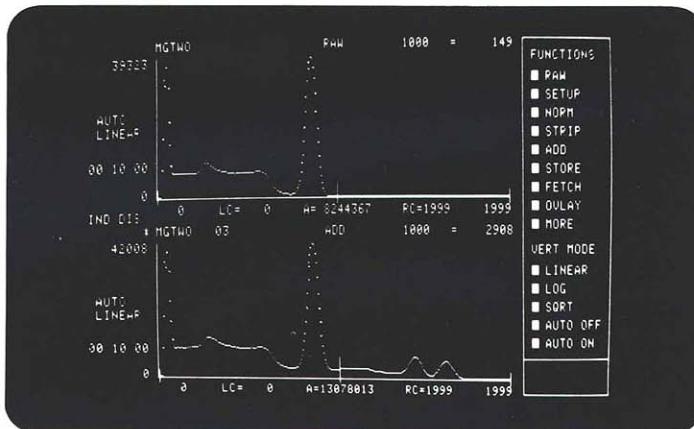
Add Strip Normalize and Overlay Functions

Data can be selectively acquired in separate memory groups to permit a variety of arithmetic and comparative operations without interrupting acquisition and data storage. The add function permits addition of spectra to integrate all common energy peaks for total net count information. With the strip function, any spectrum can be multiplied by a constant and added to, or subtracted from, any other spectrum. This, combined with the overlay function, allows very convenient direct comparison of two similar spectra. The normalize function permits adding or subtracting a fixed offset from a spectrum and multiplying it by a constant to normalize any selected spectrum by any incremental count value or factor.

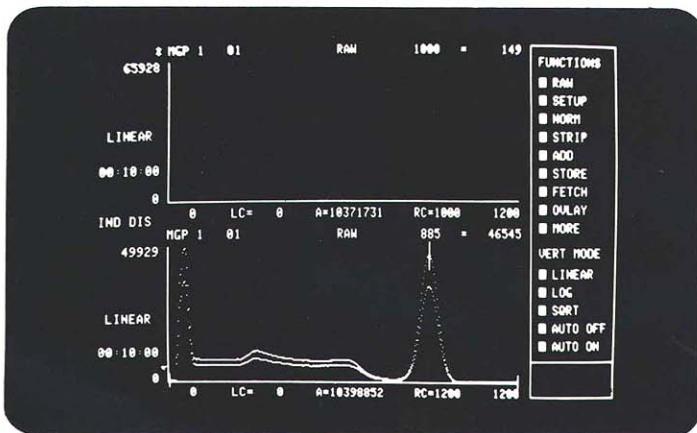
In strip operations, the normalization factor can be automatically computed as the ratio of the areas of two selected spectra, or the ratio of the marker values of two selected spectra. Similarly, the offset value for normalizing a spectrum can be automatically derived from the average value between the cursors or from the marker value of the spectra. A setup/normalize menu is provided to select strip and normalize factors and offsets.



Raw Data Prior to Addition.



Upper Graph
Added to Lower Graph.

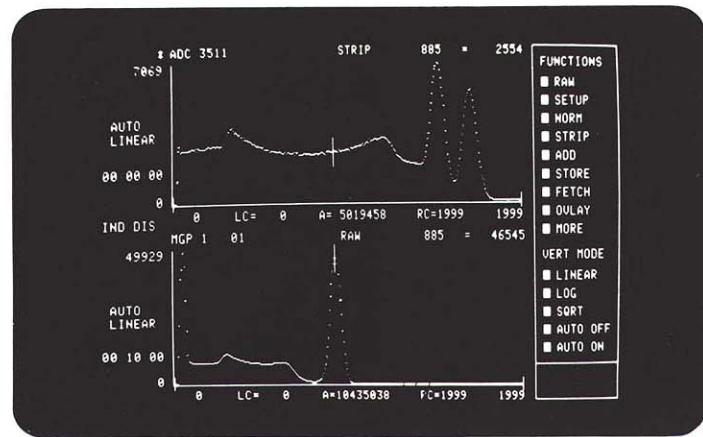


Spectra Overlaid
for Direct Comparison.

Data Analysis

```
STRIP/NORMALIZE SETUP  
  
MULTIPLIER  
□ CONSTANT 1 000E0  
■ RATIO OF AREAS  
■ RATIO OF MARKER VALUES  
  
BASE (NORMALIZE ONLY)  
□ CONSTANT 1150 <  
■ AVERAGE VALUE BETWEEN CURSORS  
■ MARKER VALUE  
  
■ EXIT
```

Strip/Normalize Setup Menu.



Result of Strip Operation.

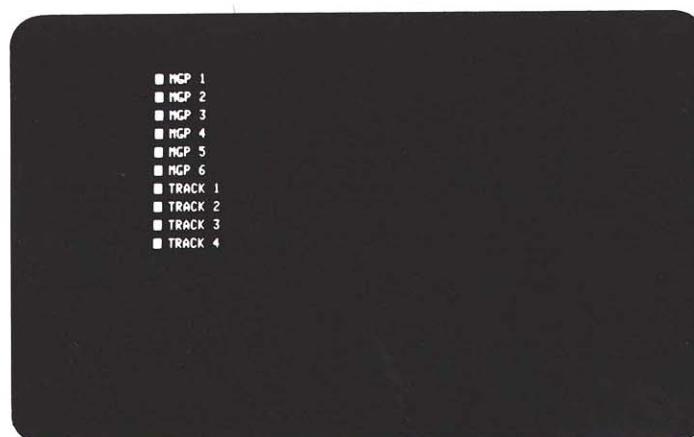
Data Store and Fetch

System 3500's data store and fetch functions allow acquired data to be temporarily stored in some unused portion of data memory for later recall and analysis. Each stored spectrum can be assigned a unique title and assigned to any available location in memory. Any number of channels can be selected for storage as long as there is sufficient unassigned memory available.

When fetching data, a list of the user assigned titles for all stored data is displayed and selected by the light pen for immediate display of that data. Combined with the add, strip, normalize, and overlay functions, data storage provides a powerful facility for manipulating and comparing a variety of input spectra.



Data Storage in Memory.



Directory of Data Stored in Memory.

Extended Analysis Functions

The Extended Analysis Firmware includes a powerful set of analysis functions for nuclear spectroscopy applications and time histogramming applications.

Calibration

System 3500's calibration feature permits precise calibration of the horizontal axis in any units selected by the user such as energy, time, distance, volume, velocity, etc. The requirement for calibration is the availability of two relevant points of known value such as two known energy peaks.

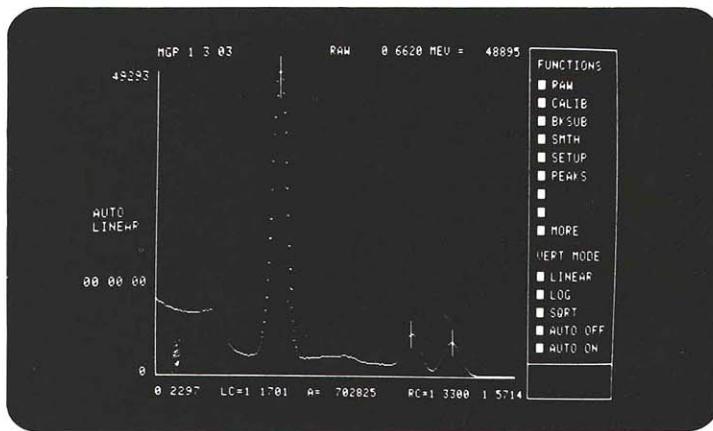
Display prompting guides the user in the calibration process. Once the entries are completed, the horizontal scales and cursor and marker locations display their locations in the physical units selected instead of channel number. The calibration values on the display are retained in both the tabular listing and graphics hard copy output formats. Floating point values of up to five significant figures are accepted for precise calibration.

Background Subtraction

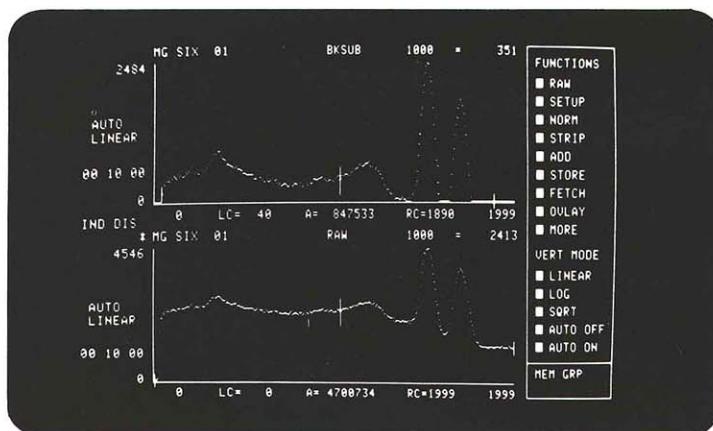
The background subtraction function provides a two-point, straight-line subtraction from any data distribution, including individual energy peaks. The two points used to determine the straight line are calculated by averaging the data around the location of the left and right cursor. The number of points or channels used to determine the average count value at each cursor location is selectable by the user to minimize errors introduced by statistical variations in a single channel's count value.

Smoothing

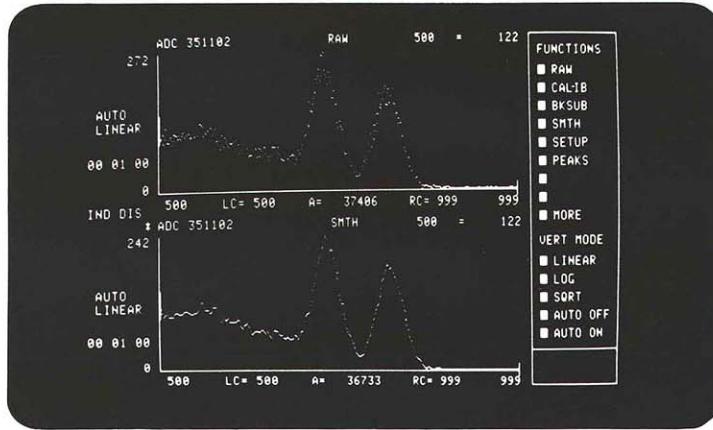
Smoothing provides a convenient and useful means of improving the interpretability of low statistical count data. To improve the use of smoothing, System 3500 provides 3, 5, 7 and 9 point smoothing. When smoothing is selected, a prompt is given requesting the user to enter the level of smoothing desired. After smoothing is executed, the data is available for direct graphics output or storage in an unassigned area of memory for later comparison with other smoothed data.



Energy Calibration with Direct Reading in MeV.



Lower graph shows raw data. Upper graph shows identical spectrum with background subtracted.



Raw and smoothed data on upper and lower graphs respectively.

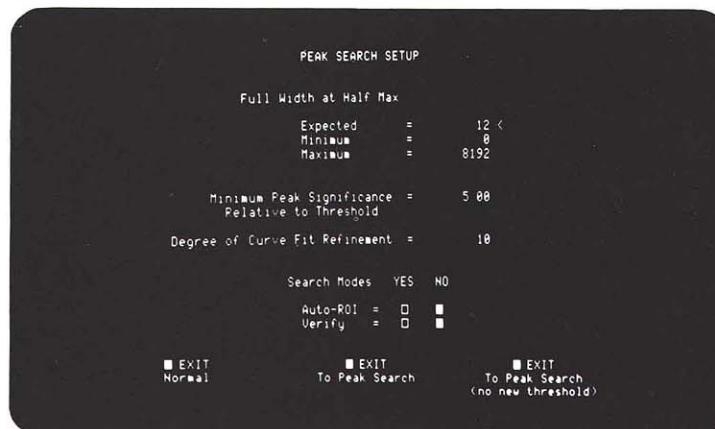
Extended Analysis Functions

Peak Search

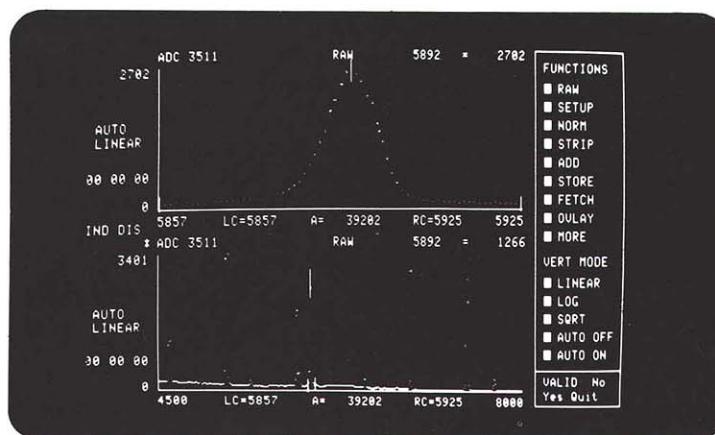
System 3500's firmware-based peak search function is a versatile and powerful peak finding and reporting program. By automatically defining a region of interest about each peak in a spectrum, it relieves the user from manually scanning a spectrum to locate peaks. Several peak detection criteria can be manually entered by the user to optimize the peak search function for the characteristics of the peaks being searched. In addition, the user can opt to manually accept or reject each peak found and can define regions about peaks that are visually determined to be valid. A peak search setup menu enables the user to define manually the range of full-width at half-maximum values of the peaks in the spectra and permits setting the significance of valid peaks relative to background variations in the spectra.

At the completion of a peak search operation, the user may initiate a peak search report. Two types of reports are available: a brief report and a full report. Both reports are output through the RS-232-C port in System 3500 to an interfaced hard copy printing device such as the Model 3931 or Model 3932. A peak search report consists of a peak or region of interest number, the centroid value of that peak, the left and right cursor values, and the count at the peak centroid. The integral count in each peak is also output as total area count, and net area count. To determine these values, each peak is approximated by a Gaussian peak with background approximated by a quadratic polynomial. If a full report is selected, the degree of curve refinement can be selected by the user. Essentially, this specifies the number of iterations performed by the fitting program. The peak search report program also computes the percent area for each peak and references the area to the total area of the spectrum between the cursors on the display, to the sum of all peak areas, and to the sum of all peak net areas.

While peak search is especially useful in nuclear spectroscopy experiments, System 3500's peak search program is also adaptable to peak searching and reporting of data from a variety of distributions including time distributions.



Peak Search Setup
Menu permits user
to define search
criteria.



User interaction
can validate detected
peaks or enter
Regions of Interest
around undetected
peaks.

Peak Search Report (Brief Analysis)							
Peak	Centroid	Left	Right	Peak Count	FWHM	Area	Net Area
1	4601	4588	4614	1057	1.05E1	1.739E4	1.196E4
2	5111	5095	5127	9249	1.295E1	4.231E4	3.744E4
3	5892	5376	5908	2526	1.235E1	3.486E4	2.942E4
4	5879	6563	6895	237	1.235E1	4.038E3	3.141E3
5	5456	7440	7472	2755	1.235E1	3.857E4	3.736E4

Peak	Percent Area Summary		
	Peak Area Area between cursors	Peak Area Sum of Peak Areas	Peak Net Area Sum of Net Areas
1	4.07	12.65	10.83
2	9.90	38.78	31.38
3	8.15	25.36	24.66
4	3.34	2.93	2.63
5	9.09	28.28	31.31

Press any key to continue

Extensive Peak
Search Report
program outputs
to line printers
for hard copy.

Auto-Analysis

The Model 3900-2 Auto-Analysis Firmware offers users the capability of fully automating collection, analysis, manipulation, and output of data with System 3500. Signals can be output to control some experimental parameter or can be accepted to signify completion of an operation external to the 3500 such as automatic sample changing.

Built-in program looping with multiple nesting of loops permits repetitive tasks to be performed without user intervention, and selectable time delay instructions offer the flexibility to interact with external operations without need for intricate handshake timing.

Auto-Analysis is completely contained in the firmware of System 3500 and includes all facilities for creating, executing and editing programs. Any logical sequence up to 600 MCA operations can be entered, stored, and executed. Included are all setup operations, start, stop, memory clear operations, all standard and Extended Analysis operations, and all output operations. If the system includes the software option of Model 3921 Dual Drive Floppy Disc Accessory, Auto-Analysis can even call and execute user defined FORTRAN programs. When execution of the FORTRAN program terminates, it returns control to the 3500's Auto-Analysis program. No other MCA offers automated operation and control with computational power and flexibility comparable to System 3500.

Creating an Auto-Analysis program consists of performing, in logical order, all the light pen, keyboard, and control pad operations that would otherwise be manually performed for an experiment. When a repetitive operation is required, such as counting 100 samples, a loop can be inserted to acquire, analyze and output or store data for 100 cycles. By nesting a loop within a loop, these 100 samples can be repetitively batch-counted with provision for changing a detection parameter such as gain or intensity for each 100-sample cycle.

If sufficient memory is available, it may be desirable to store data for successive samples independently for later recall and review before analysis and output. A data offset instruction automatically stores data in sequential memory locations. Sequential titles of each sample's

stored data can be generated automatically for convenient and organized recall.

After a program is created, it can be verified by single-step execution of each instruction and modified if necessary. System 3500's editor displays a listing of multi-page programs with line-by-line instructions each corresponding to an operation step. Insertion or deletion of instructions is quickly and easily implemented by setting a pointer to the line being modified. Editing is further simplified by a help command which displays a list of step and modify instructions.

If the floppy disc accessory is included with the system, multiple Auto-Analysis programs can be saved on a diskette and conveniently fetched for execution. A library of Auto-Analysis programs can be created and stored to completely automate setup and operation of any number of different experiments.

Disc I/O

In System 3500's containing the Model 3921 Dual Drive Floppy Disc Accessory, a disc I/O program is included to conveniently save and restore complete data files for later review and analysis. A disc data file contains all raw data in a memory group assigned to an input module, or it can be a file from a stored memory group on which some processing such as smoothing or stripping has been performed.

When the saved file is from an input module's memory group, the complete setup state of the experiment is also saved so that the experiment can be resumed or repeated later without repro-

gramming System Architecture and Module Parameters. All data related to the original acquisition is saved, including acquisition time, conversion gain, channel calibration and even all regions of interest defined in the memory group. *This exceptionally thorough and convenient archiving facility saves untold hours of manual logging of experimental parameters and minimizes the possibility of logging errors.*

Restoring a data file is equally convenient and efficient. The file name is simply typed in at the keyboard and data is automatically loaded from the disc. Alternatively, a menu of all data files stored on a particular diskette can be displayed for light pen selection of any file or files from disc. Up to 9 files of 8k channels each or sixty 1k files with full experimental status headers can be stored on each single density floppy diskette, providing a very compact archiving facility.

ISOLIB/ISOID

(3910-20)*

The ISOLIB/ISOID Software Option offers the capability of associating peaks in a spectrum with reference peaks stored in a library. The user may enter his own library, or use the 46-peak reference library supplied on the disc. Multiple libraries can be combined using the MERGE command. After the unknown spectrum peaks have been compared with the desired library, a report can be viewed on the screen or printed out to a printer via the RS-232 port.

*Included with each 3500MP; not available for 3500M



Auto-Analysis Menu.

```

RESET          loop 3
SYSTEM ARCHITECTURE   2ND FUNCT, CL DAT, START
SLOT 2, USER    ACG, START
RESET          wait update
MODULE SETUP   output 8
*TRACK*        pause time, 18
RETURN         STORE
ESC           *TRACK*
RETURN         title number
ESC           RETURN
RETURN         data offset
light pen 168 light pen 164
end
RESET         end
OUTPUT SETUP  RESET -
ESC           2ND FUNCT, SG DIS
RESET         loop 18
ESC           M GRP
2ND FUNCT, SG DIS LEFT CCSR
2ND FUNCT, CL ROI, START ESC
H GPP          RETURN
MORE          RIGHT CCSR
COUNT         ESC
ESC           RETURN
RETURN        MORE
MORE          CALIB
left down arrow

```

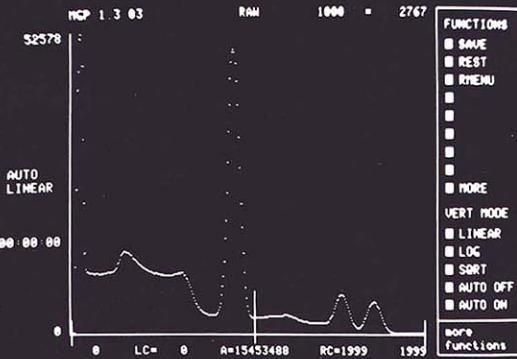
```
ESC      ESC
RETURN   end
ESC      EXIT
RETURN
ESC      quit
RETURN
SETUP
ESC
DISP MODE
DF PCI
ROI
2ND FUNCT: DEL OS
RETURN
left down arrow
LEFT CPSR
ESC
RETURN
RIGHT CPSR
ESC
RETURN
2ND FUNCT: OUTPUT START
ESC
RETURN
ESC
FETCH
```

Multiple page Auto-Analysis program listing showing looping commands and pointer for editing.

LeCroy 3500 MultiChannel Analyzer Auto-analysis

- CREATE
 - RUN
 - STEP
 - MODIFY
 - STORE
 - FETCH

File name TRAC4



Storing and Fetching Auto-Analysis Programs with Model 3921 Floppy Disc Accessory.

- MGTWO 01
- MGTWO 02
- MGPI 01
- MGPI 02
- MGPI_3 03
- MGPI_1 04
- MGTHREE 01
- ADC3511 01
- ADC3511 02
- MGFOUR 01
- MGONE 01
- MGTWO 03
- MGSIX 01

Press arrow keys for more
Restore for: Display Acquisition

Directory of Disc Files.

ISQLIB	TYPE	
1	FE-55	6 0000000
2	CO-57	14 0000000
3	AM-241	14 0000000
4	AM-241	18 0000000
5	I-129	48 0000000
6	AM-241	59 0000000
7	BA-133	81 0000000
8	CD-189	88 0000000
9	SE-75	121 0000000
10	EU-152	122 0000000
11	CO-57	122 0000000
12	SE-75	136 0000000
13	CO-57	136 0000000
14	TE-123H	159 0000000
15	SE-75	265 0000000
16	BA-133	276 0000000
17	HG-203	279 0000000
18	SE-75	288 0000000
19	BA-133	393 0000000
20	EU-152	344 0000000
21	BA-133	356 0000000
22	BA-133	384 0000000
23	SE-75	481 0000000
24	NA-22	511 0000000

Isotope Identifications using 3910-20 ISOLIB/ISOID Software

```

A>
A>
A>
A>ISOID CS137.99

Energy window (in KEV) = 2.0

Isotope library name = LIBRARY LRS

Isotope identification report

Spectrum: CS137_99
Library file: LIBRARY LRS
Energy window: 2.00 KEV

Energy = 0.0000 # CH2+ 11376 # CH+ 0.0000 KEV

Centroid Energy Area Net area Isotopes
channel KEV

1768.79 201.22 3635E+09 2681E+08
5984.53 660.25 1204E+10 1052E+10 00.127

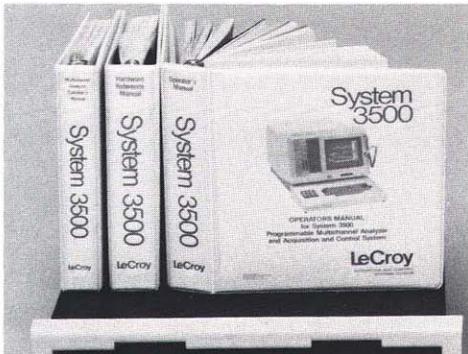
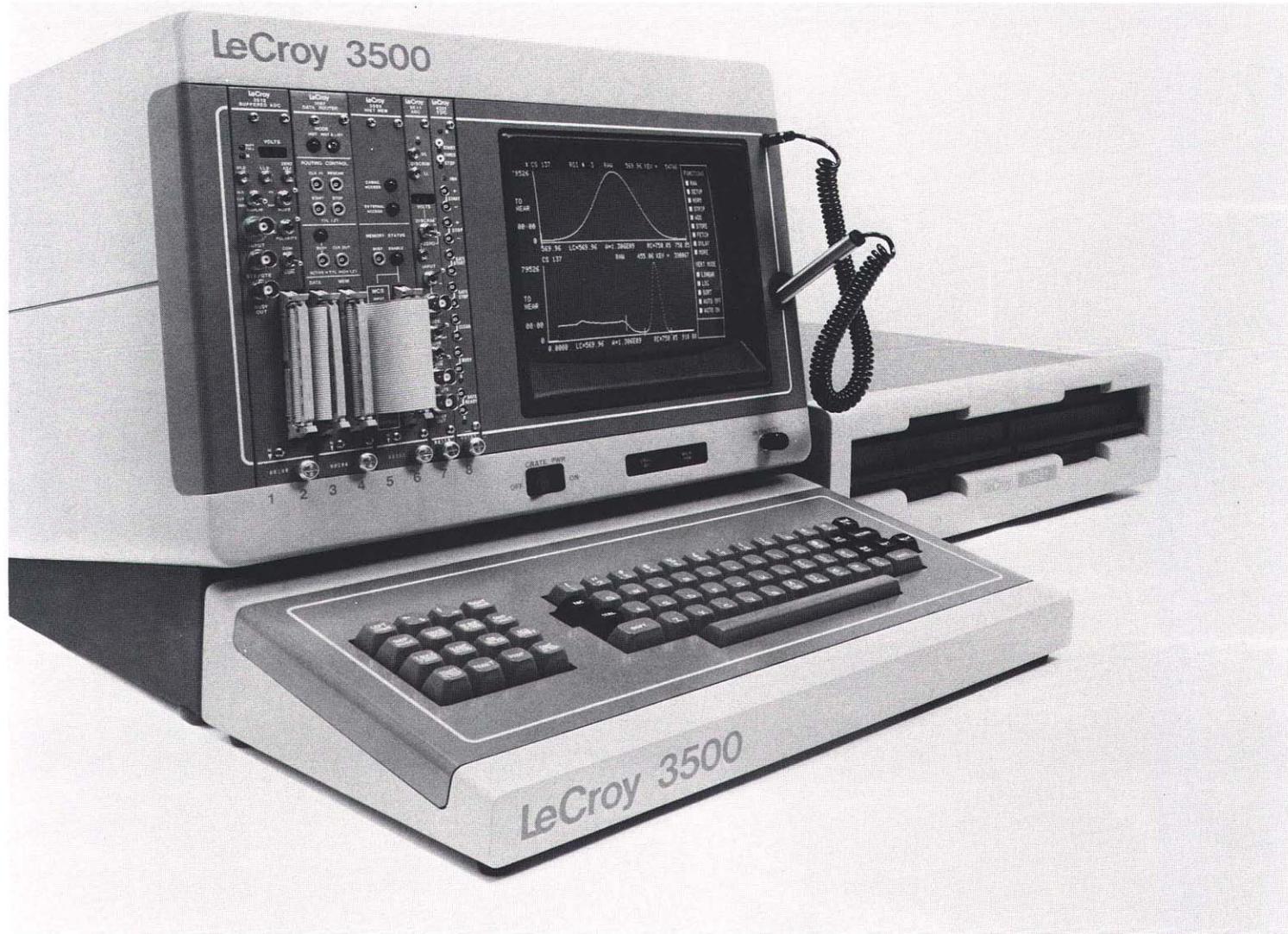
```

Accessories and Peripherals

In addition to the variety of compatible CAMAC input and control modules, System 3500 offers a wide range of accessories and peripherals for printing,

plotting, strip chart recording, data storage on diskette or magnetic tape and controlling GPIB devices. All are fully supported with necessary firmware or

software making system 3500 a truly complete system.



Hard Copy Output Devices

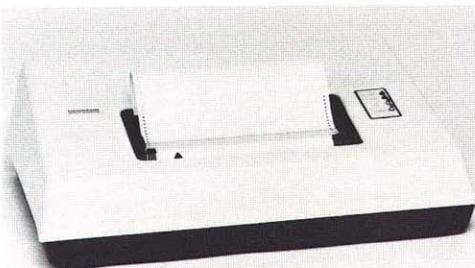
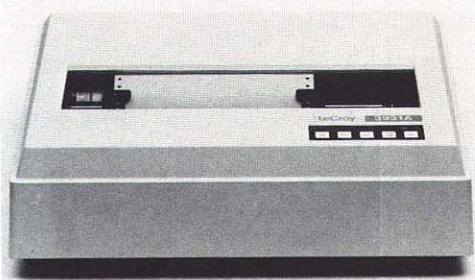
LeCroy offers one fully supported hard copy device for System 3500. However, any current-loop or RS-232-C compatible printer such as a TTY or a Decwriter* is also directly hardware and software compatible. With the 3500's Model 3500-38 GPIB accessory, any GPIB device, including printers and plotters, can be readily interfaced with the GPIB support software.

System 3500 can be configured as a complete turnkey system with facilities for software programming and unsurpassed acquisition, analysis, and output flexibility.

Accessories and Peripherals

Model 3931A Printer/Plotter

The Model 3931 is a compact, inexpensive line printer with full graphics plotting facilities. This dual capability makes it exceptionally useful in experiments requiring both tabular listings of data as well as plots of the graphic display. The graphic output to the 3931A is a "screen dump" in which the display is exactly duplicated by the plotter including alphanumerics. This exclusive feature permits the user to select and view exactly the data to be output. The print speed of the 3931A is 90 characters/second and the screen dump plot is executed in approximately 90 seconds. Fanfold paper measuring 9 x 11 inches is continuously fed by a pin feed mechanism.

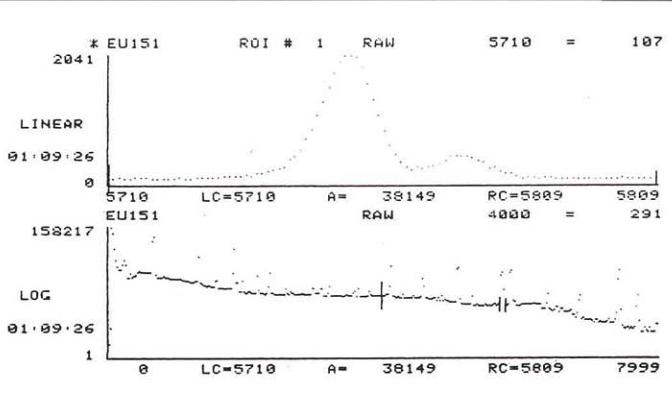


LeCros 3511 ADC PARAMETERS											
TITLE: EU151											
ACQUISITION DURATION = 01:09:26											
(HH:MM:SS OR "INFT")											
CONVERSION GAIN = 8K											
DATA MODE (0=ADD,1=SUB) = 0											
ACQUISITION TIME = 01:09:26											
AREA = 38149											
START CHANNEL = 5710											
STOP CHANNEL = 5809											
EU151 ROI # 1											
% AREA = 38											
AREA = 38149											
5710: 107 97 116 100 95 104 106 110 100 84											
5720: 100 88 95 109 96 99 104 107 107 114											
5730: 106 125 124 131 137 158 139 172 165 220											
5740: 239 280 287 400 453 543 731 882 1110 1315											
5750: 1543 1755 1919 2021 2041 2011 1853 1606 1344 1105											
5760: 858 621 481 353 284 244 275 251 277 290											
5770: 314 389 436 463 446 450 428 383 363 267											
5780: 286 216 181 169 127 100 110 114 91 116											
5790: 108 86 89 90 91 88 103 93 72 90											
5800: 100 89 83 104 88 88 97 102 95 79											

Extended tabular output showing channel address and counts per channel of Region of Interest #1 displayed in "screen dump" output.

LeCros 3511 ADC PARAMETERS											
TITLE: EU151											
ACQUISITION DURATION = 01:09:26											
(HH:MM:SS OR "INFT")											
CONVERSION GAIN = 8K											
DATA MODE (0=ADD,1=SUB) = 0											
ACQUISITION TIME = 01:09:26											
AREA = 7490993											
START CHANNEL = 0											
STOP CHANNEL = 7999											
EU151 ROI # 1											
% AREA = 38											
AREA = 38149											
EU151 ROI # 2											
X AREA = 49											
AREA = 51862											
START CHANNEL = 5810											
STOP CHANNEL = 6009											
EU151 ROI # 3											
% AREA = 15											
AREA = 15893											
START CHANNEL = 6326											
STOP CHANNEL = 6525											

Summary tabular output of 8000 channel EU-151 gamma spectrum showing three Regions of Interest, their respective start and stop channels, area count and % of counts relative to total count in all Regions of Interest.



"Screen Dump" Graphic Output duplicates System 3500 8000 Channel EU-151 gamma energy spectrum.

Data Storage and Software Supported Accessories

Model 3921

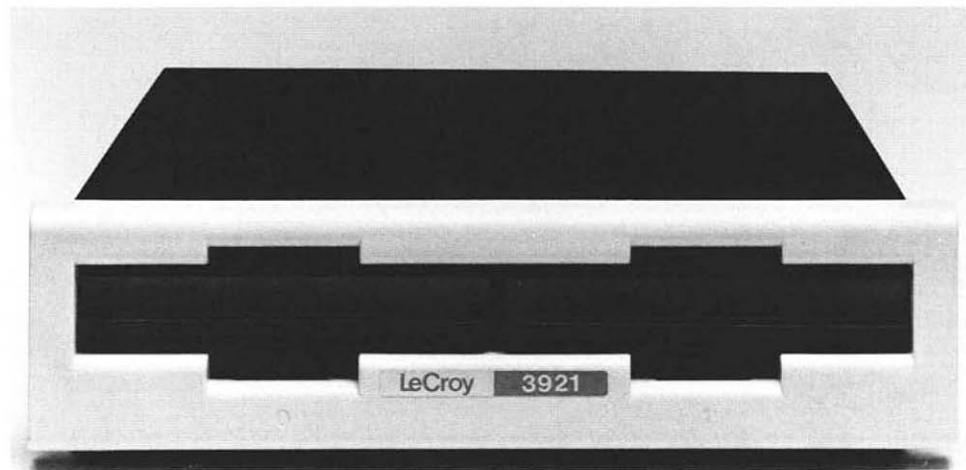
Model 3921 Dual Drive Floppy Disc is included with the Model 3500MP and is available as an add-on accessory for either the 3500M or 3500MP. In single density mode, it provides 243K bytes of data or program storage per drive in IBM 3740 format. Double-density mode increases the storage capacity to 486K bytes per drive. Since single or dual density is defined by initial system formatting tracks on the diskette, the system can automatically read and write both single and double density diskettes interchangeably.

Where needed, a second dual disc drive may optionally be added to a system to provide increased on-line storage capacity.

In addition to providing data storage, Model 3921 provides complete software programming facilities in a high level language for user access to the 3500's

microprocessors and computer memory. CP/M operating system, assembler, and FORTRAN-80 compiler are provided as standard. Model 3910-3A BASIC-80 interpreter and compiler are available as an option. The system software includes extensive graphics, plotting, and CAMAC and multibus I/O routines to fully automate data collection, control, analysis, and communication with other computers.

Included in the software is an especially powerful facility called User Analysis which allows user-written high-level programs to be embedded in the 3500's memory and executed in a manner identical to resident MCA firmware functions. Effectively, the user can customize analysis algorithms to create specific MCA functions like peak search, statistical analysis, or control and output routines.



Model 3921 Dual-Drive
Floppy Disc Accessory.

Model 3500-38 GPIB Interface

The Model 3500-38 General Purpose Interface Bus is a plug-in board accessory which provides access from the System 3500 to over 300 different instruments and computer peripherals using the GPIB (General Purpose Interface Bus)*. When installed on the Multibus of System 3500, it is a one-board, self-contained intelligent controller or listener/talker.

The 3500-38 interprets a sequence of high level instructions placed in its memory by the System 3500 and performs all of the bus protocol required to communicate over the GPIB. Model 3500-38 contains an asynchronous, parallel I/O processor which allows the program in the System 3500 to concentrate on system requirements, not on the bus. A complete software support package is supplied with the 3500-38 including I/O routines for operation as a controller or listener/talker.

*GPIB is an implementation of the IEEE Standard 488-1975: "Digital Interface for Programmable Instrumentation."

Model 3500-35 Quad Serial Port Interface

The Model 3500-35 Quad Port Interface to RS-232-C is a plug-in board accessory that provides four bidirectional interface ports for System 3500 in addition to the RS-232-C interface built into the standard system. Multiple ports are necessary in configurations of System 3500 that require simultaneous serial connections to devices such as:

Model 3931A Printer/Plotter
Accessory,

A direct serial link to a host computer for data transfer and/or control,
Connection to data sets or data terminals for data transfer by means of Modems.

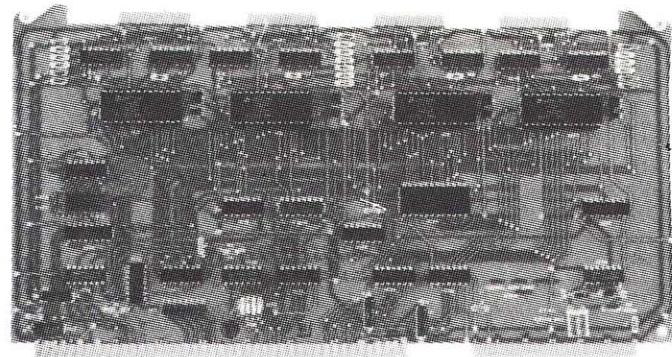
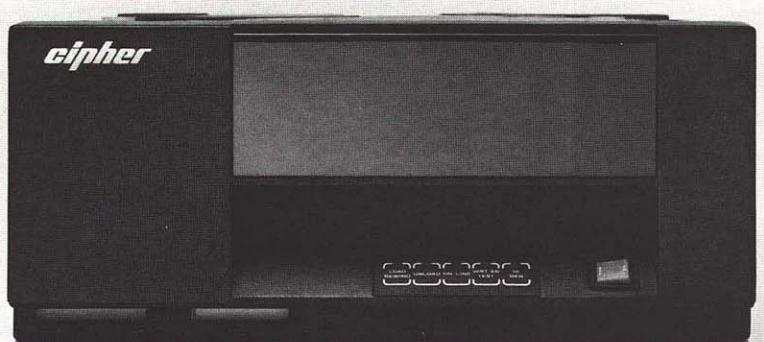
Data Storage and Software Supported Accessories

Magnetic Tape Drive Accessories

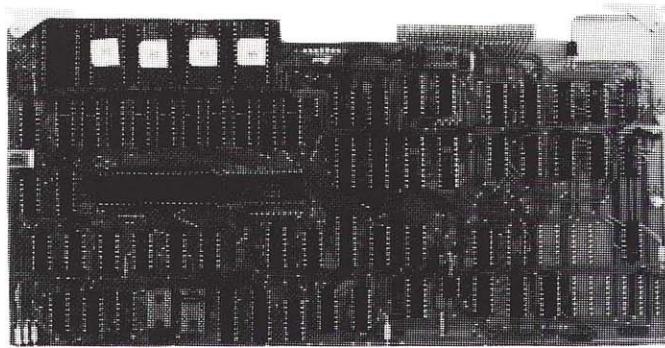
The System 3500 supports a 9-track tape accessory. The Industry Standard tape drive has a 25 inch per second (IPS) speed in normal mode, and 50 or 100 IPS in streaming mode with maximum data densities of 3200 bite-per-inch (BPI) at 50 IPS and 1600 BPI at 100 IPS. Standard tape length is 2400 feet. System combinations are as follows:

Model 3965 includes only the 9-track tape drive accessory for either rack or bench-top mounting. Firmware and software for 3500M interfacing are supplied.

Model 3965
Tape Drive Accessory.



Model 3500-35
Quad Serial
Port
Interface.



Model 3500-38
GPIB
Interface.

Software

Programmable System 3500s are supported with high level languages including FORTRAN and BASIC and extensive utility subroutines and calls for CAMAC I/O, RS-232-C I/O, Disc I/O, plot and APU libraries and support of Multibus accessory boards. The following is a partial list of various software facilities currently available:

Model 3910-1 Disc Operating System

The 3910-1 contains the Disc Operating System of the Model 3921 Dual Drive Floppy Disc Accessory for System 3500 which provides for disc management and program construction, storage, editing, assembling, and debugging. It is supplied on a single diskette with the 3921.

Model 3910-2A FORTRAN-80 Software

The 3910-2A contains all programs necessary to create and execute FORTRAN programs with System 3500 and Model 3921 Floppy Disc Accessory. It includes a FORTRAN compiler, linker, library, library manager, and a macro assembler on a single diskette. It is one of two high level language choices for System 3500 and Model 3921.

Software

Model 3910-3 BASIC-80 Software

The 3910-3 provides all programs necessary to create and execute both compiled and interpreted BASIC programs with the System 3500 and Model 3921 Floppy Disc Accessory. It includes a BASIC interpreter, compiler, linker, library, library manager and macro assembler on a single diskette. BASIC can be substituted for FORTRAN at no extra cost or can be purchased in addition to FORTRAN. Interpreted BASIC programs can be created and executed to verify program operation. Then, the file can be compiled and linked to speed the execution time.

Model 3910-4 BASIC Support Software

Model 3910-4 consists of a variety of subroutines for performing CAMAC I/O, graphics display and output, I/O to the RS-232-C port, accessing data memory, and linking the arithmetic processor to a BASIC program for hardware arithmetic operations. A set of utility programs is also included to access FORTRAN subroutines. The 3910-4 is supplied with 3910-3 on a separate diskette.

Model 3910-5 FORTRAN Support Software

Model 3910-5 consists of a variety of subroutines for performing CAMAC I/O, graphics display and output, I/O to the RS-232-C port, accessing data memory, and linking the arithmetic processor to a FORTRAN program for hardware arithmetic operations. The 3910-5 is supplied with 3910-2 on a separate diskette.

Model 3910-6 MCA Support Software

The Model 3910-6 contains a special MCA version of the Disc Operating System to permit direct software compatibility with the MCA firmware of System 3500. It also contains a variety of executable programs including System 3500's Disc I/O facility for saving and recalling data and parameter files and Auto-Analysis program files. Other programs include a spectrum overlay program for vertical movement of one spectrum about another and a fast update real time display program. Sample Nal and GeLi derived data files are also included. This software is supplied on a single diskette with the 3921.

Model 3910-7 User Analysis Software

Model 3910-7 includes the special MCA Disc Operating System, Disc I/O, Overlay, and Real Time Display program but also includes relocatable files which can link a user-written FORTRAN program to the MCA. The user program can be executed by a light pen command from the Function Menu on the graphic display. Several user analysis programs are provided in source code as examples. The user program can provide virtually every operation with the 3500 system afforded by FORTRAN, including CAMAC, I/O, data analysis, Serial I/O, GPIB I/O, and special graphics displays and output. The 3910-7 is supplied on a single diskette with the System 3500 MCA and Model 3921 Disc Drive.

Model 3910-8 System Checkout Software

The 3910-8 contains a variety of diagnostic tests for verifying proper operation of the display, arithmetic processor, computer memory, keyboard, and disc drive. It is supplied with all disc-based System 3500s on a single diskette and contains interactive messages to the user for execution of test routines.

Model 3910-9 Disc Utility Software

This software package is supplied with all disc-based System 3500s on a single diskette and includes programs for formatting blank diskettes, copying and comparing diskettes, and operating System 3500 as a computer terminal.

Model 3910-11 GPIB Software

When System 3500 is equipped with Model 3500-38 GPIB Interface Board, the Model 3910-11 is supplied on a single diskette which contains software drivers to support GPIB.

Model 3910-12B Diagnostics Software

This software, combined with built-in diagnostic firmware, tests memory, the serial I/O port, keyboard and lightpen interrupts, and display. It is supplied on a single diskette with Model 3500MP.

Model 3910-14 Quad Serial Interface Software

The Model 3910-14 contains programs and FORTRAN subroutines to support the Model 3500-35 Quad Serial Interface Board option. It is supplied on a single diskette with the Model 3500-35. Routines include a computer terminal and a serial I/O program to help configure any of the four ports for the desired use.

Model 3910-15 Screen Oriented Text Editor

The Model 3910-15 provides vastly improved text editing capability so that programmers have fast thorough control of program content and structure. A movable cursor, controlled by a keypad, permits direct access to text locations to delete, insert, change, or move copy. The editor also provides full Word Processing facilities. This single diskette and a complete User's Manual are an option to System 3500.

Model 3910-17 9-Track Magnetic Tape Software

This software provides data archiving facilities for use with Model 3500MP. It permits storage of all experimental data and description as with Disc I/O. It is supplied on a single diskette with Model 3965.

Model 3910-19 Reformatter CP/M to RT-11*

The Model 3910-19 reformats CP/M floppy diskette files to RT-11 formatted files and the reverse. This provides 3500 users access to PDP-11* system software for data analysis and reduction. It also permits RT-11 data files to be displayed, analyzed, and manipulated by 3500 software. It is supplied with a detailed User's Manual on a single diskette as an option to System 3500.

* PDP-11 and LSI-11 are trademarks of Digital Equipment Corporation.

Specifications

General Description

System 3500 is a complete acquisition, control, and analysis system. Major components include: 1) 8-module CAMAC minicrate for acquisition modules; 2) 9" CRT Display; 3) ASCII keyboard; 4) 23-function control pad; Central, display, and arithmetic microprocessors; 6) Computer memory; 7) Power supply; 8) Serial I/O port. System 3500 also includes 8k data memory, light pen and firmware for multichannel analyzer acquisition, display, analysis, and output.

Data Acquisition

System 3500 can acquire in two basic ways: through Direct Memory Access (DMA), under firmware and hardware control, and through the CAMAC data-way under software control.

DMA Acquisition Modes

Pulse Height Analysis—
Model 3511/3514 ADC Module

Multichannel Scaling—
Model 3521A MCS Module

Time Analysis—
Model 4201/4204 TDC Modules

Acquisition Rates

PHA- up to 350 kHz throughput

MCS- up to 100 MHz count rate and
1 μ sec minimum dwell time/channel

TDC- up to 1 MHz throughput

Acquisition Stop Control

Acquisition can be terminated manually, by preset time or number of sweeps, or by external signal control through an optional 16-bit register module.

Preset and Elapsed Time Range for Each DMA Input Module

1 second to 100 hours in 1 second increments programmed for each module during module setup.

Preset Live/Real Time Range (PHA Acquisition Mode)

1 to 900,000 milliseconds or seconds.
(Programmable in Model 3541 Dual Deadtimer Module.)

Preset Number of Sweeps (MCS Acquisition Mode)

From 1 to 65,535 or infinity can be selected, limited only by the first channel to reach 16,777,215 counts which is determined by the input rate and dwell time per channel.

Multiple Inputs

Eight DMA inputs through the CAMAC minicrate. Over 20 inputs total with addition of an external CAMAC crate.

Data Memory

Size

8192 channels by 24 bits (16,777,215 counts) per Data Memory Board, Model 3500-2.

Type

Solid state static RAM (available with battery backup) Model 3500-2B.

Segmentation

Up to 32 memory groups of 256 channels (16 at 512 channels, 8 at 1024 channels, etc.).

Expansion

System 3500 can accept 8 Data Memory Boards providing 64k total memory. Memory can be flexibly configured such that 1 to 8 memories can be associated with the minicrate or an external crate. This permits maximum inputs with maximum resolution. For example, with 64k of memory assigned to a 20-input module external crate, each DMA input can have a maximum of 2k channel resolution.

Control

System operation and control is provided through a dedicated 23-function, 16-key control pad, an ASCII keyboard, and a light pen.

Display

Nine-inch CRT for display of spectral data, graphics with alphanumeric annotations, setup programs, channel number and count, and FORTRAN or BASIC program listings.

Resolution

256 vertical×512 horizontal picture elements.

Controls

Front Panel Intensity Control.

Display Graphics

Vertical Modes

Linear, Logarithmic, and Square Root vertical scale with selective autorormalize for each mode.

Vertical Maximum and Minimum

Selectable from 0 to 16,777,215 counts full scale.

Horizontal Maximum and Minimum

Selectable from 0 to 8,191 channels.

Single or Dual Graph Display

One or two graphs of spectra with alphanumerics. Dual graphics can contain total memory and a memory group, two independent memory groups, or a memory group and a region of interest. Both graphs display marker and dual cursors.

Alphanumeric Annotations on Graphs

Vertical and horizontal maximums and minimums, marker channel location and count value, left and right cursor channel locations, area count between cursors, six-digit time display, vertical mode state and menu, graph title, data state, analysis function menus and prompt instructions.

Setup Program Status Pages

System Program, Module Program, Output Program, Auto-Analysis Program Disc I/O Program, Peak Search Program, and Strip/Normalize Program

Display Manipulations

Cursors and Marker

Dual cursors plus one marker on each graph. Total area between cursors and marker count continually updated. Bidirectional accelerated movement of cursors and marker provided by push-button. Right cursor linked to left cursor positioning creating region of interest window.

Regions of Interest

Up to 255 regions of interest can be defined from 1 to 8,192 channels/region of interest. Regions of interest can overlap and lie within one another. Dual cursors define region of interest channel spacing.

Memory Groups

8,192 channels of data memory can be segmented into memory groups of 256, 512, 1,024, 2,048, 4,096, or 8,192 channels each. E.G. 32 memory groups of 256 channels each can be defined. All defined memory groups can be displayed together or any two can be selected for expansion and display simultaneously.

Specifications

Analysis Functions

Three levels of analysis functions are available:

Standard

Add, strip, normalize, area integration, offset, store, recall, and overlay functions are standard and are light pen selectable from the Function Menu.

Extended Analysis Option

Model 3900-1 includes linear calibration of the horizontal axis in any units individualized for each memory group; linear background subtraction from individual peaks from 3 to 8,192 channels or from memory group; 3, 5, 7 and 9 point smoothing of any memory size; and peak search and reporting facilities including 2nd order polynomial background subtraction and net area readout.

Auto-Analysis Option

Model 3900-2 provides for programming and storing over 600 steps of sequential keystroke or light pen commands with automatic execution. Full editing facilities and disc storage and recall of programs are included.

Microprocessors and Memory

Central Processor

8085A (10 MHz)

Computer Memory

64k×8-bit implemented with 16k×1-bit dynamic RAM.

Read Only Memory

30k×8-bit EPROM (2716) contains standard MCA firmware programs for acquisition, display, analysis, and I/O.

Scratchpad Memory

1k×8-bit (CMOS static RAM, battery backed-up).

Video Processor

8085A with private 8k×8-bit EPROM and 8k×8-bit RAM.

Arithmetic Processor

AM9511; 3.3 MHz provides 32-bit floating point hardware multiply, divide, transcendental functions, etc. (See APU data sheet for typical execution times.)

Display Memory

128k bits of 16k dynamic RAM. Integral 16-bit light pen register.

I/O Buses and Ports

Serial I/O Port

Conforms to EIA-RS-232-C. Baud 75 to 19,200 (hardware programmable). Wired as a data terminal (DTE). Signals can be rearranged with optional 3500-81 breakout box or converted to current loop with 3500-80. Modem control and handshake signals are:

- 1 Request to send;
- 2 Clear to send;
- 3 Data Terminal Ready;
- 4 Data Set Ready.
(Can generate interrupt on receipt of serial input character.)

Video Display Output

Composite video output (RS-170) provided on rear panel BNC connector.

CAMAC Minicrate

8-slot

Power available with Standard System 3500 Configuration.

+ 6V	50.9 amp
- 6V	11.9 amp
+12V	8.8 amp
-12V	9.9 amp
+24V	3 amp
-24V	3 amp

CAMAC Controller

Conforms to IEEE (583) 1 μsec cycle. Provided to allow LAMs to generate system interrupt. 24-bit read and write capability.

Computer Crate (Multibus) IEEE 796 type (SBC)

Power used in Standard System 3500 Configuration.

+ 5V	30 amp
- 5V	100μ amp
+12V	3 amp
-12V	100μ amp

18 slots are provided. The standard System 3500 MCA uses 7 slots.

System Dimensions, Weight, Temperature and Power Requirements

Dimensions

15.85 inches (40.2 cm) high×17.38 inches (44.1 cm) wide×32.57 inches (82.5 cm) deep. Depth includes keyboard. 24.77 inches (62.9 cm) is depth of mainframe only. Rack mounting by means of optional rack-mounting shelf.

Weight

80 pounds (36 kg.) typical.

Operating Temperature Range

Complete System-10-45 degrees C (32-113 degrees F).

Power Requirements

115/230 volts ac, 50/60 Hz. System 3500, 450 watts (typical with 4 acquisition modules).

Specifications Subject to Change

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Ordering Information

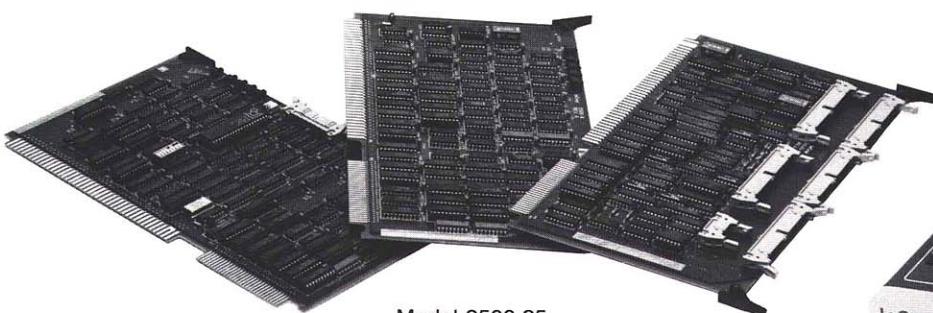
The System 3500MCA is offered in two configurations: Model 3500M and Model 3500MP. The 3500MP is the same as the 3500M but includes the Model 3921 Dual Drive Floppy Disc and Software.

Model 3500M Multichannel Analyzer is supplied with:

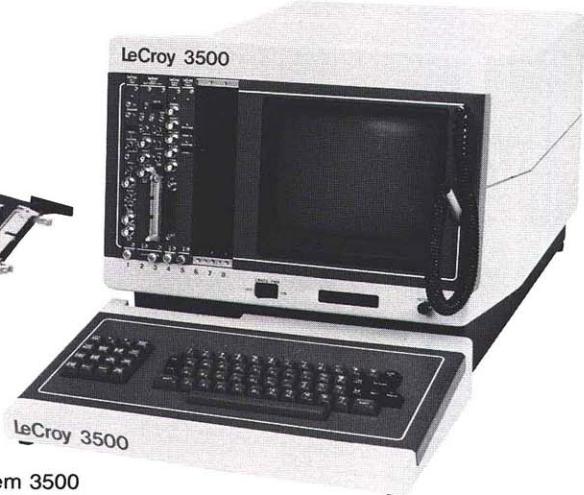
1. All data analysis and display firmware described in this brochure.
2. All acquisition and I/O firmware described.

Model 3500MP includes the above, plus:

1. Model 3921 Dual-Drive Double-Density Floppy Disc,
2. Model 3500-8 Disc Controlled Board,
3. Complete standard system software including Models 3910-1, 3910-2A, 3910-5, 3910-6, 3910-7, 3910-8, 3910-9, and 3910-12B.

Model 3500-25**CAMAC Multibus™ Microprogrammable Controller (MUPC)**

Model 3500-25



System 3500

Features

- A fast, powerful acquisition, display, and processing accessory for System 3500.
- CAMAC* read or write operations at greater than 0.8 MHz rates.
- Provides on-line data flagging such as digital discrimination to histogram or to display pre-programmed ranges of time or pulse height conversions.
- Permits acquisition from any CAMAC module and archiving or display at nearly full CAMAC bandwidth (0.8 MHz).
- Ideal for multiple input high throughput applications such as digital data logging, multi-hit time of flight, multi-parameter pulse height analysis.
- High speed processing: 6 MHz 48-bit microinstruction rate.
- 24-bit bus structure optimized for CAMAC. Full bandwidth for arbitrary Read, Write, and Control.
- Wide, powerful 48-bit microinstruction. 1024 by 24-bit registers and independent 1024 by 48-bit program memory.

* Conforms to CAMAC standard for nuclear instrumentation modules (ESONE Committee Report EUR 4100C or IEEE Report No. 583).

- Modern symbolic assembly language, real time debugging tool and disassembler make the 3500-25 in the 3500 a complete System for software development.
- Fast, direct access to system memory and peripherals.
- Independent 24-bit ALU and 24-bit shift register.
- Capable of addressing a megabyte of System RAM.

Introduction

The Model 3500-25 MUPC is an intelligent, microprogrammable CAMAC and Multibus controller accessory for the System 3500. Its 24-bit architecture allows fast and complex programmable CAMAC operations at greater than 0.8 MHz rates with standard CAMAC modules and 1 MHz rates with 3500-Series CAMAC modules. 3500-Series modules and standard CAMAC modules can be operated simultaneously. Because it is a full capability computer, optimized for CAMAC and Multibus Control, the MUPC provides unprecedented flexibility and speed in data acquisition or control applications.

Multibus is a trade mark of Intel Corporation and conforms to IEEE standard 796-1978.

Description

The MUPC consists of three Multibus boards which reside in the System 3500 housing. The three boards are partitioned into control, arithmetic, and interface functions.

The program control board contains 1 K of 48-bit wide program memory, 256 words of vector (jump address) memory, an Am2910 microsequencer, and associated logic such as a microinstruction (pipeline) register, condition code multiplexer, and clock generator. One microcycle is 167 nsec (6 MHz clock rate); all instructions require exactly one microcycle. This board also contains the I/O interface through which the host computer in the 3500 System can load microcode and initialize or examine the state of the MUPC. The MUPC's microprogram is stored entirely in RAM and can be changed dynamically. For example, the MUPC can acquire data with one microprogram and manipulate it with a different one.

The arithmetic board contains arithmetic logic, a 24-bit universal shift register, a 1 K x 24-bit high-speed memory, and a bus master interface. The on-board memory can store various parameters for data acquisition, such as stop counts, data selection criteria, and data routing information. It can also be used as a data buffer. The bus master interface allows the MUPC to take control of the System 3500 internal bus, giving it direct access to the host computer's memory and I/Q devices. For instance, the MUPC can write data into system RAM at greater than a megabyte/sec.

The interface board contains the CAMAC and Data Memory interfaces. All CAMAC dataway bits can be accessed by the MUPC. CAMAC can be serviced via programmed polling or vectored interrupts (LAM driven servicing). Standard CAMAC timing generation hardware is provided; in addition, the user can specify special timing cycles (e.g. for use with System 3500 DMA-type CAMAC modules) via a programmable timing memory. A private connection to one or more (up to 8) model 3500-2 Data Memory Boards provides 8 K to 64 K by 24-bits of auxiliary memory. Data can be written to 3500-2 memory at 3 million 24-bit words/sec and read out at 2 million 24-bit words/sec.

Applications

Many data acquisition applications involve multiple inputs with high overall throughput rates, often exceeding the data transfer rate of ordinary CAMAC controllers and readout systems.

Examples of such high throughput applications include high repetition rate, multi-hit time-of-flight ex-

periments, multiple input fast data logging applications or multi-parameter nuclear studies.

For these applications, the MUPC is an ideal CAMAC controller and processor. the MUPC is optimized for arbitrary CAMAC read, write, or control operations. It employs a 24-bit CAMAC bus structure with a micro-instruction cycle time of 167 nanoseconds which translates into complex CAMAC transfers approaching the CAMAC bandwidth of 1 MHz (3 MBytes/sec). In addition, transfer of 24-bit data to System 3500 computer or data memory or to peripheral archiving devices such as Winchester or floppy disc or 9-track tape can be achieved almost concurrent with CAMAC read operations. Some applications require data processing such as digital discrimination, flag bits, offsets, etc. before transfer to memory or to a bulk storage device. Depending on the extent of processing, the MUPC can perform a variety of on-line data manipulations at the expense of only a few microcycles in throughput time.

Hardware and Software Compatibility

MUPC is a completely integrated accessory for System 3500 and includes all hardware interfaces and interconnecting cables to data memory, the built-in CAMAC minicrate, or to an external CAMAC crate equipped with the LeCroy Model 3501 External CAMAC Interface Module.

The Model 3910-25 MUPC Software includes a FORTRAN support package which duplicates the standard System 3500 CAMAC I/O subroutines. Effectively, existing FORTRAN programs written on System 3500 can be relinked to duplicated MUPC subroutines, recompiled and executed to use the MUPC in place of the Model 3500-5 CAMAC controller existent in the System.

Other software included with Model 3910-25 in the MUPC software package is a symbolic microassembler (MU) and a debugger (MUD). The MUPC has been designed so that microprograms can be written and debugged directly from the System 3500 with no external development system or hardware.

The microinstruction set itself is quite straightforward: it has been designed to minimize the number of special rules a programmer must keep in mind while writing code. Independent shift register, ALU, sequencer and interface control fields result in a high degree of parallelism. (See Sample Program)

MUPC programs run independently from System 3500 processor programs. Communication between programs permits sequential or parallel processing. High level language programs in the 3500 processor can offload I/O or arithmetic-intensive tasks to the MUPC to optimize system performance.

SAMPLE PROGRAM

```

;-----  

; RDOUT -- Read data from 2256          20 MHz Waveform Digitizer  

0070 4e0ef000e008 RDOUT: M2256,s -> lmask      ;Look for 2256 LAM only  

0071 0e0eb000e200 NEWL -> cctrl      ;Take new LAM value  

0072 2e8e0000e190 NUMDAT -> s.CTR      ;Set up loop  

0073 0e0e8000e18f NEW - 1 -> dmed      ; to store data  

0074 000000073074 RDWT: cjp.lamc RDWT      ;Wait for LAM from 2256  

0075 0eaad000e020 RDLP: s.N2256 ! F2 -> cnfa      ;F(2) to read  

0076 00000000e000 clr -> none      ;No-or prevents outrunning CAMAC  

0077 08f68040e000 dmed + s.INC -> dmed camso      ;Set up data mem, address and  

0078 00000080e000 dmen      ;initiate CAMAC  

0079 2e820880e001 s.CTR - $1 -> s.CTR ls dmen      ;Decrement loop counter  

007a 290e0000e000 dmr -> s.0      ;Add in old value and store  

007b 0a0690933075 cmcr + s.0 -> dmw dmen cjp.st RDLP  

007c 00000010a000 crttn  

;-----  


```

Sample Program

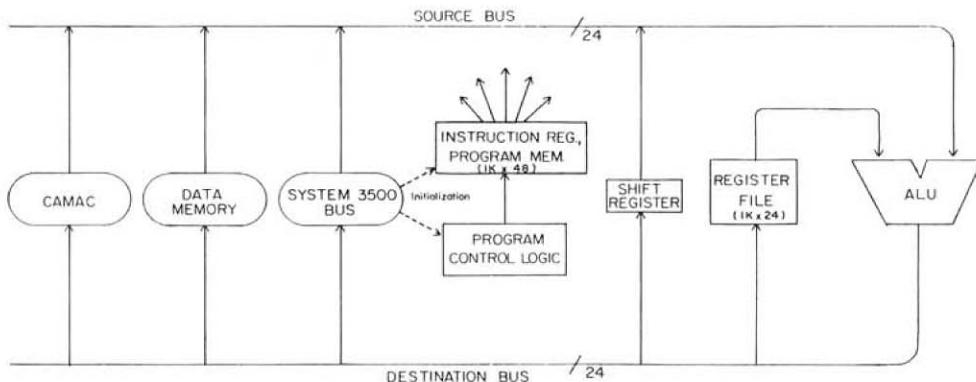
Above is part of the listing for a signal averaging program. This subroutine reads out a LeCroy 2256A Waveform Digitizer. Symbolic constants, defined elsewhere, are capitalized; MU Keywords are in small letters. Each line shows program counter and object code (in hex) followed by the source code. Line 7b is an example of the parallel operations permitted by the MUPC's wide microinstruction. The following op-

erations take place simultaneously: the CAMAC read lines (cmcr) are added to the value building up in the data memory (dmr was put in register g.0 in line 7a) and written back into the data memory (dmw); the data memory is enabled (dmen); and a jump (cjp) occurs back to the top of the loop (RDLP) conditional on the loop counter still being greater than zero. The loop counter was decremented in line 79, with arithmetic status bits being latched (ls) for future use (in line 7b).

P	47	46	45	44	43	40	39	36 35	32 31	28 27	26	24	23	22	21	20 19	16 15	12 11	8 7	4 3	0
P	S	R	W	E	G	Y	G	SRC	REG	ALUOP	DEST	L	S	SROP	D	C	A	T	SEQOP	CONST	
ARI	SWAP											MEN	C	AGO							
Y																					

SRC	ALUOP	DEST	SROP	COND	SEQOP	CONST
ONES	Ø	CLR 0	NONE Ø	HOLD Ø	IØ T	JZ Ø Ø
SR	1	-S 2	STAT 1	LOAD 1	LT 11	GJS 1
PAGE	2	-SC 3	PAGE 2	ASL 2	EQ 12	JMAP 2
SBC	3	-R 4	SCTRL 3	ASR 3	GT 13	CJP 3
SADD	4	-RC 5	SADD 4	RLC 4	ALUCC 4	PUSH 4
INTS	5	+ 6		RRC 5	SRCC 5	JSRP 5
DMAD	8	+ C 7	DMAD 8	ROL 6	MACKS 16	CJV 6
DMR	9	(EXOR) A 8	DMW 9	ROR 7	LAMS 17	JRP 7
CMCR	A	(OR) A	CMCW A	XS 18	XC 8	RFCT 8
CXOL	B	B (AND) C	CCTRL B	QS 19	QC 9	RPCT 9
SHFL	C	PASS E	CFA C	DMASS IA	DMASC A	CRTN A
TMEM	D		CNFA D	HBRQS IB	HBRQC B	CJPP B
CONØ	E		MCTRL E	BUSMS IC	BUSMC C	LDCT C
CON I	F		LMASK F	ATNS ID	ATNC D	LOOP D
				XACKS IE	XACKC E	CONT E
				XREQS IF	XREQC F	TWB F

Model 3500-25. Microinstruction Set and 48-Bit Word Format



Simplified Block Diagram of Model 3500-25 MUPC

SPECIFICATIONS
Model 3500-25
CAMAC/MULTIBUS™ MICROPROMGRAMMABLE CONTROLLER
(MUPC)

HARDWARE

Microinstruction Rate:	6 MHz
ALU:	Schottky TTL combinatorial logic. (24 bits on 24 bits with 24-bit result.)
Program Sequencer:	Am2910
Program (microinstruction) Memory:	1024 by 48-bit words downloaded from System 3500 SBC bus.
Local (register) Memory:	1024 by 24-bit words directly interfaced to ALU.
Programmable LAM Mask:	8-bit binary mask independent of module programming. (For LeCroy 3500 System minicrate only.)
Interface to 3500-2 Memory	24-bit wide private interface. Read: 4.5 Mbytes/sec. Write: 6 Mbytes/sec. Read/Modify/Write: 1.2 Mwords/sec.
Vector Memory:	256 by 10-bit vector jump addresses for program flow control.
Auxilliary Memory:	Up to 64 K by 24-bit (3500-2) Up to 1 M by 24-bit (3500-2D)
Power Requirements:	3500-10: 4.9 A at + 5 V. 3500-11: 6.5 A at + 5 V. 3500-12: 3.2 A at + 5 V.

PACKAGE

3 MULTIBUS Boards
3500-10 Program Control Board
3500-11 Arithmetic, Memory and Bus Master Board
3500-12 CAMAC and Data Memory Interface Board

SOFTWARE

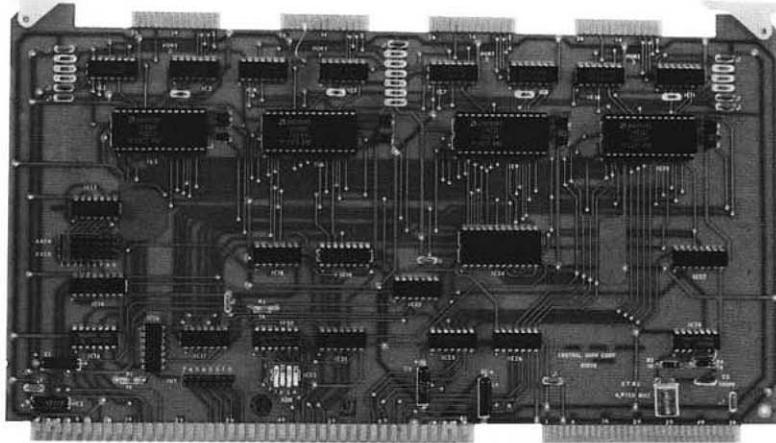
Microassembler (MU):	Symbolic microassembler that runs within 3500 under CP/M. Produces microinstruction object code, optional listing file and optional vector jump address file.
Debugging Tool (MUD):	Enables user to load, modify, and save microprograms. Single step or execute with up to 16 hardware breakpoints. Examine and modify internal states.
Disassembler (UM):	Translates hexadecimal ASCII object code into microassembly language.
FORTRAN Support Package:	Duplicates standard System 3500 CAMAC I/O routines.
	Provides routines for loading object code and vector memory.
	Provides communication and interrupt handling routines for parallel processing.

ORDERING INFORMATION

Model 3500-25 Micro-Programmable Controller (MUPC). Consists of 3 Multibus boards, Model 3910-25 MUPC Software which includes Micro-Assembler (MU), Micro-Assembler Debugger (MUD), Disassembler (UM), and FORTRAN Library consisting of CAMI and CAMO calls. Also included are two sets of interconnecting cables and a complete Hardware and Software manual.

Model 3500-35**Quad Port Interface to RS-232-C
Accessory for System 3500**

System 3500



Model 3500-35

Introduction

LeCroy's Model 3500-35 Quad Port Interface to RS-232-C is a plug-in board accessory for LeCroy's System 3500 Programmable Multichannel Analyzer and CAMAC Acquisition and Control System. It provides four RS-232-C interfaces for System 3500 in addition to the RS-232-C interface built into the standard System 3500. Multiple RS-232-C ports are necessary in configurations of System 3500 that require multiple simultaneous serial output connections to devices such as:

1. Model 3931A Printer/Plotter Accessory,
2. An external serial terminal for remote operation,
3. A direct serial link to a host computer for data transfer and/or control.
4. Connection to data sets or data terminals for data transfer by means of Modems.

Description

Model 3500-35 contains four 8251 USART's for parallel-to-serial conversion, and three interval timers to control the baud rate of each USART (two USARTS use one of the clocks and their baud rates are the same).

Baud rates and specifications for the data transmission are totally programmable by System 3500. Model 3500-35 uses 16 I/O ports, and is addressable on any 16-port boundary in System 3500's I/O arrangement. The full 16-bit I/O address bus can be used to determine the addressing of the board if desired.

Straps for each USART can enable interrupts at the end of character transmission or reception.

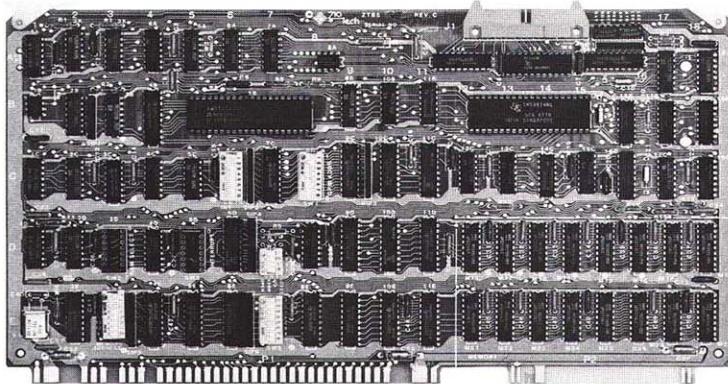
SPECIFICATIONS

Model 3500-35

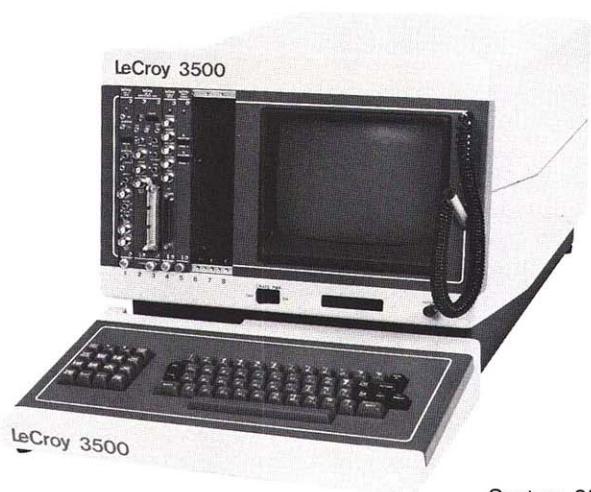
QUAD PORT INTERFACE TO RS-232-C ACCESSORY FOR SYSTEM 3500

Word Size:	8 bits.																										
Access Time:	500 nsec maximum.																										
Baud Rate-Programmable:	75, 150, 300, 600, 1200, 2400, 4800, 9600, and 19,200.																										
Interrupt Sources:	Any transmitter empty condition or receiver full condition can trigger an interrupt on any of the eight vectored interrupt lines of System 3500's computer bus. Straps for each USART determine whether receiver or transmitter interrupts can come from that chip.																										
Addressing:	<p>Model 3500-35 requires 16 I/O ports, and the base address for these ports can be on any 16 port boundary. Full 16-bit dip-switch I/O addressing is strap-selectable.</p> <p>The first eight ports on the board are divided between the USARTs. Each USART gets two consecutive ports, and their functions are as follows:</p> <table><thead><tr><th>ADDRESS</th><th>INPUT FUNCTION</th><th>OUTPUT FUNCTION</th></tr></thead><tbody><tr><td>0</td><td>Receiver Holding Reg.</td><td>Transmit Holding Reg.</td></tr><tr><td>1</td><td>Status Register</td><td>Command Register</td></tr></tbody></table> <p>The interval timer uses the next four ports in the following manner:</p> <table><thead><tr><th>ADDRESS</th><th>INPUT FUNCTION</th><th>OUTPUT FUNCTION</th></tr></thead><tbody><tr><td>0</td><td>Read Counter 0</td><td>Load Counter 0</td></tr><tr><td>1</td><td>Read Counter 1</td><td>Load Counter 1</td></tr><tr><td>2</td><td>Read Counter 2</td><td>Load Counter 2</td></tr><tr><td>3</td><td>No-Operation</td><td>Write Control Word</td></tr></tbody></table>			ADDRESS	INPUT FUNCTION	OUTPUT FUNCTION	0	Receiver Holding Reg.	Transmit Holding Reg.	1	Status Register	Command Register	ADDRESS	INPUT FUNCTION	OUTPUT FUNCTION	0	Read Counter 0	Load Counter 0	1	Read Counter 1	Load Counter 1	2	Read Counter 2	Load Counter 2	3	No-Operation	Write Control Word
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1	Read Counter 1	Load Counter 1																									
2	Read Counter 2	Load Counter 2																									
3	No-Operation	Write Control Word																									
RS-232-C Specifications:	The drivers and receivers used on the board are the 1488 and 1489 type. This provides a compatible interface for the following lines: TxD, RxD, DSR, DTR, and RTS.																										
Electrical Characteristics:	$V_{cc} + 5 \text{ V} \pm 5\%$ $I_{cc} = 0.85 \text{ A typ, } 1.0\text{A max.}$ $V_{dd} = + 12 \text{ V} \pm 5\%$ $I_{dd} = 0.05 \text{ A typ, } 0.1\text{A max.}$ $V_{bb} = - 12 \text{ V} \pm 5\%$ $I_{bb} = 0.05 \text{ A typ, } 0.1\text{A max.}$																										
Ordering Information:	<p>Model 3500-35 Quad Port Interface to RS-232-C Accessory. (Note: The System 3500 must include Model 3921 Dual-Drive Floppy Disc Accessory for operation with Model 3500-35.) Includes: one Model DC 3500-35 Data Cable, instruction manual, and Model 3910-14 Quad Serial Interface Software.</p> <p>Accessory: Model DC3500-35 Data Cable (15 feet).</p>																										

SPECIFICATIONS SUBJECT TO CHANGE

Model 3500-38**General Purpose Interface Bus (GPIB)
Accessory for System 3500**

Model 3500-38



System 3500

Introduction

LeCroy's Model 3500-38 General Purpose Interface Bus is a plug-in accessory for LeCroy's Model 3500 Programmable Multichannel Analyzer and CAMAC Acquisition and Control System which provides access from the System 3500 to over 300 different instruments and computer peripherals, using the GPIB (General Purpose Interface Bus: IEEE Standard 488).

The Model 3500-38 is a one-board, self-contained, intelligent controller for the GPIB (General Purpose Interface Bus), when installed in a System 3500 with the programmable option offered by the Model 3921 Dual Drive Floppy Disc Accessory.

High Level Interface Commands

The Model 3500-38 interprets a sequence of high level instructions placed in its memory by the System 3500 and performs all of the bus protocol required to communicate over the GPIB. Model 3500-38 is an

asynchronous, parallel I/O processor. This allows the program in the System 3500 to concentrate on system requirements, not on the bus. The messages shown in Table 1 map into the GPIB protocol and allow the user to completely exercise the bus without having to manipulate each bit separately.

Table 1

Receive Block of Data	Clear Lockout and Go Local
Send Block of Data	Go to Local
Request Service	Clear
Send Status Byte	Enable/Disable Parallel Poll
Trigger	Send Parallel Poll
Remote Enable	Pass Control
Go to Remote	Conduct Serial Poll
Local Lockout	

All messages to and from the GPIB are communicated through an eight Kilobyte Memory on the 3500-38. This memory acts as a slave module to both the 3500-38 processor and the System 3500's Central Processor and can be accessed by either the System 3500 or the 3500-38.

Standard Computer Peripheral and Instrument Interface

The Model 3500-38 GPIB provides the flexibility to satisfy many I/O requirements. It can replace many other special-purpose interface boards for substantial savings in initial cost, service, spares and program efficiency. A large and growing list of peripherals is available that attach via the GPIB: printers, plotters, cartridge tape units and 9-track formatters. In addition, the GPIB provides a parallel communication link to compatible host computers.

In electronic instrumentation there are many types of GPIB-compatible instruments ranging from inexpensive counters and DVMs to complete frequency synthesizers and systems.

With the 3500-38 there is very little loading of the System 3500, since all GPIB actions are handled in parallel by a microprocessor on the interface. This leaves the System 3500 free of I/O overhead.

Complete GPIB Controller, Talker, and Listener Capability

GPIB-compatible devices can usually be divided into four types: only able to talk; only able to listen; able to talk and listen; and able to talk, listen, and control. Certain restricted instrument systems can be configured without a controller, but to fully utilize peripherals and instruments, a GPIB controller such as the 3500-38 is needed. (Software on the 3910-11 diskette allows the 3500-38 to be configured only as a controller.)

As a controller, the 3500-38 can use all of the instructions in Table 1. When received by devices, the mes-

sages cause a predetermined action to occur. They can send (talk) or receive (listen) data in a device-dependent manner, or they can take some control action based on the message. The 3500-38 implements the full set of controller capabilities as defined by the IEEE Standard 488-1978. It may optionally be restricted from being a system controller.

The 3500-38 may also optionally be restricted to be only a talker and listener. This is useful if the board is being used to give the System 3500 a GPIB interface. In this mode, the board has all capabilities except PP1 and the controller functions.

The following table gives the IEEE 488-1978 subsets implemented by the 3500-38.

SH1 Source Handshake

AH1 Acceptor Handshake

TE2 Basic extended talker and serial poll

LE2 Basic extended listener

SR1 Service Request

RL1 Remote-Local with lockout

PP2 Parallel Poll w/o programmed configuration

DC1 Device Clear

DT1 Device Trigger

C1 System Controller

C2 Interface Clear and take charge

C3 Remote Enable

C4 Respond to SRQ

C5 All other controller functions

Software Support

The 3910-11 diskette contain all the software necessary to manipulate the GPIB from a Fortran program. Subroutines enable the user to initialize the 3500-38 as a controller, send data, receive data, and return the status of the GPIB.

SPECIFICATIONS

Model 3500-38

GENERAL PURPOSE INTERFACE BUS (GPIB)

ACCESSORY FOR SYSTEM 3500

GPIB Electrical:	Conforms to IEEE Standard 488-1978. Each of the 16 lines is driven, received, and terminated with Texas Instruments 7516/0,1,2 transceivers. This provides 500 mV input hysteresis, 0.4 volt output at 48 mA, bus divider voltage of 2.5 to 3.7 V, and open collector or three-state drivers.
GPIB Mechanical:	Conforms to IEEE Standard 488-1978. Note that this connector uses the metric threaded lock screw. The connector is similar to the 24-pin Microribbon (Amphenol or Cinch series 57).
Backplane:	P1 logically, electrically and physically compatible with the Multibus™ of System 3500. P2 used for test points and should not be connected to other boards.
Environment:	0° to 55°C temperature. (operating) – 20° to 75°C temperature. (non-operating) < 90% relative humidity, non-condensing.
Power Requirements:	+ 5 volts DC at 4.1 A maximum + 5 volts DC at 2.8 A typical
Data Rate:	240 K Bytes/sec.

ORDERING INFORMATION

Model 3500-38 GPIB Accessory for System 3500. (Note: The System 3500 must include Model 3921 Dual Drive Floppy Disc Accessory for operation with Model 3500-38).

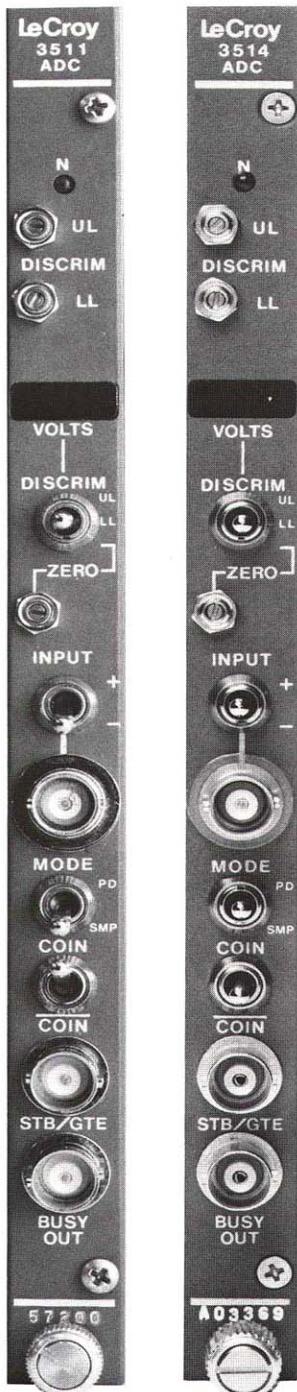
Includes:

1. Instruction manual.
2. Rear Panel Connector Kit and Jumper Cable from Model 3500-38 to System 3500 Rear Panel. Note: When ordered with System 3500, the Connector Kit is installed on the 3500 rear panel at the factory.
3. Model 3910-10 support software.

Accessory: Model DC3500-38 Standard GPIB, IEEE-488, Double-Ended Cable (15 feet).

TM Multibus is a trademark of Intel Corporation and conforms to IEEE Standard 796-1978.

SPECIFICATIONS SUBJECT TO CHANGE



CAMAC Models 3511 and 3514 High Performance Spectroscopy ADC's

- Model 3511 combines low dead time and 5 μ sec conversion time for 8K channels permitting 150 kHz throughput rate
- Model 3514 offers minimum spectroscopy dead time and 1 μ sec conversion time for 4K channels permitting 350 kHz throughput rate
- 250 to 8K (Model 3511) or 250 to 4K (Model 3514) programmable conversion gains
- Directly compatible with LeCroy Model 3500M Multichannel Analyzer for complete multiple-input pulse height analysis with built-in acquisition, display, data analysis, and I/O
- Memory transfer time of <1 μ sec/conversion with Model 3500M
- Peak-detect, strobed sampling and gated inputs with built-in self-strobe capability

INTRODUCTION

LeCroy's Models 3511 and 3514 are high-speed, high resolution, ADC's for gamma and x-ray spectroscopy applications. Model 3511 offers 250 to 8000 channel conversion gains with a conversion time of 5 μ sec for an 8000 channel conversion. Model 3515 offers 250 to 4000 channel conversion gains with a conversion time of just 1 μ sec for a 4000 channel conversion.

GENERAL DESCRIPTION

Models 3511 and 3514 operate in either peak-detect mode, with coincidence or anti-coincidence gating, or strobed sample mode for sampling DC or slowly varying AC signals. Built-in self strobing permits sampling the input signal from 100 nsec to 35 μ sec after triggering the lower level discriminator. Both bipolar and monopolar, positive or negative, DC-coupled inputs in the range of 0 to 8 V can be accepted with risetimes of 300 nsec to 20 μ sec.

Upper and lower discriminator and zero adjust are precisely set by 22-turn potentiometers with settings read on an LED display. An ADC prompt or delayed busy output can be provided to enable successive ADC's or for external timing or control.

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ZERO DEAD TIME MEASUREMENTS

With several 3511 or 3514 ADC's cascaded, dead time of the analysis system can be effectively eliminated. Model 3541 is a single-width CAMAC companion module to Models 3511 and 3514 and provides two channels of preset live/real time control and % dead time display for two ADC's. The preset time range is to 0.01 to 900,000 sec.

COMPATIBLE WITH MODEL 3500 MULTICHANNEL ANALYZER

To take full advantage of their fast conversion times, Models 3511 and 3514 are directly compatible with and fully supported by LeCroy's Model 3500M

Multichannel Analyzer System. Model 3500M includes firmware for programming acquisition parameters and permits direct memory access (DMA) data transfer to 8192 channels of histogramming data memory in less than 1 μ sec/conversion. In the basic 3500M, up to eight 3511 and/or 3514 modules can be directly interfaced for inputting data to Model 3500M. With sufficient data memory in Model 3500M, each ADC can be used with maximum conversion gain for maximum resolution.

Models 3511 and 3514 are high-density, single-width CAMAC modules measuring only 0.7 inches by 9 inches, one-half the size of a single-width NIM module, and one-fourth to one-sixth of most NIM ADC's.

SPECIFICATIONS CAMAC Models 3511 and 3514 HIGH PERFORMANCE SPECTROSCOPY ADC's

GENERAL

Type:

Model 3511 is a 13-bit (8000 channel) and Model 3514 is a 12-bit modified successive approximation type analog-to-digital converter.

Packaging:

Single-width CAMAC module.

Operating Modes:

Models 3511 and 3514 provide two input conversion operating modes: Peak-Detect and Sample. In the Peak-Detect (PD) mode, conversion is self-triggered upon detection of a signal peak within discriminator settings. In the Sample (SMP) mode, conversion is initiated by a strobe pulse for a signal within discriminator settings. Built-in self-strobing capability permits sampling the input 100 nsec to 35 μ sec after the lower level discriminator is triggered.

CONVERSION

Conversion Gain:

Model 3511: 250, 500, 1K, 2K, 4K, or 8K channels full scale; Model 3514: 250, 500, 1K, 2K or 4K channels full scale. Programmable through CAMAC Dataway.

Conversion Time:

Model 3511: Fixed at 5 μ sec for 8K channels. Model 3514: Fixed at 1 μ sec for 4K channels.

Total Conversion Dead Time:

ADC conversion time plus 0.3 to 20 μ sec risetime, plus 0.5 to 2.0 μ sec risetime compensation (selectable by internal switch in 0.5 μ sec steps), plus 100-400 nsec storage offset processing time, plus 400 nsec buffer memory transfer time.

Conversion Triggering:

Conversion is initiated by peak detection or a strobe pulse for an input signal within discriminator setting.

INPUT

Peak-Detect Mode:

Shaped pulses, positive or negative (switch-selectable) bipolar or monopolar, 50 mV to 8 V input range. Risetime range—300 nsec to 20 μ sec in five internal switch-selected ranges. Each selection optimizes peak detection response for that range of risetimes. (See Risetime Select Switch.)

Sample Mode:

Positive or negative (switch-selectable) bipolar or monopolar, 0 to 8 V input range. Minimum duration—500 nsec.

Coupling:

DC input.

Input Impedance:

1 k Ω for positive input.
600 Ω negative input.

Str/Gate Input:

The Strobe/Gate Input serves two functions. In the Peak-Detect mode, a gate pulse enables or inhibits conversion in conjunction with the Coincidence/Anti-Coincidence switch. In the Sample mode, a strobe pulse initiates conversion of a DC signal or slowly varying AC signal. The input is both TTL and NIM compatible.

A unique feature of Models 3511 and 3514 is a self-strobe capability achieved by using the delayed busy signal output initiated by the lower level discriminator firing, as the input to the Strobe/Gate Input. The Busy delay is adjustable from 100 nsec to 35 μ sec for selecting the desired time after the signal exceeds the lower level discriminator for sampling.

OUTPUT

Busy Output:

Signals that the 3511 or 3514 is performing a conversion. The Busy Output permits cascading several ADC's to reduce overall system dead time. A Busy Output connects to the Strobe/Gate Input of the next ADC to enable it only when all of the preceding ADC's are performing a conversion. A delay (internally adjustable from 100 nsec to 35 μ sec) determines the time after peak detection, or after lower level discriminator firing when the Busy Output is present, such that only one ADC will convert any given pulse. An internal jumper permits selecting either peak detect (delayed) or lower level discriminator (prompt) initiation of the Busy signal. A prompt Busy Output is available on the rear panel to drive a LeCroy Model 3541 Deadtimer module which monitors dead time and provides timing control of the experiment. An internal jumper permits bringing the prompt Busy rather than a delayed Busy Output to the front-panel Busy connector for external timing and control requirements. The front-panel Busy Output pulse is positive TTL logic.

Zero Adjust:

Provides for ± 0.5 V analog offset in input signal such that a zero energy (volt) input can correspond to channel zero. Set by a 22-turn potentiometer with the setting read on a LED Display for reproducibility.

Storage Offset:

A converted signal for histogramming can be assigned to memory segments of 8192, (model 3511 only), 4096, 2048, 1024, 512, or 256, depending upon the conversion gain selected and memory available. With 8K of memory and conversion gain of 4K, a converted signal can be assigned to either memory half. One ADC is programmed for a storage offset of 4K channels to assign its conversions to the 4K to 8K memory segment. Up to 32 ADC's can be accommodated by 8K of memory if conversion gains on each are 250. Storage offsets of up to 65,280 channels can be provided. Storage offset programming is through the CAMAC dataway.

LINEARITY AND STABILITY

Integral Non-Linearity:

Model 3511: Better than $\pm 0.0375\%$ over 99% of 50 mV to 8 V input range for shaded pulses. Typically better than $\pm 0.0125\%$ over upper 99.9% of 0 to 8 V input range for strobed DC input.

Model 3514: Better than $\pm 0.05\%$ over upper 99% of 50 mV to 8 V input range for shaped pulses. Typically better than $\pm 0.0125\%$ over upper 99.9% of 0 to 8 V range for strobed DC input.

Differential Non-Linearity:

Model 3511: Better than $\pm 1\%$ over upper 99% of 50 mV to 8 V input range for shaped pulses.

Model 3514: Better than $\pm 2.5\%$ over upper 99% of 50 mV to 8 V input range for shaped pulses.

Temperature Stability:

Less than 0.01%/ $^{\circ}$ C baseline shift over 15 $^{\circ}$ C to 55 $^{\circ}$ C. Less than 0.01%/ $^{\circ}$ C conversion gain shift over 15 $^{\circ}$ C to 55 $^{\circ}$ C.

DISCRIMINATION

Upper and Lower Level Discriminators:

Separate controls continuously adjustable from 0 to greater than 8 V monitored by 3-digit display accurate to ± 10 mV. In the Peak-Detect mode, the discriminators' range is from 50 mV to 8 V.

CAMAC COMMANDS

All conversion data transfers and module control instructions are carried through the CAMAC dataway. When Model 3511 or 3514 are used in a Model 3500M Multichannel Analyzer System, Model 3500M firmware automatically sets CAMAC functions for DMA data transfer to memory. CAMAC functions for both the 3511 and 3514 are:

F(0):

Read data.

F(2):

Reads and Clears Data, Clears LAM, and generates Q response, if LAM is present.

F(8):

Test LAM, generates Q response.

F(10):

Clear LAM.

F(16):

Writes into control register conversion gain storage offset.

F(24):

Disable.

F(26):

Enable.

Initialize (Z), Clear (C), Inhibit (I) also implemented.

FRONT-PANEL CONTROLS

PD/SMP Switch:	Selects either self-triggering Peak-Detect mode or strobed Sample of a DC or slowly varying AC input.
Positive/Negative Input Polarity Switch:	Set for the polarity of unipolar input signal, or polarity of leading phase of bipolar input signals.
Coincidence/Anti-Coincidence Switch:	Two-function switch dependent on operating mode selection. In Peak-Detect mode, the gate input can be used for either Coincidence or Anti-Coincidence operation, depending on the switch position. In Sample mode, the Coincidence position selects the front edge of a positive TTL or standard NIM logic pulse for initiating conversion. Anti-Coincidence position selects the back edge of triggering. When peak detecting with no gating requirement, Anti-Coincidence position is used.
Discriminator/Zero Switch:	Select either Upper (UL) or Lower (LL) level discriminator or zero adjust setting for readout in volts on the LED display.
Discriminator Adjustments:	Screwdriver adjustable 22-turn potentiometers set UL and LL discriminator settings. Range is from 0 to greater than 8.00 V read on the LED display. In the Peak-Detect mode, the usable discriminator range is 50 mV to 8 V (0.05 to 8.00 on the LED display).
Zero Adjust:	Screwdriver adjustable 22-turn potentiometer reproducibly sets input offset such that zero voltage input corresponds to channel zero. Offset range is ± 0.5 V. Zero setting is displayed on LED indicators which read from 0.00 to 1.00 V (where 0.00 V reads as -0.5 V offset; 1.00 V reads as $+0.5$ V offset; and 0.50 V reads as 0.00 V offset).
Risetime Select (Side-Panel) Switch:	In the Peak-Detect mode, Models 3511 and Model 3514 accept shaped input pulses with risetimes in the range of 300 nsec to 20 μ sec. Five switch-selectable subranges are provided to optimize the input circuit's response to the appropriate input risetime.

Position	Risetime Range
1	300 nsec to 400 nsec
2	350 nsec to 1 μ sec
3	1 μ sec to 4 μ sec
4	3 μ sec to 10 μ sec
5	7 μ sec to 20 μ sec

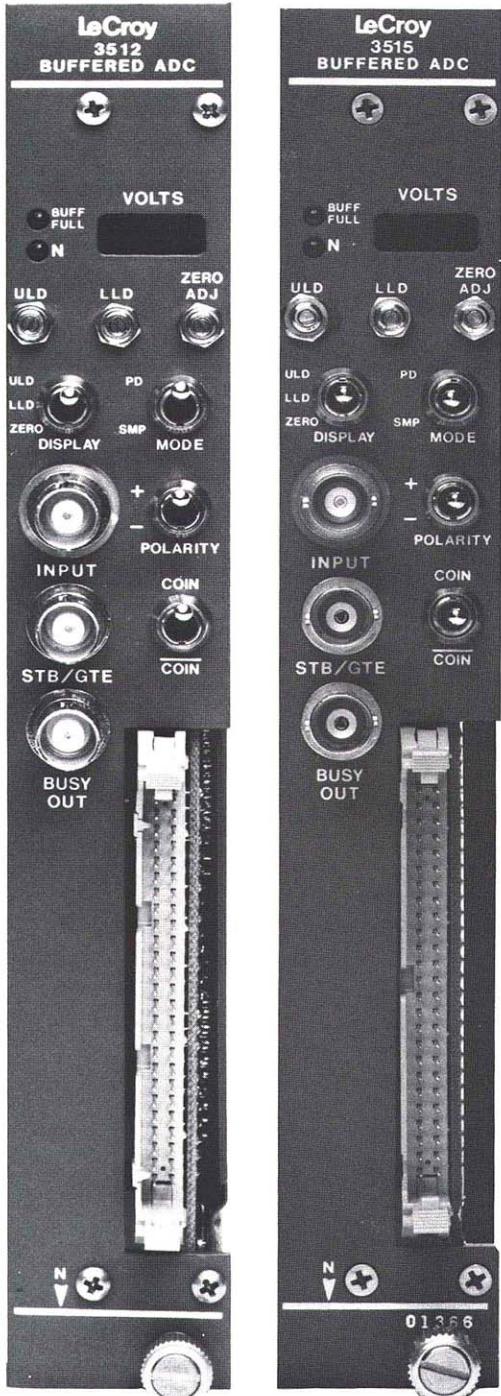
For risetimes longer than 20 μ sec, the input should be strobed either by an external strobe to the Str/Gate input connector, or the input should be strobed using the self-strobing capability of Model 3511 and 3514 (refer to Str/Gate Input).

POWER REQUIREMENTS

For both Models 3511 and 3514:

- 1.2 A at + 6 V
- 150 mA at + 24 V
- 150 mA at - 24 V

SPECIFICATIONS SUBJECT TO CHANGE



CAMAC Models 3512 and 3515 High Performance Buffered Spectroscopy ADC's

For High-Throughput CAMAC Acquisition And Multi-Parameter Applications

- Low dead time and high-speed ADC conversion permits fast 300 kHz rate (Model 3515) or 150 kHz (Model 3512) throughput rate
- 250 to 8K (Model 3512) or 250 to 4K (Model 3515) programmable conversion gains.
- Peak detect, strobed sampling, and gated inputs with built-in self-strobe capability.
- 1024 words of buffer memory accept high burst rate (up to 150 KHz for Model 3512 and up to 350 kHz for Model 3515)
- For time-correlated multi-parameter applications, provides list mode data with tag words for each conversion and accepts externally generated delimiting words through front-panel connectors.
- Front-panel bus transfers data to external CAMAC Model 3588 Histogramming Memory module for Time-Resolved Spectroscopy in up to 64 memory segments, and for compact CAMAC based PHA capability.

General Description

Models 3512 and 3515 operate in either peak-detect mode, with coincidence or anti-coincidence gating, or strobed sample mode for sampling DC or slowly varying AC signals. Built-in self strobing permits sampling the input signal from 100 nsec to 35 μ sec after triggering the lower level discriminator. Both bipolar and monopolar, positive or negative DC-coupled inputs in the range of 0 V to 8 V can be accepted with risetimes of 300 nsec to 20 μ sec.

Upper and lower discriminator and zero adjust are precisely set by multturn potentiometers with settings read on an LED display. An ADC prompt or delayed busy output can be provided to enable successive ADC's or for external timing or control.

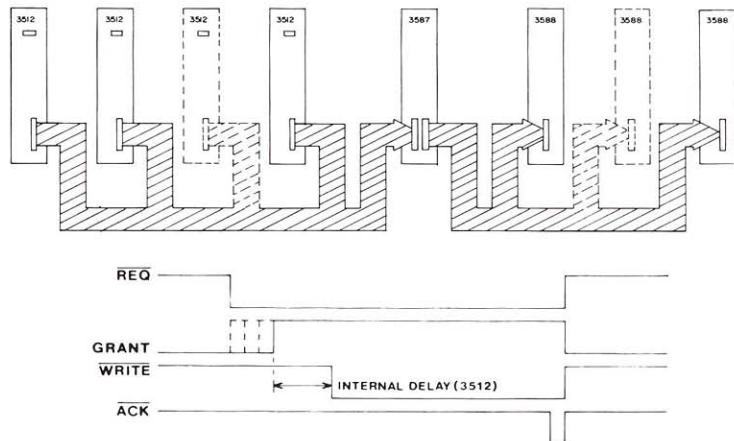
up to 16,384 channels of histogramming memory, a count capacity of 16,777,215 counts (24 bits)/channel, and a memory cycle time of 1.25 μ sec/ conversion (800 kHz). The memory is divisible into segments as small as 256 channels (8 bits) to permit multiple ADC's to write into a single memory module.

Time-Resolved Spectroscopy

A single ADC can be interfaced to multiple Model 3588 Memory modules. This configuration is appropriate in time-resolved spectroscopy applications in which multiple consecutive spectra are acquired at different time periods. In this application, the Model 3587 Data Router is used to provide the switching and offset bits for acquisition in successive memory locations. A single 3587 is capable of timing and offsetting data from multiple ADC's to multiple 3588s. Models 3512 and 3515 can share the external data bus to the 3587 and 3588.

Direct CAMAC Compatibility

Model 3512's and 3515's CAMAC format makes them directly compatible with any CAMAC system. No additional hardware is required for bidirectional communication with the associated computer. As a result, Model 3512's and 3515's acquisition parameters such as conversion gain, storage offset, and preset



Model 3512s or 3515s configured with Model 3588 Histogramming Memory and a Model 3587 Data Router.

controls can be changed under program control during an experiment to fully automate data acquisition.

Models 3512 and 3515 are high-density, double-width CAMAC modules measuring only 1.4 inches by 9 inches, the size of a single-width NIM module, and one-half to one-third the size of most NIM ADC's. Up to eleven ADC's can be installed in, powered by, and interfaced through a single standard CAMAC crate.

SPECIFICATIONS CAMAC Models 3512 and 3515 HIGH PERFORMANCE BUFFERED SPECTROSCOPY ADC's

GENERAL

Type:

Model 3512 is a 13-bit (8000 channel) and Model 3515 is a 12-bit (4000 channel) modified successive approximation type analog-to-digital converter.

Memory Type:

1024 words \times 16 bits of static RAM configured as FIFO. Memory cycle time is 400 nsec per 16-bit write operation.

Packaging:

Double-width CAMAC module. Up to 11 Model 3512s and/or 3515s can be installed in, powered by, and interfaced through a single CAMAC crate.

Operating Modes:

Models 3512 and 3515 provide two input conversion operating modes: Peak-Detect and Sample. In the Peak-Detect (PD) mode, conversion is self-triggered upon detection of a signal peak within discriminator settings. In the Sample (SMP) mode, conversion is initiated by a strobe pulse for a signal within discriminator settings. Built-in self-strobing capability permits sampling the input 100 nsec to 35 μ sec after the lower level discriminator is triggered.

CONVERSION

Conversion Gain:

Model 3512: 250, 500, 1K, 2K, 4K, or 8K channels full scale; Model 3515: 250, 500, 1K, 2K or 4K channels full scale. Programmable through CAMAC Dataway.

Conversion Time:

Model 3512: 5 μ sec for 8K channels. Model 3515: 1.2 μ sec for 4K channels.

Total Conversion Dead time:

ADC conversion time plus 0.3 to 20 μ sec risetime, plus 0.5 to 2.0 μ sec risetime compensation (selectable by internal switch in 0.5 μ sec steps), plus 100-400 nsec storage offset processing time, plus 400 nsec buffer memory transfer time.

Conversion Triggering:

Conversion is initiated by peak detection or a strobe pulse for an input signal within discriminator setting.

INPUT

Peak-Detect Mode:	Shaped pulses, positive or negative (switch-selectable) bipolar or monopolar, 50 mV to 8 V input range. Risetime range—300 nsec to 20 μ sec in five internal switch-selected ranges. Each selection optimizes peak detection response for that range of risetimes. (See Risetime Select Switch.)
Sample Mode:	Positive or negative (switch-selectable) bipolar or monopolar, 0 to 8-V input range. Minimum duration—500 nsec.
Coupling:	DC input.
Input Impedance:	1 k Ω for positive input. 600 Ω negative input.
Str/Gate Input:	The Strobe/Gate Input serves two functions. In the Peak-Detect mode, a gate pulse enables or inhibits conversion in conjunction with the Coincidence/Anti-Coincidence switch. In the Sample mode, a strobe pulse initiates conversion of a DC signal or slowly varying AC signal. The input is both TTL and NIM compatible. A unique feature is a self-strobe capability achieved by using the delayed busy signal output initiated by the lower level discriminator firing as the input to the Strobe/Gate Input. The Busy delay is adjustable from 100 nsec to 35 μ sec for selecting the desired time after the signal exceeds the lower level discriminator for sampling.

OUTPUT

Busy Output:	Indicates that a conversion is in process. The Busy Output permits cascading several ADC's to reduce overall system dead time. A Busy Output connects to the Strobe/Gate Input of the next ADC to enable it only when all of the preceding ADC's are performing a conversion. A delay (internally adjustable from 100 nsec to 35 μ sec) determines the time after peak detection, or after lower level discriminator firing when the Busy Output is present, such that only one ADC will convert any given pulse. An internal jumper permits selecting either peak (delayed) detect or lower level discriminator (prompt) initiation of the Busy signal. A prompt Busy Output is available on the rear panel to drive a LeCroy Model 3541 Deadtimer module which monitors dead time and provides timing control of the experiment. An internal jumper permits bringing the prompt Busy rather than a delayed Busy Output to the front-panel Busy connector for external timing and control requirements. The front-panel Busy Output pulse is positive TTL logic.
External Read/Write:	A 50-pin front panel connector is provided to: (1) Read external delimiting words to enter into buffer memory for time-correlating data blocks or for defining experiment parameter changes such as angle, time, or position; (2) Write data to external electronics such as model 3588 Histogramming Memory instead of writing into buffer memory. Handshake control lines are provided for reading or writing.
Zero Adjust:	Provides for ± 0.5 V analog offset in input signal such that a zero energy (volt) input can correspond to channel zero. Set by a 22-turn potentiometer with the setting read on a LED Display for reproducibility.
Storage Offset:	Storage offset is used only when the data is to be read as histogram data (i.e., the conversion is the address to a memory location, and the data is an “add one” to that location). When the conversion address is read as List mode data, the Storage Offset is not needed and can be masked by a 3-bit tag word which increments for each conversion. Mode selection is software programmable. A converted signal for histogramming can be assigned to memory segments of 8192, (Model 3512 only) 4096, 2048, 1024, 512, or 256, depending upon the conversion gain selected and memory available. With 8K of memory and conversion gain of 4K, a converted signal can be assigned to either memory half. One ADC is programmed for a storage offset of 4K channels to assign its conversions to the 4K to 8K memory segment. Up to 32 ADC's can be accommodated by 8K of memory if conversion gains on each are 250. Storage offsets of up to 65,280 channels can be provided. Storage offset programming is through the CAMAC dataway.

LINEARITY AND STABILITY

Integral Non-Linearity:	Better than $\pm 0.0375\%$ for 3512 or $\pm 0.05\%$ for 3515 over 99% of 50 mV to 8 V input range for shaded pulses. Typically better than $\pm 0.0125\%$ over upper 99.9% of 0 to 8 V input range for strobed DC input.
Differential Non-Linearity:	Better than $\pm 1\%$ for 3512 or $\pm 1.5\%$ for 3515 over upper 99% of 50 mV to 8 V input range for shaped pulses.
Temperature Stability:	Less than 0.01%/ $^{\circ}$ C baseline shift over 15 $^{\circ}$ C to 55 $^{\circ}$ C. Less than 0.01%/ $^{\circ}$ C conversion gain shift over 15 $^{\circ}$ C to 55 $^{\circ}$ C.

Zero Dead Time Measurements

With several 3512 or 3515 ADC's cascaded, dead time of the analysis system can be effectively eliminated. Model 3541 is a single-width CAMAC companion module to Models 3512 and 3515 and provides two channels of preset live/real time control and % dead time display for two ADC's. The preset time range is to 0.01 to 900,000 sec.

High Burst Rate Capability

The buffered memory in Model 3512 and 3515 contains 1024×16 -bit words of static RAM configured as FIFO. In CAMAC acquisition systems, the high throughput capability of Model 3512 or 3515 may be limited by the data transfer (CAMAC read) rate of the computer controlling the CAMAC system. Model 3515 performs a 12-bit conversion and transfer data to buffer memory in just $3.0 \mu\text{sec}$, giving it a throughput rate of over 300 kHz. Typical programmed data transfer times in CAMAC systems typically limit the Model 3512's throughput rate, but use of the buffer memory allows high burst rates of up to 1024 events to be accepted without increased dead time.

Multi-Parameter Applications

In multi-parameter spectroscopy applications, coincident time correlation must be maintained between all ADC input channels. This requires external gating to enable all ADC's simultaneously. Models 3512 and 3515 include coincident or anti-coincident external gating capability for this purpose. For each multi-parameter event, data from all ADC's must be identified with the same code so that during later reconstruction and correlation of inputs, time coinci-

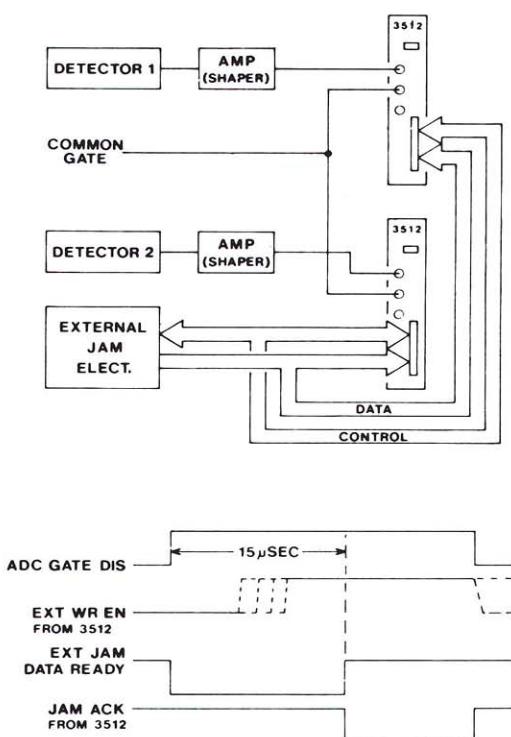
dent verification is possible. Each conversion in a Model 3512 or 3515 produces a 16-bit word. Up to 13 bits (8000 channels in an 3512) represent the digitally converted signal amplitude. Three bits are used to consecutively code or tag each conversion. In applications of multiple ADC's, a coincidence gate input can simultaneously enable all ADC's and coincident conversions will have the same 3-bit tag in all ADC's. In the absence of an input satisfying discriminator settings, and when enabled by a gate signal, the ADC will write a zero address into memory to maintain the time correlation of subsequent conversions with those of other ADC's.

Models 3512 and 3515 include a 50-pin front-panel connector to permit writing a delimiting word from external electronics between each conversion or between any selected numbers of conversions. The delimiting word can be "daisy-chained" to all ADC's in the multi-parameter experiment to provide a common time-correlated word for each coincident conversion or block of conversions. During later analysis of data, total verification of time correlation for all inputs is, therefore, possible and any non-coincident conversions or blocks of conversions can be rejected.

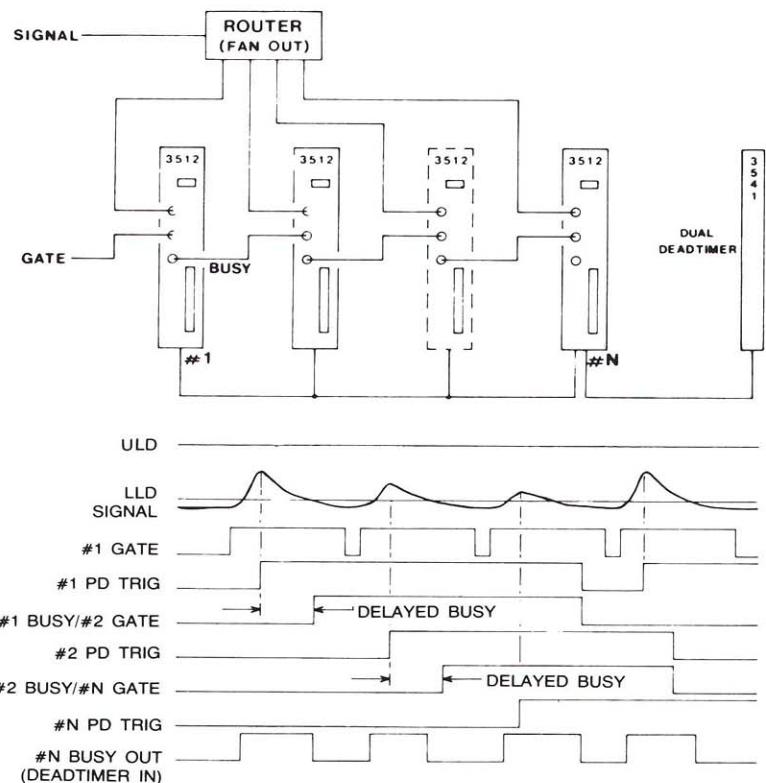
The external delimiting word also can be used to define some experimental parameter change such as angle, time, or position information related to preceding or succeeding events.

Available With External Histogramming Memory Accessory

Models 3512 and 3515 are available with a dedicated CAMAC memory module (Model 3588) that provides



Use of 3512s or 3515s in an multi-parameter time correlated.



Model 3512s or 3515s cascaded for minimum dead time.

DISCRIMINATION

Upper and Lower Level Discriminators:

CAMAC COMMANDS

F(0):

F(2):

F(8):

F(10):

F(16):

F(24):

F(26):

Separate controls continuously adjustable from 0 to greater than 8 V monitored by 3-digit display accurate to ± 10 mV. In the Peak-Detect mode, the discriminators' range is from 50 mV to 8 V.

All conversion data transfers and module control instructions are carried through the CAMAC dataway.

Operational CAMAC Function Codes for both the Model 3512 and 3515 are listed below: These codes are valid for any subaddress and only with a valid station number (N), with the exception of Z, C, and I. Subaddresses are not decoded.

Read data. Non-destructive read increments memory read pointer after read.

Reads data and decrements buffer length counter, generates Q response, if data is present, clears LAM when buffer is empty. This is a destructive read.

Test LAM, generates Q response if LAM is present. Can be used to test state of LAM flip-flop even if LAM is disabled, (F(24)).

Clear LAM and clear Buffer.

Writes into control register conversion gain, storage offset, mode select, and acquisition enable/disable.

Disable the LAM.

Enable the LAM.

Initialize (Z), Clear (C), Inhibit (I) also implemented.

FRONT-PANEL CONTROLS

PD/SMP Switch:

Selects either self-triggering Peak-Detect mode or strobed Sample of a DC or slowly varying AC input.

Positive/Negative Input Polarity Switch:

Set for the polarity of unipolar input signal, or polarity of leading phase of bipolar input signals.

Coincidence/Anti-Coincidence Switch:

Two-function switch dependent on operating mode selection. In Peak-Detect mode, the gate input can be used for either Coincidence or Anti-Coincidence operation, depending on the switch position. In Sample mode, the Coincidence position selects the front edge of a positive TTL or standard NIM logic pulse for initiating conversion. Anti-Coincidence position selects the back edge of triggering. When peak detecting with no gating requirement, Anti-Coincidence position is used.

Discriminator/Zero Switch:

Select either Upper (UL) or Lower (LL) level discriminator or zero adjust setting for readout in volts on the LED display.

Discriminator Adjustments:

Screwdriver adjustable 22-turn potentiometer set UL and LL discriminator settings. Range is from 0 to greater than 8.00 V read on the LED display. In the Peak-Detect mode, the usable discriminator range is 50 mV to 8 V (0.05 to 8.00 on the LED display).

Zero Adjust:

Screwdriver adjustable 22-turn potentiometer reproducibly sets input offset such that zero voltage input corresponds to channel zero. Offset range is ± 0.5 V. Zero setting is displayed on LED indicators which read from 0.00 to 1.00 V (where 0.00 V reads as -0.5 V offset; 1.00 V reads as $+0.5$ V offset; and 0.50 V reads as 0.00 V offset).

Risetime Select (Side-Panel) Switch:

In the Peak Detect mode, shaped input pulses are accepted with risetimes in the range of 300 nsec to 20 μ sec. Five switch-selectable subranges are provided to optimize the input circuit's response to the appropriate input risetime.

Position	Risetime Range
1	300 nsec to 400 nsec
2	350 nsec to 1 μ sec
3	1 μ sec to 4 μ sec
4	3 μ sec to 10 μ sec
5	7 μ sec to 20 μ sec

For risetimes longer than 20 μ sec, the input should be strobed either by an external strobe to the Str/Gate input connector, or the input should be strobed using the self-strobing capability (refer to Str/Gate Input).

POWER REQUIREMENTS

For both Models 3512 and 3515:

2.3 A at + 6 V

180 mA at + 24 V

160 mA at - 24 V



CAMAC Model 3521A Multichannel Scaling Module

- 100 MHz double-buffered scaling input
- 1 μ sec/channel dwell time
- <5 nsec interchannel dead time. Count capacity is up to 24 bits – 1 (16,777,215) counts per dwell period
- Directly compatible with LeCroy's System 3500M Multichannel Analyzer for multiple input MCS acquisition, display, analysis and I/O
- CAMAC-compatible for operation with LeCroy's CAMAC Models 8201A or 8206A Memory Modules, providing 16K or 64K \times 16-bit words of buffer storage
- Provides high count rate performance required in fast single ion or photon counting applications
- Ideal for event counting radiochromatography applications

Introduction

LeCroy's Model 3521A Multichannel Scaling Module provides 100 MHz input rate capability with 1 μ sec dwell time per channel, negligible interchannel dead time. 24-bit scaling (over 16 million counts per dwell period) bi-directional addressing, and external synchronization control. It is the ideal instrument for applications having high input rate and fast rate change conditions. Examples include ion counting measurements with mass spectrometers and laser scattering and luminescence decay-time measurements having fast, single-photon counting requirements. Model 3521A is also applicable in counting and high resolution histogramming of the pulse outputs of gas, liquid, paper, and thin-layer radiochromatograph detectors.

Compatibility

Model 3521A is a single-width CAMAC module directly compatible with LeCroy's System 3500M Multichannel Analyzer or with any CAMAC system. System 3500M is a complete stand-alone acquisition and analysis system providing dedicated acquisition, direct memory access data transfer and storage, display, analysis, archiving, and hard copy I/O capability for Model 3521A.

Up to 8 Model 3521A modules can be operated concurrently in System 3500M. With sufficient data memory in System 3500M, each 3521A can scale into 65,535 channels for optimum time resolution. In CAMAC systems Model 3521A can be operated with LeCroy's Models 8201A or 8206A Memory Modules which provide 16,384 or 65,535 sixteen-bit words of 1 μ sec cycle time buffer memory for fast acquisition without interchannel dead time associated with CAMAC read/write cycles.

Description

Model 3521A offers both single and continuous sweep modes with Ramp-Up/Ramp-Down sweep capability or Ramp-Up and return to zero. Model 3521A counts input logic pulses (either NIM or TTL levels) from a single-channel analyzer, discriminator, or other logic pulse generator.

Synchronization between the Model 3521A and external equipment may occur in either direction; i.e., the Model 3521A may be used to generate synchronization signals or it may be synchronized to an externally-generated signal. In single sweep mode an external trigger initiates each sweep for synchronization. Channel advance can be controlled by System 3500M with dwell time from 1 μ sec to 4296 seconds or externally controlled at any time increment down to 1 μ sec. The channel address can be input or output through a front-panel connector to synchronize the sweep with the experiment or to initiate sweeps at any channel location for multiplexing many detector inputs.

Internal counters and registers allow programming the number of channels per scan, the number of scans per run, address offset for direct memory access (DMA) storage in System 3500's data memory, and a choice of Ramp-Up and return to start or Ramp-Down address scanning.

CAMAC Model 8201A Memory Module



SPECIFICATIONS

CAMAC Model 3521A

MULTICHANNEL SCALING MODULE

Package:	Single-width CAMAC* module
Count Rate Range:	0 to 100 MHz.
Dead Time Between Channels:	<5 nsec.
Maximum Count Per Dwell Interval:	16,777,215 counts into System 3500 Data memory. 65,535 counts per dwell interval into Models 8201A or 8206A Memories.
Dwell Time Per Channel:	$\geq 1 \mu\text{sec}$. 1 μsec minimum. Maximum programmable dwell time can be 4296 seconds in System 3500 or dwell time can be externally controlled in any increment to 1 μsec minimum.
Inputs:	BNC connectors—NIM or TTL levels— 50Ω input impedance.
(a) SIGNAL:	Count on leading edge of positive-going TTL pulse or negative-going NIM pulse.
(b) INHIBIT:	Positive logic—gates off count pulses to scaler.
(c) EXT ADV:	Positive logic—advance occurs on leading edge. 100 nsec minimum pulse width.
(d) EXT EN:	Positive logic—enables external advance input, otherwise advance is controlled by clock signal on the P2 bus of the CAMAC dataway.
(e) TRIG:	Positive logic—starts each scan in the triggered sweep mode and initiates scanning in the continuous scan mode. 150 nsec minimum pulse width.
J3 Special Input:	37-pin D-type front-panel connector allows preloading an address into the 16-bit address counter or reading the current address on a bi-directional bus. 16 address lines 2^0 - 2^{15} . Address load control line. Read control line. External signals are TTL level negative logic. (An address load strobe overrides a read strobe.)
J2 Lines: (on rear panel)	List Memory Data Port; 40-pin connector for the LeCroy Model 8201 Memory module.
CAMAC Control:	<p>F(0) Reads scaler data—clears LAM.</p> <p>F(2) Reads channel address (16-bit) until leading edge of S1 after which scaler count appears on read lines—clears LAM.</p> <p>F(16)•A(0) Loads address offset register (16 bits).</p> <p>F(16)•A(1) Loads sweep counter with number of desired sweeps.</p> <p>F(16)•A(2) Loads number of channels register and mode control register.</p> <p>F(24) Disable LAM.</p> <p>F(26) Enable LAM.</p> <p>C,Z,F(9) Initialize.</p>
Description of Above Registers:	<p>A. Number of Channels Register—determines number of channels per scan in multiples of 2^8 channels up to 2^{16}—1 channels. Channel 0 is used as a Scan Counter.</p> <p>B. Address Offset Register—allows assignments of address locations for the number of selected channels to any segment of the 2^{16} address field.</p> <p>C. Mode Control Register—3 bits. Bit 1 selects either Ramp-Up return-to-start scan or Ramp-Up Ramp-Down scan. Bit 2 selects either triggered scanning or continuous scanning. Bit 3 selects automatic stop after a preprogrammed number of scans (determined by number loaded into sweep register by F(16)•A(1) or manual termination of scanning).</p>
Power Requirements:	1.2 A at + 6 V 550 mA at - 6 V

*Conforms to CAMAC standard for nuclear instrumentation modules (ESONE Committee Report EUR 4100C or IEEE Report No. 583).

SPECIFICATIONS SUBJECT TO CHANGE

TECHNICAL DATA

LeCroy



CAMAC Model 3541 Dual Deadtimer

- Provides 2 channels of % deadtime measurement and display.
- Compatible with Models 3511 and 3512 Spectroscopy ADC's.
- Provides 2 independent channels of preset time control.
- Offers both live and real time control.
- Preset live/real time range from 1 to 900,000 milliseconds or seconds.
- Directly compatible with and software-supported by LeCroy's System 3500M Multichannel Analyzer.
- % deadtime from both channels can be read through CAMAC.

Introduction

Model 3541 Dual Deadtimer contains two independent channels of live/real time. It is directly compatible with the LeCroy Models 3511 and 3512 Spectroscopy Analog-to-Digital Converter Modules to provide preset live/real time control with % deadtime display of two separate ADC's.

Two preset time ranges are provided: from 1 to 900,000 milliseconds or from 1 to 900,000 seconds. Selections in each range are from 1 to 9 times powers of ten from 10^0 to 10^5 . An internal jumper selects the desired range.

Description

Both channels of Model 3541 are programmable through the CAMAC dataway. Up to twenty 3511 or 3512 ADC's can be controlled by a single channel of the 3541 timer. Timing may be enabled either through the 3541 or through the modules being timed. A front-panel 2-digit LED readout of % deadtime is provided for each of the two 3541 channels. Deadtime calculation is performed by calculating the duty cycle of the input busy signal from the ADC with a clock derived from an internal 10 MHz oscillator.

Model 3541 is a high density, single-width CAMAC* module measuring only 0.7 inches by 9 inches.

October 1982

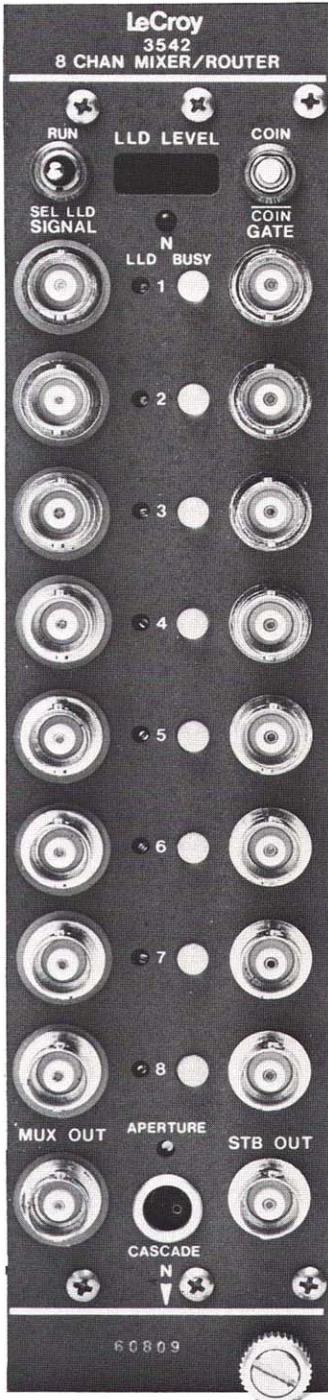
SPECIFICATIONS

CAMAC Model 3541

DUAL DEADTIMER

Deadtime Readout:	Two-digit LED display per channel of % deadtime.																												
Timing Source:	Selectable either real time or live time.																												
Preset Time Programming Range:	Two ranges — 1 millisecond to 900,000 milliseconds or 1 second to 900,000 seconds in six decade ranges each. A jumper selects the desired range. ($A \times 10^B$ sec or msec where $A=1$ to 9 and $B=0$ to 5.)																												
I/O Connector: (Rear Panel)	Dual flat cable header accepts and supplies negative logic TTL. Cable provided for direct connection to Model 3511 or 3512 ADC's.																												
I/O Signals:	ADC Busy, Bi-directional Enable/Disable.																												
LAM:	LAM is asserted when preset time is reached.																												
Package:	Single-width CAMAC* module.																												
CAMAC Functions:	<p>NOTE: N = 0 First Timer N = 1 Second Timer</p> <p>F(2) : (A(0)) – Read status bit (R16). True after timeout occurs. F(2) : (A(1)) – Read % deadtime from both channels. 16-bit word. High byte gives BCD coded % deadtime for second timer. Low byte gives BCD coded % deadtime for first timer. F(8) : (A(N)) – Test LAM. Q=1 when LAM is true. F(10) : (A(N)) – Clear LAM. F(17) : (A(N)) – Write control word. 9-bit word.* *Control Word Format-Preset Time = $A \times 10^B$ sec. W(9) : Enable/Disable deadtimer. W(8) : Select Live time/Real time. W(7)-W(5): Exponent B Factor. W(4)-W(1): BCD Digit A.</p>																												
	<table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th style="width: 10px;">B</th> <th style="width: 10px;">W(7)</th> <th style="width: 10px;">W(6)</th> <th style="width: 10px;">W(5)</th> </tr> </thead> <tbody> <tr><td>0</td><td>0</td><td>1</td><td>0</td></tr> <tr><td>1</td><td>0</td><td>1</td><td>1</td></tr> <tr><td>2</td><td>1</td><td>0</td><td>0</td></tr> <tr><td>3</td><td>1</td><td>0</td><td>1</td></tr> <tr><td>4</td><td>1</td><td>1</td><td>0</td></tr> <tr><td>5</td><td>0</td><td>0</td><td>1</td></tr> </tbody> </table>	B	W(7)	W(6)	W(5)	0	0	1	0	1	0	1	1	2	1	0	0	3	1	0	1	4	1	1	0	5	0	0	1
B	W(7)	W(6)	W(5)																										
0	0	1	0																										
1	0	1	1																										
2	1	0	0																										
3	1	0	1																										
4	1	1	0																										
5	0	0	1																										
	<p>F(24) : (A(N)) – Disable Timer N. F(26) : (A(N)) – Enable Timer N. C · S₂ – Clears LAMS. Z · S₂ – Clears LAMS and disables timers.</p>																												
Power Requirements:	+6 V at 1.1 A +24 V at 120 mA																												
Ordering Information:	Model 3541 Dual Deadtimer. Includes: Two cables to jumper each channel to a 3511 or 3512 ADC. (Specify the number of ADC's to be controlled by each channel of the deadtimer). Instruction Manual.																												

*Conforms to CAMAC standard for nuclear instrumentation modules (ESONE Committee Report EUR 4100C or IEEE Report No. 583).



CAMAC Model 3542 8-Input ADC Mixer/ Router Module

- Accepts up to 8 asynchronous 0-8 Volt analog inputs for mixing and routing to Model 3511 or Model 3514 ADC with 8 to 13-bit resolution.
- Overall throughput rate of Models 3514/3542 is 350 kHz with individual channel rate of better than 40 kHz/input.
- Independent lower level discriminators for each channel with 3-digit LED display and independent precision pots for discriminator settings.
- Independent coincidence/anticoincidence gate inputs.
- Bipolar signal inputs (all channels must be of same polarity as determined by ADC polarity selection switch).
- Compatible with either the peak detect or strobed (sampling) mode of operation in the ADC.
- Each input can be individually enabled or disabled under software control.
- Ideal for multiple detector spectroscopy experiments.
- Lower cost per ADC channel.
- Directly compatible with System 3500 MCA for acquisition, display, analysis, and I/O of spectra.

The Model 3542 eight-Input ADC Mixer Router is an accessory for Models 3511 and 3514 Spectroscopy Analog-to-Digital Converters that can significantly increase the ADC's pulse height analysis input capacity. When used with the System 3500 Multichannel Analyzer, an ADC/3542 combination effectively doubles the input capacity within the built-in System 3500 minicrate and reduces the cost per input channel by over 75% versus inputting to eight individual ADC's. For low to high resolution, medium rate, multiple input experiments, a 3511 or 3514 and 3542 combination offers an efficient, economical solution.

The 3542 is a 3-wide CAMAC module which accepts 1-to-8 asynchronous 0-to-8 volt analog inputs for mixing and routing to a single ADC and provides 8 to 13-bit resolution for each (12 bits for 3514, 13 bits for 3511). The overall data throughput rate is 350 kHz, and better than 40 kHz average for each of the eight inputs when used with a 3514.

Each channel includes an independent gate and an independent lower level discriminator adjustable from 0 to 8 volts and selectively monitored on a single 3 digit LED readout. After each conversion, System 3500 automatically routes data to that input's pre-assigned 250 to 8,000-channel data memory location.

Individual bi-color LED's indicate which channel is selected for LLD threshold readout on the 3-digit LED display and for anticoincidence/coincidence mode setting by a single front panel push-button. The color of the LED indicates which mode is selected. The LED's also flash to indicate which channels are being converted by the ADC during run time.

SPECIFICATIONS

CAMAC Model 3542

8-INPUT MULTIPLEXER/ROUTER MODULE

INPUTS (BNC)

SIGNAL 8, bipolar 0 to ± 8 V > 100 nsec risetime, input impedance 1 k ohm, DC coupled, internal delay approximately 250 nsec.

GATE 8, coincidence or anticoincidence, NIM or TTL logic compatible.

OUTPUTS (BNC)

MUX OUT 0 to 8 V, gain 1 $\pm 1\%$, BNC, to 3511 ADC DC/N.

CASCADE Differential Lemo joins two Model 3542 units operating in cascade.

STB OUT To STB/GTE on Model 3511 ADC. Precludes spurious conversions in the Model 3511.

J3 On rear panel, to connect two Model 3542 units for cascade operation.

J2 On rear panel, to connect Model 3542 to J2 of Model 3511 ADC. Cables provided.

CONTROLS

RUN/SEL LLD 3-position (1 toggle) switch used to select an input for modification of coincidence/anticoincidence or LLD setting.

COIN/COIN Pushbutton determines coincidence condition for selected input.

LLD 8, 22-turn potentiometers. Set discrimination level for each channel in the range 0 to ± 8 V. Discriminator is a symmetric window discriminator centered on zero so one setting applies to both positive and negative going pulses.

APERTURE 22-turn potentiometer sets the linear gate width to accommodate a wide range of amplifier inputs of different shaping time constants.

INDICATORS

BUSY 8, one for each input. Flashes when an input is being converted. In SEL LLD mode, BUSY LED will be illuminated for selected input.

In RUN mode, the BUSY LED flash red or green for COIN or COIN respectively.

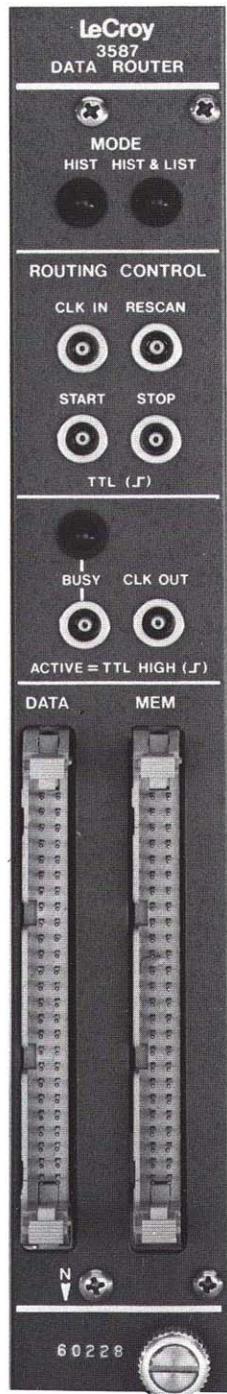
LLD LEVEL A 3-digit display of LLD setting for the selected input.

N Illuminated (in red) when module is active.

GENERAL

Power Requirements: 130 mA at -6 V
575 mA at +6 V
125 mA at -24 V
250 mA at +24 V

SPECIFICATIONS SUBJECT TO CHANGE



CAMAC Model 3587 Data Router

- Dual output ports for Histogram and/or List type memories
- Programmable dwell intervals from 100 μ sec minimum for time resolved spectroscopy
- 18-bit address space
- Routes multiple ADC's into mass memory
- 800 kHz maximum data flow
- Configuration flexibility
- Auto Rescan — time resolved summing of spectra
- Compatible with LeCroy's Spectroscopy ADC's and Model 3588 Histogramming Memory

The LeCroy Model 3587 Data Router is a memory controller for a high rate, CAMAC time-resolved spectroscopy system. It complements the LeCroy Models 3512 and 3515 Spectroscopy ADC's and the Model 3588 Histogramming Memory modules. The data router is used to marry the ADC and histogramming memory, in order to provide the user with a complete low dead time MCA system. The 3587 is capable of a maximum data flow of 1 MHz, but the actual rate depends on the ADC and/or memory configuration to which it is interconnected.

Routing of digital data from an ADC into different address spaces of the 3588 Histogramming Memory permits recording of multiple spectra. Routing on cue from a dwell clock allows time correlated sequences of spectra to be accumulated. The 3587 can manage multiple ADC's and multiple histogramming memories allowing the recording of a vast number of spectra from several inputs.

A List Mode of operation permits ADC data to be recorded either concurrently with, or instead of a histogram, by using the 3587's list output port and the Model 8201A or 8206A Memory modules. The ADC data is appended with tag bits to identify the time interval, before being written into sequential locations of the list memory.

The 3587 is applicable in high resolution gamma and soft x-ray spectroscopy systems. Of particular interest is the data router's capabilities when used in high count rate neutron spectroscopy systems, such as those required for neutral beam diagnostics and for monitoring other plasma heating techniques.

SPECIFICATIONS

CAMAC Model 3587

DATA ROUTER

MODES

HIST: Switch on side panel selects Histogram or Histogram and List modes.
 HIST & LIST: Data is histogrammed in attached LeCroy 3588 Histogramming Memory(ies).
 Data is concurrently histogrammed and sequentially listed in the attached LeCroy 3588 and 8201A or 8206A Memories respectively.
 External Control: External control signals applied at front panel start and stop the Data Router.
 Autostart: Router starts directly once it has been enabled.
 Single Scan: Router stops when Spectrum Count Register reaches zero.
 Rescan: Router returns to first memory group and repeats the routing process when Spectrum Count Register reaches zero.

ROUTING CONTROL

START: All inputs are TTL compatible, edge sensitive with optional $50\ \Omega$ internal termination. Minimum pulse width is 100 nsec.
 External Command starts routing if enabled.
 STOP: External Command stops routing if enabled.
 CLOCK IN: External Clock input defines dwell time of data routing to current memory group.
 CLOCK OUT: A positive going pulse that marks the end of the dwell interval. Drives $50\ \Omega$ load.
 RESCAN: reinstates router to preprogrammed settings and proceeds with routing.
 BUSY: Output asserted (TTL High) when router is active. LED provides visual indication. Drives $50\ \Omega$ load.

SIGNAL CONNECTIONS

DATA: External data input. 50 pin connector — 20 data, 4 control, 25 ground.
 MEM: Memory data output to LeCroy Model 3588 Histogramming memory. 50 pin connector, 4 control, 25 ground.
 NOTE: Two data cables Model DC3588/nm are needed for each Data Router.
 List Memory: Memory data output to LeCroy Model 8201A or 8206A Dual Port List Memories. 40 pin connector — 16 data, 2 control, 20 ground. LeCroy Model DC8801/nm data cable connects the List Memory to the 3587.

ROUTING PARAMETERS

Memory Group: A CAMAC accessible Memory Group Register defines the memory segment into which the data will be histogrammed. Each group is associated with a separate spectrum. The register contents are incremented at the end of each dwell clock period.
 Spectrum Count: A CAMAC readable spectrum count register defines the number of spectra remaining to be accumulated. The register contents are decremented at the end of each dwell period.
 Dwell Time: A CAMAC accessible Dwell Clock Register defines the dwell time associated with each spectrum.

CAMAC COMMANDS AND RESPONSES

X: An X = 1 (command accepted) response is generated when a valid F, A, N command is generated.
 Q: A Q = 1 response is generated in recognition of an F(8), if the LAM is set.
 L: A Look-At-Me is generated when routing is stopped due to Spectrum Count Register reaching zero or when a STOP command is input. LAM is also generated if there is a Memory Group Register overflow error on a non-existent memory address error.
 Z or C: Resets the module, Disabling the router, placing it in External Control and Single Scan Modes.

CAMAC FUNCTION CODES

F(1)•A(0): Read Memory Group Register on R1-R12.
 F(1)•A(1): Read Spectrum Count Register on R1-R8.
 F(1)•A(2): Read Dwell Clock Register on R1-R7.
 3 LSB's yield range, 4MSB's yield multiplier. See F(17)•A(2).
 F(1)•A(3): Reads Router Status Register. R1-R3 indicate current status of router. R4-R6 indicate specific reasons of LAM generation.

	R1	R2	R3
0	Router Disabled	External Clock Mode	Single Scan Mode
1	Router Enabled	Auto Start Mode	Rescan Mode
R4:	When set indicates that routing stopped due to Spectrum Count Register reaching zero or Stop Command.		
R5:	When set indicates Memory Group Register overflow error.		
R6:	When set indicates non-existent memory address error.		
F(8):	Read LAM Status: Q = 1 if LAM is set.		
F(9):	Reset module, Disable Routing, place module in External Control and Single Scan Modes.		
F(10):	Reset LAM and LAM status bits.		
F(17)•A(0):	Write Memory Group Register on W1-W12.		
F(17)•A(1):	Write Spectrum Count Register on W1-W8.		
F(17)•A(2):	Write Dwell Clock Register on W1-W7 - 3 LSB's yield range, 4MSB's yield multiplier. For straight binary decoding.		
W1-W3	0	1	2
Range	EXT	100 μ sec	1 msec
W4-W7	0	1	2
Multiplier	1	1	2
	3	4	3
	4	5	4
	5	6	5
	6	7	6
	7	8	7
	8	9	8
	9		9

Note: Ext - An external clock input or CAMAC F(25) defines the end of a dwell period.

F(17)•A(3): Writes Mode Control Register. Defines functional state of the Data Router:

	W1	W2	W3
0	Router Disabled	External Control Mode	Single Scan Mode
1	Router Enabled	Auto Start Mode	Rescan Mode

F(24): Disable LAM.

F(25): CAMAC Dwell Clock.

F(26): Enable LAM.

GENERAL

Packaging: In conformance with CAMAC standard for nuclear modules, European ESONE Committee Report EUR4100 or IEEE Standard and #583. RF shielded #2 CAMAC Module.
 Power Requirements: + 500 mA at + 6 V

SPECIFICATIONS SUBJECT TO CHANGE



CAMAC Model 3588

Fast Histogramming Memory Module

- **800 kHz Histogramming Speed.**
- **16,384 Channels (14 bits of addressing).**
- **16,777,215 counts/channels (24 bits – 1).**
- **Capacity for multiple histograms. For example: 2 histograms of 8K channels, 4 histograms of 4K channels, 1 histogram of 8K channels and 4 histograms of 2K channels, etc.**
- **Can interface to multiple ADC's and/or TDC's.**
- **Up to sixteen 3588 modules can share the same bus to allow 256K of histogramming memory.**
- **True dual port memory. Data can be read via CAMAC while histogramming is in progress.**
- **Data can be read, written or histogrammed from CAMAC for on line diagnostics.**

The LeCroy Model 3588 Histogramming Memory Module is a high density memory housed in a standard two-wide CAMAC package. It is an accessory module for Models 3512 and 3515 Spectroscopy ADC; and Model 4204 Time-to-Digital Converter Module. The 3588 is available in two memory configurations: 16,384 channels (14 bits of addressing) by 16,777,215 counts/channel (24 bits) or 32,768 channels (15 bits) by 4,095 counts/channel (12 bits).

Multiple 3512 or 3515 ADC's can be interfaced to a single 3588 Memory Module or multiple 3588s can be interfaced to a single 3512 or 3515. The latter configuration is most appropriate in time resolved spectroscopy applications in which multiple consecutive spectra are acquired at different time periods. In this application, the Model 3587 Data Router is used to provide the time switching and offset bits for acquisition in successive memory locations. A single 3587 is capable of timing and offsetting data from multiple ADC's to multiple 3588s.

Multiple Model 4204 TDC's can also be interfaced to one or more 3588 Memory Modules either with or without the 3587 Data Router.

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SPECIFICATIONS

CAMAC Model 3588

FAST HISTOGRAMMING MEMORY MODULE

MODE SELECTION See CAMAC commands.

HISTOGRAMMING MODE

Inputs: Input lines can be either front panel connector or CAMAC Dataway. 50-pin front panel connector—TTL levels. 4 control, 20 address (14 for addressing and 6 address lines for module decode are available, but physical crate space and bus cable length limit the number of usable address lines to 4), 25 grounds.

Function: Read data from address on input lines, add one, and rewrite at same memory address.

Control: Handshake between ADC's or TDC's and 3588s to arbitrate priorities and timing. Maximum rate of 800 kHz. Minimum rate—none.

MEMORY STATUS

Busy: Lemo TTL output level asserted during CAMAC memory access, histogramming cycle, or when front panel histogram port is disabled.

Enable: LED indicates histogram port inputs enabled.

CAMAC Access: LED indicates CAMAC memory access.

External Access: LED indicates front panel histogram port memory access.

MEMORY

Type: 16K dynamic RAM with onboard refresh.

Speed: 1.2 μ sec read/modify/write.

Size: Configured as 16K, 24 bits deep or 32K, 12 bits deep.

CAMAC COMMANDS AND RESPONSES

Z, C: Reset module and zero all memory contents.

LAM: Set if any histogramming channel contents overflow or when memory has self cleared after reset.

X: X = 1 Response is returned only for valid F, N, and A.

Q: Q = 1 Response is returned for memory read function only when data is valid.

CAMAC FUNCTION CODES

F(1): Read LAM Register.

F(2): Read data, Q = 1 if valid data available. Once a CAMAC read cycle F(2) is requested, data will be fetched only when no ADC or TDC request is present. For high data rates it may be necessary to poll the 3588 with F(2) until a Q = 1 is returned. If this is not possible, the ADC port can be disabled which gives CAMAC highest memory priority.

F(8): Test LAM. Q = 1 returned if internal LAM is on.

F(9): Reset module, zero all memory contents and set auto increment mode.

F(10): Reset LAM & LAM Register.

F(11): Enable front panel histogramming port.

F(16): Write data into location given by Memory Address Register.

F(17): Disable auto increment of Memory Address Register.

F(18)•A(0): Load Memory Address Register via CAMAC for a subsequent CAMAC write cycle F(16).

F(18)•A(1): Load Memory Address Register via CAMAC, fetch data for a subsequent CAMAC read cycle F(2), and increment to the next memory address if auto increment is enabled.

F(18)•A(2): Load Memory Address Register via CAMAC and increment the corresponding memory contents by one (CAMAC histogramming).

F(19): Disable port for histogramming.

F(24): Disable LAM.

F(25): Enable auto increment of CAMAC Memory Address Register.

F(26): Enable LAM.

GENERAL

Packaging: In conformance with the international CAMAC standard (IEEE Std. #583 and ESONE Report #4100e). RF shielded #2 width module.

Current Requirements: 1 A at + 24 V or 820 mA at + 12 V (jumper selected) while memory active (CAMAC or HIST).

100 mA at + 24 V or 75 mA at + 12 V (jumper selected) while memory idle.

1.5 A at + 6 V.

20 mA at - 6 V.

TECHNICAL DATA

LeCroy

Models 3910-2B (Includes 3910-2A and 3910-5) Fortran Software and Fortran Support Software Accessories for System 3500



FEATURES

- CAMAC library allows control of CAMAC modules through Fortran
- Complete graphic package with "screen dump" capability
- Direct communication between Fortran programs and System 3500 histogramming memory
- Hardware mathematical operations reduce program execution time
- Fortran-80® enhances the 1966 ANSI standard

INTRODUCTION

The LeCroy Model 3910-2B contains all the software necessary to create and execute Fortran programs using the System 3500 and the Model 3921 dual disc drive accessory. This software consists of a Model 3910-2A diskette which includes a Microsoft Fortran-80 Version 3.44 compiler, linker, library, library manager, and macro assembler. The Model 3910-2B also includes the Model 3910-5 diskette which contains support software that enables the user to perform CAMAC I/O, link to the arithmetic processing unit for hardware arithmetic operations, communicate directly with data memory, drive extra RS-232-C ports, perform bit manipulations, do graphics on the screen or on the printer, and perform interrupt processing.

SOURCE FOR PROGRAM KEYPAD.FOR

```

PROGRAM KEYPAD
LOGICAL X,Q
INTEGER D,W,A,F,N,RD,WD
DIMENSION KP(5,2),RD(1000),WD(1000)
EQUIVALENCE (RD(1000),WD(1000))
DATA KP/'C','W','A','F','N',5*0/
KPM = 5
KPK = 2

C   INITIALIZE CAMAC CRATE
CALL CAMCTL(0,1)

C   INITIALIZE PLOT
360 CALL PLINIT
CALL PLTCLS(0)

C   WRITE TEXT
99  WRITE(1,99)
FORMAT(1X,'This program allows the user to enter CAMAC slot
1 number (N),function',/,'(F),subaddress (A),crate (C),and
1 16 bit write data (W) as inputs, and',/,'to execute CAMAC cycles
1 in one of three modes. The above prompts are',/,'entered
1 by pressing the desired prompt key and then
1 typing the decimal',/,'value followed by RETURN.',/,',
1 'Single step mode'
1 generates a CAMAC cycle with every depression of the',/,
1 'SNGL STEP key. SLOW mode generates repeated cycles and both
1 give up',/,
1 'dates on the monitor of read or write data and the current
1 prompt values.',/,'The cycles are stopped by pressing any
1 keypad key. FAST mode gener',/,'ates 1000 consecutive cycles
1 before displaying the values of data and',/,'prompts of the
1 thousandth cycle. This is useful for exercising a CAMAC',/,
1 'module while trouble-shooting. ',/,'The keypad does not
1 generate interrupts, but is a polled port. There',/,'fore it
1 may be necessary to hold a key momentarily before the function'
1 ',/,'is executed.',/,',
1 'Pressing any undefined key will return the keypad overlay.
1 Pressing',/,'"HELP" will return this text. "EXIT"
1 will return the Disc Operating',/,'System',/,',
1 'Type RETURN to continue.')
PAUSE
GOTO 380

C   ERROR MESSAGE
350 CALL PLINIT
CALL WRTSYM(20,20,'INVALID KEYPAD ENTRY: TRY AGAIN!',32,0.0)
GOTO 381

C   SET ORIGIN OF PEN
380 CALL PLINIT
381 CALL PLOT(200,48,-3)
C   DRAW KEYPAD OVERLAY
382 CALL PLOT(160,0,2)
CALL PLOT(160,25,3)
CALL PLOT(0,25,2)
CALL PLOT(0,50,3)
CALL PLOT(160,50,2)
CALL PLOT(160,75,3)
CALL PLOT(0,75,2)
CALL PLOT(0,100,3)
CALL PLOT(160,100,2)
CALL PLOT(160,0,2)
CALL PLOT(120,0,3)
CALL PLOT(120,100,2)
CALL PLOT(80,100,3)
CALL PLOT(80,0,2)
CALL PLOT(40,0,3)
CALL PLOT(40,100,2)
CALL PLOT(0,100,3)
CALL PLOT(0,0,2)

C   WRITE SYMBOLS INTO OVERLAY
480 CALL WRTSYM(18,92,'N',1,0.0)
CALL WRTSYM(58,92,'F',1,0.0)
CALL WRTSYM(98,92,'A',1,0.0)
CALL WRTSYM(138,92,'W',1,0.0)
CALL WRTSYM(6,67,'FAST',4,0.0)
CALL WRTSYM(6,42,'SLOW',4,0.0)
CALL WRTSYM(125,67,'CRATE',5,0.0)
CALL WRTSYM(6,20,'SNGL',4,0.0)
CALL WRTSYM(6,8,'STEP',4,0.0)
CALL WRTSYM(129,17,'HELP',4,0.0)
CALL WRTSYM(86,17,'EXIT',4,0.0)
CALL PLTCLS
KPM = 5

C   POLL AND DECODE KEYPAD
300 KPI = INP(253)
KPK = KPI + 1
GOTO(900,360,350,420,420,420,420,420,350,350,400,350,
1 350,400,400,520),KPK

C   SELECT 'MODE' IF NO KEYPAD ACTION
520 GOTO(460,350,350,450,300)

C   PRINT 'MODE'
400 KPM = KPK - 10
GOTO(401,405,405,402,403),KPM
405 GOTO 300
401 WRITE(1,141)
GOTO 460
402 WRITE(1,142)
GOTO 450
403 WRITE(1,143)
GOTO 450
141 FORMAT(1X,' FAST MODE')
142 FORMAT(1X,' SLOW MODE')
143 FORMAT(1X,' SINGLE STEP MODE')

C   UPDATE PROMPT AFTER KEYPAD ENTRY
420 KPM = 5
KPP = KPK - 3
WRITE(1,130)KP(KPP,1),KP(KPP,2)
IF(KPP.NE.2)GOTO 422
130 FORMAT(1X,A2,=',I6,' NEW VALUE =')
422 READ(1,132)KP(KPP,2)
FORMAT(16)
IF(KPP.NE.1)GOTO 421
CALL CRATE(KP(1,2))
421 GOTO 300

C   STANDARD READ CAMAC CYCLE
450 IF(KP(4,2).GE.16)GOTO 458
CALL CAMI(KP(5,2),KP(4,2),KP(3,2),X,Q,D)

C   FIND VALUES OF X, Q, AND LAM
456 IF(X) GOTO 451
IX = 0
GOTO 452
451 IX = 1
IF (Q) GOTO 453
IQ = 0
GOTO 454
453 IQ = 1
L = LAM(0)
IF(KPM.EQ.1)GOTO 466
GOTO 480

C   STANDARD WRITE CAMAC CYCLE
458 CALL CAMO(KP(5,2),KP(4,2),KP(3,2),KP(2,2))
GOTO 480

C   FAST MODE BLOCK CAMAC CYCLE
460 IF(KP(4,2).GE.16)GOTO 465

C   BLOCK READ CYCLES
466 CALL BLK16(KP(5,2),KP(4,2),KP(3,2),X,Q,RD,1000)
GOTO 456
D = RD(1000)
GOTO 480

C   LOAD WRITE DATA ARRAY: 1000 TIMES W
465 DO 467 I = 1,1000
467 WD(I) = KP(2,2)

C   BLOCK WRITE CYCLES
480 DISPLAY N,F,A,CRATE,AND W OR R
WRITE(1,100)KP(5,2),KP(4,2),KP(3,2)
100 FORMAT(1X,'N =',I2,'F =',I2,'A =',I2)
IF(KP(1,2).EQ.0)GOTO 482
WRITE(1,105)KP(1,2)
105 FORMAT(1X,'CRATE =',I2)
IF(KP(4,2).GE.16)GOTO 485
WRITE(1,110)IX,IQ,L
110 FORMAT(1X,'X =',I2,'Q =',I2,'LAM =',I2)
482 WRITE(1,112)D
483 FORMAT(1X,'READ DATA =',I6)
112 GOTO 300
485 WRITE(1,115)KP(2,2)
FORMAT(1X,'WRITE DATA =',I6)
115 GOTO 300

C   STOP
900 STOP
END

```

FORTRAN-80®

Microsoft Fortran-80® is the most complete implementation of the Fortran language available for 8080 microprocessors. It is comparable to compilers on large mainframe computers. The Fortran-80® package includes full ANSI standard Fortran X3.9—1966 except for the COMPLEX data type. It enhances the 1966 ANSI standard in the following ways.

1. Single byte LOGICAL variables which can be used as integer quantities in the range + 127 to – 127.
2. DO loops which use LOGICAL variables for tighter, faster execution of small loops.
3. Mixed mode arithmetic expressions.
4. Hexadecimal constants.
5. Hollerith (character) literals accepted.
6. Logical operations on integer data. .AND., .OR., .NOT., .XOR. can be used for 8 bit, 16 bit, or 32 bit Boolean operations.
7. READ/WRITE End of File or Error Condition Transfer. END = n or ERR = n (where n is the statement number) can be included in READ or WRITE statements to transfer control to the statement specified by n when an error or file end is detected.
8. ENCODE/DECODE for FORMAT operations to memory.
9. IMPLICIT statement for redefining default variable types by specifying a type and a range of initial letters.
10. INCLUDE statement for including commonly used subroutines, code, or declarations from another file.
11. INTEGER*4 variables and constants using 32 bits in the range of + 2,147,483,647 to – 2,147,483,648.
12. Support for CP/M™ version 2.x providing access to a maximum of 65,536 records in a file as large as 8 megabytes.

Functions that are “built in” to Fortran-80® include the logarithm (natural and common), exponential, sine, cosine, square root, arc tangent, hyperbolic tangent, absolute value, maximum, minimum, positive difference, transfer of sign, conversion between integer and real, conversion between single and double precision, and modulo n. Also provided is a random number generator and routines that allow a Fortran program direct access to program memory and the I/O ports.

3910-2A DESCRIPTION

Filename	Description
F80.COM	Fortran-80® Version 3.44 compiler. Processes several hundred statements per minute in a single pass; uses less than 27K bytes of memory to compile most programs; generates diagnostic outputs; aids program efficiency by common subexpression elimination (common subexpressions are evaluated once only, peephole optimization (small sections of code are replaced by more compact code), constant folding (integer constant expressions are evaluated at compile time), and branch optimization (number of conditional jumps in arithmetic and logical IF's is minimized); produces a relocatable file to be linked and loaded at run time.
L80.COM	Link 80 relocating loader. Performs library searches for system subroutines while requiring no more than 10K bytes of program memory. Produces an executable file.
M80.COM	Macro 80 relocating assembler. Includes complete Intel standard Macro facility; provides a full set of conditional pseudo-operations, conditional listing control, comment blocks, octal or hex listings, and a variable input radix; accepts Intel 8080 mnemonics; resides in approximately 19K bytes of program memory.
FORLIB.REL	Library of Fortran functions. Provides for program initialization, termination, I/O, and arithmetic functions.
LIB.COM	Library manager. Aids in creation and modification of libraries.

® Fortran-80 is a trademark of Microsoft

TM CP/M is a trademark of Digital Research

3910-5 DESCRIPTION

Filename	Description
APU.REL	APU library. Provides hardware mathematical operations such as square root, sine, cosine, etc, when linked to a Fortran program.
BITLIB.REL	Bit manipulation library. Permits bit manipulations to be performed on 16-bit integers. Operations include the logical functions AND, OR, NOT, and XOR, shifts, set, clear, and individual bit tests.
CAMAC.REL	CAMAC library. Routines permit the user to execute one CAMAC cycle, read or write 16 or 24 bit integer data, manipulate CAMAC control lines, transfer blocks of data, execute DMA (direct memory access) cycles, and reference the System 3500 minicrate or external CAMAC crates.
HMUTIL.REL	Histogram memory utility. This package allows direct access to System 3500 histogram memory from a Fortran program. Routines permit the two way transfer of data between a Fortran array and data memory, addition of an integer to memory contents, and access to multiple histogram memory boards.
LPTDRV.REL	Line printer drive. This module may replace the line printer module in the Fortran library. It defines logical units 11 through 14 which correspond to the four extra RS-232-C I/O ports on the LeCroy Model 3500-35 Quad Serial Interface Board. (NOTE: This software must be used with the 3500-35.)
OVLAY.REL	Routines for overlaying program segments in memory. Used in programs that exceed the program memory area.
FIXADR.COM	OVLAY utility. Assists OVLAY by determining, from the linker, the address of the subroutine to be overlaid.
PLOTLIB.REL	Plotting library. These routines draw lines, label axes, define light pen regions, provide 13 levels of shading (suitable for 3 dimensional plots), and allow contents of screen to be printed.
SETINT.REL	Interrupt processing library. Allows one subroutine to service interrupts from up to 8 devices. Runs under the standard disc operating system only.
TIMER.REL	Timing functions. Routines set up time intervals based on the frequency of the line voltage, provide programmable delays in program execution, and time programs or program segments.
TTYIO.MAC	Routine to perform I/O to RS-232-C port from a Fortran program.
KEYPAD.FOR	Sample Fortran program. Demonstrates the use of CAMAC.REL and PLOTLIB.REL. The source code for this program is listed below.

ORDERING INFORMATION

Models 3910-2B includes two diskettes (Models 3910-2A and 3910-5) and is supplied with System 3500SA, System 3500M with 3921 Disc Drive option, Model 3500MP, and Model 3921 upgrade for system 3500M. In all cases, a Fortran manual and the System 3500 Operator's Manual will be included.

SPECIFICATIONS SUBJECT TO CHANGE

Software Product Description Screen Oriented Editor Cat. No. 3910-15

- Faster Program Editing
- Replication of Program Routines
- File Structuring
- Printer Formatting

The Screen Oriented Editor is an optional software package for the LeCroy 3500M which gives the 3500M vastly improved text editing capability so that the programmer has fast, thorough control of program content and structure. The word processing commands are extremely flexible and provide a powerful means of manipulating information directly on the CRT screen. The Screen Oriented Text Editor is far superior to the standard Line Editor because the movable cursor permits direct access to text locations. The system keypad quickly and easily positions the cursor to find places to delete, insert, change, move, or copy. The Screen Oriented Editor may be used as a program editor, as an aid in structuring files, as a means of formatting printed output, or even (as a bonus), a conventional word processor.

The word processing commands provide the user with a simple means of deleting, inserting, and moving characters, lines, or blocks of text. Typical commands for this purpose include CHARACTER INSERT, LINE DELETE, and WORD DELETE. A SCROLL command permits movement of the text, backwards or forwards on the screen, either one line, or one page at a time.

Specific commands allow the user to manipulate the various files, or portions of files, for convenient access and use. For example, the INCLUDE command allows the user to merge part or all of one file with another file he is editing. This command is used most frequently to copy common pieces of a program. A typical example is the inclusion of shared variables in FORTRAN subroutines. Other commands allow the user to create data files for display or output. HELP files, for example, can be designed for reference use only, with no text generated.

PRINT commands give the user flexible control of printed formats, including text shape, placement on the page, margins, spacing, etc. Another set of commands allows access to external data files so they can be output to a specific location of the text. Other commands allow the user to fill in the value of variables at run time, by typing them at the keyboard when the text is actually printed.

The above description covers only a few examples of the many features and uses of the Screen Oriented Editor. The commands are summarized below.

SUMMARY OF FEATURES

Character Delete	Merging files	Indentations
Character insert	Underscoring	Page length
Scrolling	Subscripting/Superscripting	Centered text
Word delete	Reference files	Proportional spacing
Line delete	Data files	Justified text
Block movement	Margins	Bold face
Block delete		Headers/footers

SPECIFICATIONS SUBJECT TO CHANGE

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Model 3921

Dual Drive Floppy Disc Accessory For System 3500

Introduction

The LeCroy Model 3921 Dual Disc Drive is an accessory for LeCroy's System 3500M Multichannel Analyzer, and converts it to the 3500MP Programmable MCA. Model 3921 is a random access memory device that records and retrieves data on two removable, flexible diskettes. It provides 243 kilobytes per drive of data or program storage in IBM 3740 format when formatted for single density storage or 486 kilobytes per drive when formatted for double density.

Model 3921 consists of a Dual Drive unit, a Disc Controller Interface board (3500-8), diskettes containing the System 3500 Disc Operating System, Fortran or Basic software, Fortran or Basic support software including CAMAC I/O, PLOT, and APU libraries and other support utilities. With the System 3500MP Multichannel Analyzer, MCA support and User Analysis software is also included. By addition of Model 3921, System 3500M becomes a fully programmable Multichannel Analyzer and/or a CAMAC Data Acquisition and Control System, with the added advantage of having a dedicated, high speed random access bulk data storage capability.

In addition to providing data storage, Model 3921 provides complete software programming facilities in a high level language for user access to the 3500's microprocessors and computer memory. The standard software is supported by extensive graphics, plotting, and CAMAC and Multibus™ I/O routines to fully automate data collection, control, analysis, and communication with other computers.

Field Expansion

A second Dual Disc Drive unit, can be added to a System 3500 equipped with a Model 3921 to double storage capacity. Since the Disc Controller interface board supports two Dual Drive units, no additional interface hardware is required. Both models are equipped with the necessary connecting cables.



System 3500

Model 3921

Features

Compact The LeCroy Dual Disc Drive unit is 5.25" high, 17.6" wide, 21.0" deep, and can be mounted in a 19" rack.

Reliable The Shugart drive system has proven itself as the industry standard for performance and reliability. Modular construction permits plug-in replacement for minimum down time.

Diskette protection A fully automatic diskette load and unload feature assures simple diskette insertion, accurate diskette positioning, and eliminates the possibility of diskette damage.

IBM compatibility The Read/Write/Erase head of the Dual Disc Drive unit is compatible with IBM 3740 system; therefore, diskettes prepared on the IBM 3740 system can be read by the disc drive and vice versa.

RT-11® compatibility Data stored on LeCroy diskettes can be read by other mini- or micro-computer disc drives, such as those supported by Digital Equipment Corporation's RT-11 or RSX-11 operating systems.

TM Multibus is a trademark of Intel Corporation and conforms to IEEE Standard 796-1978.

RT® is a trademark of Digital Equipment Corporation.

SPECIFICATIONS

Model 3921

DUAL DRIVE FLOPPY DISC ACCESSORY

	Single Density	Double Density
Capacity:		
Without system tracks	256 K bytes/diskette	512 K bytes/diskette
With system tracks	243 K bytes/diskette	486 K bytes/diskette
Number of tracks	77/surface	77/surface
Number of sectors	26/track	26/track
Bytes per sector	128	256
Drives per chassis	2	2
Track Density:	48 tracks per inch (inner track)	
Bit Density:	3200 bits per inch	
Rotational Speed:	360 RPM ± 2%	
Transfer Rate:	250 KHz off diskette	
Operating Time:	Track-to-track access: 8 msec (including settle time) Random average seek: 296 msec 76 track seek: 635 msec Head engage: 35 msec	
Controls and Indicators:	Rear Panel: Power ON-OFF switch Front Panel: Diskette eject push button (on each drive); Head read/write LED indicator (on each drive).	
Physical Dimensions:	Height: 5.25" Width: 17.6" Depth: 21.0" Weight: 48 lb., 6 oz	
Operation Environment:	Temperature: 60 - 104°F Relative Humidity: 10% - 95%	
Power Requirements:	110 or 220 V AC 50 or 60 Hz (must be specified)	
Power Consumption:	138 W (nominal) 166 W (maximum)	
Heat Dissipation:	317 BTU/Hr (idle) 471 BTU/Hr (busy)	
Media:	IBM 3740 Diskette or Memorex 3201-3090 (capable of single or double density storage) with write-protect and soft sectoring.	

MODEL 3201-3090 DISKETTE SPECIFICATIONS

Durability:	2 million passes
Substrate:	3 mil polyester
Coating:	Thickness: 110 microinches nominal gamma ferric oxide Surface Roughness: 3 microinches or less, arithmetic average
Dimensions:	Diameter: 7.88" Inside Diameter: 1.50" Index Hole: 0.1"
Jacket Characteristics:	Outside Dimensions: 8 inches square Material Thickness: 0.01" Total Jacket Thickness: 0.072" Material: Matte vinyl
Environment:	Operating Temperature: 50-125°F Non-operating Temperatures: - 40 to 125°F

ORDERING INFORMATION

Model 3921 includes:

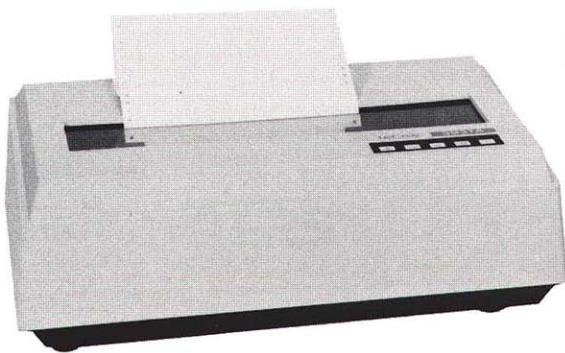
1. Dual Disc Drive Unit
2. Disc Controller Interface (Single and Double Density)
3. Diskettes containing LeCroy's 3500 Operating System, Fortran or Basic software, MCA support software, MCA User Analysis software, and utility software
4. Interconnecting cable to System 3500
5. Line cord
6. Instruction manuals

SPECIFICATIONS SUBJECT TO CHANGE

TECHNICAL DATA

LeCroy

Model 3931A Printer/Plotter



Model 3931A



System 3500

The Model 3931A Printer/Plotter is a compact, inexpensive line printer with full graphics plotting facilities. This dual capability makes it exceptionally useful in experiments requiring both tabular listings of data as well as plots of the graphic display. The graphic output to the 3931A is a "screen dump" in which the display is exactly duplicated by the plotter including alphanumerics. This exclusive feature permits the user to select and view exactly the data to be output. The print speed of the 3931A is 90 characters/second and the screen dump plot is executed in approximately 90 seconds. Fanfold paper measuring 9 by 11 inches is continuously fed by a pin feed mechanism.

SPECIFICATIONS

Model 3931A

PRINTER PLOTTER

Printhead:	9 wire vertical (Ballistic type) 150 cps (characters per second) (75 cps for correspondence quality) Lifetime of 600 million characters 9 x 9 or 9 x 18 matrix
Printer Mechanism:	Form thickness adjustment Slew rate: 4 inches/second Paper advance: 25 msec/line Character height: .105 inch Character width: .075" at 10 cpi (characters per inch), .062" at 12 cpi, .045" at 16.5 cpi Characters per line: 80 at 10 cpi, 96 at 12 cpi, 132 at 16.5 cpi
Paper:	Type: Labels, Single sheet, Roll paper, Fan fold, Multi-part (6 parts maximum) Drive: Tractor adjustable from 1.5" to 10" Forms Control: 11 or 12 inch top of form, 6 line perforation skip (operator selectable), 7 channel Vertical Forms Unit (VFU), Paper out indicator, Vertical tabs
Operator Controls:	Power: On/Off On-line: On-line/Off-line (hold) Reset: Initializes printer electronics and top of form is set at present paper position. Step: Advances paper incrementally when held for less than .5 seconds or slews paper at 4 inches per second (ips) when held for over .5 seconds without changing the top of form position. Top of Form: Advances paper to next top of form. Test: Initializes self-test.
Operator Indicators:	Power: Indicates AC power is on and + 5 volts is available. Paper Out: Indicates printer is out of paper. Top of Form: Indicates at top of form only. On-line: Indicates printer is on-line to host CPU.
Interface:	Parallel: Centronics plug compatible; 7 bit with busy acknowledge handshake Serial: EIA RS232-C or current loop Baud Rate: 110, 300, 1200, 2400, 4800, or 9600 (user selectable) Stop Bits: 1 or 2 Data Bits: 7 or 8 Parity: Odd, even, or no parity Protocol: Character busy, buffer full busy, X-On/X-Off
Power:	Voltage: 80 to 125 volts or 220 to 260 volts Frequency: 47 to 63 Hz Power: 75 watts maximum
Electronic Features:	Bidirectional Logic seeking 96 character ASCII set Input Buffer: 350 to 3422 characters
Programmable Features:	6 or 8 lpi (lines per inch) 10, 12, or 16.5 cpi Double width Double density at 10 cpi Superscripts Subscripts VFU (7 channel) Vertical tabs Forms length Graphic mode

Ribbon:

Type: Cartridge
Material: Nylon
Width: .5 inch
Thickness: .004 inch
Length: 45 feet \pm 6 inches
Path: Endless mobius loop
Ink: Permanent dye-based matrix ink

Environmental:

Noise: 60 dba (decibals above ambient)
Temperature: 5 to 35°C. (operating), -10 to 65°C. (non-operating)
Relative humidity: 10% to 99% (operating), 5% to 95% (non-operating)
Temperature change: 10°C./hr. (operating), 30°C./hr. (non-operating)
Altitude: 0 to 10,000 ft. (operating), 0 to 40,000 ft. (non-operating)

Physical:

Size: 7.25" high, 21.25" wide, 16.5" deep
Weight: 30 lbs. (13.6 kg.)

SAMPLE OUTPUTS

Four sample outputs from a Model 3931A Printer/Plotter follow. The Summary tabular output gives a brief description of the data and setup parameters for a given graph. The Extended tabular output lists all the setup parameters plus the contents of each channel of the selected graph. The Screen Dump output exactly reproduces the contents of the screen. With the System 3500M, all three modes can be selected from the OUTPUT SETUP menu shown below.



LeCroy 3511 ADC PARAMETERS
TITLE: CS 137
ACQUISITION DURATION = INFINITY
(HH:MM:SS OR "INF")
CONVERSION GAIN = 8K
DATA MODE (0=ADD,1=SUB) = 0
ACQUISITION TIME = 48:00:00
AREA = 115544759
START CHANNEL = 5850
STOP CHANNEL = 5900

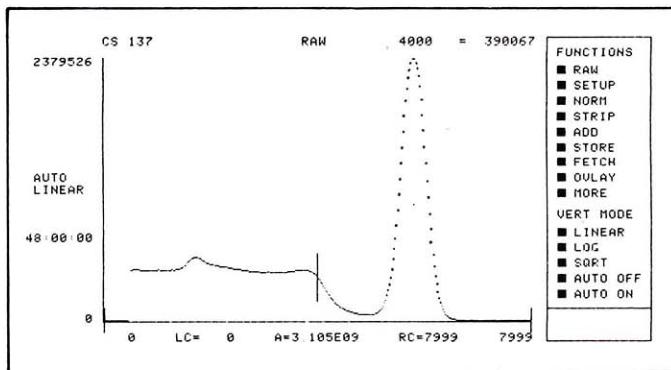
CS 137 ROI # 4
% AREA = 25
AREA = 115544759

5850:	2331918	2338323	2324860	2326477	2314693	2330569	2330697	2320113
5859:	2315780	2318112	2311324	2312892	2302173	2308509	2299178	2300545
5864:	2294894	2298706	2286583	2284853	2279386	2286033	2283746	2281990
5874:	2275902	2275866	2263921	2270571	2255334	2260032	2249924	2252129
5882:	2245582	2241903	2231990	2227655	2198260	2242087	2252683	2222920
5890:	2221813	2222636	2211772	2207211	2197291	2204689	2193790	2191187
5898:	2185147	2183442	2174776					

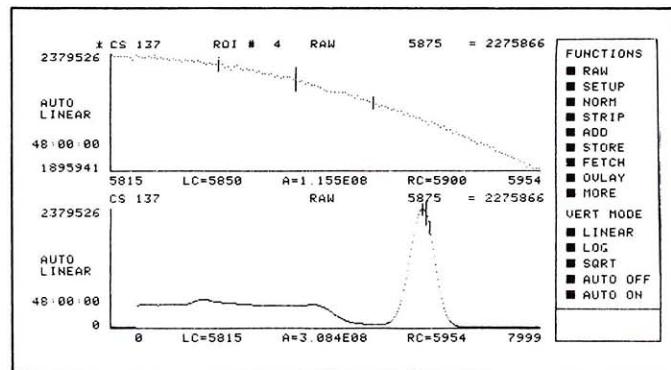
Extended tabular output for 50 channels of an 8000 channel CS-137 spectrum.

LeCroy 3511 ADC PARAMETERS
TITLE: CS 137
ACQUISITION DURATION = INFINITY
(HH:MM:SS OR "INF")
CONVERSION GAIN = 8K
DATA MODE (0=ADD,1=SUB) = 0
ACQUISITION TIME = 48:00:00
AREA = 310553790
START CHANNEL = 0
STOP CHANNEL = 7999

Summary tabular output of an 8000 channel CS-137 spectrum



Screen dump output of CS-137 spectrum in single display mode.



Screen dump output of CS-137 spectrum plus ROI #4.

ORDERING INFORMATION

The Model 3931A includes

1. Interface Firmware/Software for System 3500
2. Data cable for direct interface to RS-232-C port on the System 3500
3. Approximately 50 sheets of fanfold pinfeed paper
4. Instruction Manual

SPECIFICATION SUBJECT TO CHANGE

Appendix A

NIM Standard

NIM is a packaging standard for instrumentation used primarily in high energy, nuclear and cosmic ray physics. The term is an acronym, standing for Nuclear Instrumentation Module. For details of the standard, see report TID20893 distributed by the U.S. Government printing office.

A NIM power chassis, such as LeCroy Model 1402 accepts up to 12 NIM modules. It supplies power and ground (and a "Bin Gate" in most U.S. manufacturing bins) to the modules it houses. Each of the 12 slots contains a multipin block connector which contacts the module as it is inserted. The NIM standard allows a variety of devices to use a common set of power supplies and defines a standard mechanical package.

Although some manufacturers have used the NIM standard for data acquisition systems, this standard is principally used for instruments which have front panel inputs and outputs only. Examples of modules commonly packaged in NIM are logic units (discriminators, coincidence units, etc.) and linear electronics (amplifiers, fan-ins, etc.).

The NIM standard specifies a chassis with six well-regulated, low-noise ± 24 V, ± 12 V and ± 6 V DC power supplies. Caution: The first version of the NIM standard did not specify the ± 6 V supplies so older chassis may be lacking these voltages. Most modern NIM modules will not operate in these chassis.

The top and the bottom of the NIM chassis are slotted to provide a path for cooling air. NIM modules are designed with slots or gratings allowing air to enter from the crate, pass through the module and exit

through the top. When installing NIM bins in an electronics rack, it is necessary to leave clearance above and below the NIM chassis to allow for air flow. Air should be baffled so the hot air exiting one chassis does not enter the next chassis.

Although the "NIM" logic levels have specific ranges defined for input and output signals, for most practical purposes, a "logical 1" in the NIM standard can be considered to be -16 mA or -800 mV into 50Ω , and a "logical 0" 0 volts or 0 mA.

CAMAC Standard

CAMAC is an instrumentation system which has been developed specifically for accommodating digital circuits. The system definition, which has become the standard for nuclear digital data acquisition systems, was prepared by the ESONE (European Standards on Nuclear Electronics) Committee and has been adopted by the United States NIM Committee. The system has been accepted by all of the major accelerator laboratories and a large number of industries, and modular components are available from a large number of firms.

One of the most important features of CAMAC is that it uses a multiwire printed circuit dataway mounted at the rear of the power crate to provide a large number of interconnections between modular hardware without external cabling. It provides for bidirectional communication between modules and the computer or between modules themselves, thus allowing digital control of modules in addition to the more common data acquisition function.

The CAMAC crate is designed to accept up to 25

modules via 86-pin card-edge connectors mounted on the printed Dataway. Operationally, 23 of these connectors (or stations) are used for modules like ADC's, scalers, registers, etc. The remaining two are utilized by a crate controller. The smallest (single width) CAMAC module is half the width of the NIM single-width module. This compact package is more compatible with the high-density integrated circuits now used extensively and, in conjunction with the small size of the standard Lemo connector, permits a substantial reduction in physical size of a typical system.

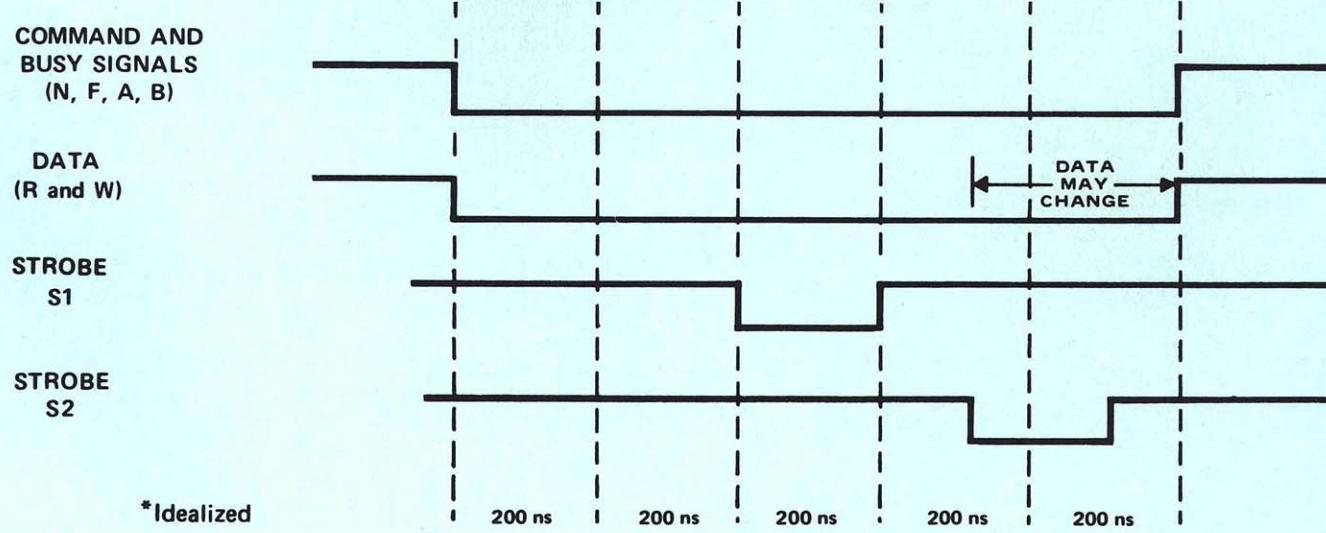
Local control of modules within a crate is provided by the standard Type A1 or Type A2 crate controller which accepts external commands from the branch highway. The branch highway is a separate cable data bus which interconnects Type A controllers in several crates with a branch driver-interface for the data processor in use. Branch drivers are available for most popular computers from a variety of manufacturers.

Detailed specifications covering the CAMAC system are contained in ESONE Report EUR 4100. A brief summary of CAMAC function codes, pin allocations, timing, and standard dataway usage is also presented here.

CAMAC Function Codes

CODE F()	FUNCTION	FUNCTION SIGNALS					CODE F()
		F16	F8	F4	F2	F1	
0	Read Group 1 Register	0	0	0	0	0	0
1	Read Group 2 Register	0	0	0	0	1	1
2	Read and Clear Group 1 Register	0	0	0	1	0	2
3	Read Complement of Group 1 Register	0	0	0	1	1	3
4	Non-standard	0	0	1	0	0	4
5	Reserved	0	0	1	0	1	5
6	Non-standard	0	0	1	1	0	6
7	Reserved	0	0	1	1	1	7
8	Test Look-at-Me	0	1	0	0	0	8
9	Clear Group 1 Register	0	1	0	0	1	9
10	Clear Look-at-Me	0	1	0	1	0	10
11	Clear Group 2 Register	0	1	0	1	1	11
12	Non-standard	0	1	1	0	0	12
13	Reserved	0	1	1	0	1	13
14	Non-standard	0	1	1	1	0	14
15	Reserved	0	1	1	1	1	15
16	Overwrite Group 1 Register	1	0	0	0	0	16
17	Overwrite Group 2 Register	1	0	0	0	1	17
18	Selective Set Group 1 Register	1	0	0	1	0	18
19	Selective Set Group 2 Register	1	0	0	1	1	19
20	Non-standard	1	0	1	0	0	20
21	Selective Clear Group 1 Register	1	0	1	0	1	21
22	Non-standard	1	0	1	1	0	22
23	Selective Clear Group 2 Register	1	0	1	1	1	23
24	Disable	1	1	0	0	0	24
25	Execute	1	1	0	0	1	25
26	Enable	1	1	0	1	0	26
27	Test Status	1	1	0	1	1	27
28	Non-standard	1	1	1	0	0	28
29	Reserved	1	1	1	0	1	29
30	Non-standard	1	1	1	1	0	30
31	Reserved	1	1	1	1	1	31

DATAWAY Timing*



Pin Allocation at Normal Station

(Stations 1-24)

Bus-line	Free Bus-line	P1	B	Busy	Bus-line
Bus-line	Free Bus-line	P2	F16	Function	Bus-line
Individual patch contact		P3	F8	Function	Bus-line
Individual patch contact		P4	F4	Function	Bus-line
Individual patch contact		P5	F2	Function	Bus-line
Bus-line	Command Accepted	X	F1	Function	Bus-line
Bus-line	Inhibit	I	A8	Sub-address	Bus-line
Bus-line	Clear	C	A4	Sub-address	Bus-line
Individual line	Station Number	N	A2	Sub-address	Bus-line
Individual line	Look-at-Me	L	A1	Sub-address	Bus-line
Bus-line	Strobe 1	S1	Z	Initialize	Bus-line
Bus-line	Strobe 2	S2	Q	Response	Bus-line
		{ W24 W22 W20 W18 W16 W14 W12 W10 W8 W6 W4 W2 R24 R22 R20 R18 R16 R14 R12 R10 R8 R6 R4 R2 }	W23 W21 W19 W17 W15 W13 W11 W9 W7 W5 W3 W1 R23 R21 R19 R17 R15 R13 R11 R9 R7 R5 R3 R1		
<u>24 Write Bus Lines</u>					
		W1 = least significant bit			
		W24 = most significant bit			
<u>24 Read Bus Lines</u>					
		R1 = least significant bit			
		R24 = most significant bit			
Power Bus-lines	{ -12V d.c. +200V d.c. 117V a.c. Live Reserved +12V d.c. Reserved OV (Power Return) }	-12 +200 ACL Y1 +12 Y2 0	-24 -6 ACN E +24 +6 0	-24V d.c. -6V d.c. 117V a.c. Neutral Clean Earth +24V d.c. +6V d.c. OV (Power Return)	Power Bus-lines

(VIEWED FROM FRONT OF CRATE)

Pin Allocation at Control Station

(Station 25)

Individual patch contact	P1	B	Busy	Bus-line			
Individual patch contact	P2	F16	Function	Bus-line			
Individual patch contact	P3	F8	Function	Bus-line			
Individual patch contact	P4	F4	Function	Bus-line			
Individual patch contact	P5	F2	Function	Bus-line			
Bus-line	Command Accepted	X	Function	Bus-line			
Bus-line	Inhibit	I	Sub-address	Bus-line			
Bus-line	Clear	C	Sub-address	Bus-line			
Individual patch contact	P6	A2	Sub-address	Bus-line			
Individual patch contact	P7	A1	Sub-address	Bus-line			
Bus-line	Strobe 1	S1	Z	Bus-line			
Bus-line	Strobe 2	S2	Q	Bus-line			
<u>24 Individual Look-at-Me Lines</u> L1 from Station 1, etc.		L24 L23 L22 L21 L20 L19 L18 L17 L16 L15 L14 L13 L12 L11 L10 L9 L8 L7 L6 L5 L4 L3 L2 L1	N24 N23 N22 N21 N20 N19 N18 N17 N16 N15 N14 N13 N12 N11 N10 N9 N8 N7 N6 N5 N4 N3 N2 N1	<u>24 Individual Station Number Lines</u> N1 to Station 1, etc.			
Power Bus-lines	-12V dc. +200V d.c. 117V a.c. Live Reserved +12V d.c. Reserved OV (Power Return)		-12 +200 ACL Y1 +12 Y2 0	-24 -6 ACN E +24 +6 0	-24V d.c. -6V d.c. 117V a.c. Neutral Clean Earth +24V d.c. +6V d.c. OV (Power Return)		Power Bus-lines

(VIEWED FROM FRONT OF CRATE)

Standard Dataway Usage

TITLE	DESIGNATION	CONTACTS	USE AT A MODULE
Command			
Station Number	N	1	Selects the module (Individual line from control station).
Sub-Address	A1, 2, 4, 8	4	Selects a section of the module.
Function	F1, 2, 4, 8, 16	5	Defines the function to be performed in the module.
Timing			
Strobe 1	S1	1	Controls first phase of operation (Dataway signals must not change).
Strobe 2	S2	1	Controls second phase (Dataway signals may change).
Data			
Write	W1 – W24	24	Bring information to the module.
Read	R1 – R24	24	Take information from the module.
Status			
Look-at-Me	L	1	Indicates request for service (Individual line to control station).
Busy	B	1	Indicates that a Dataway operation is in progress.
Response	Q	1	Indicates status of feature selected by command.
Command Accepted	X	1	Indicates that module is able to perform action required by the command.
Common Controls			
Initialize	Z	1	<i>Operate on all stations connected to them, no command required.</i> Sets module to a defined state. (Accompanied by S2 and B).
Inhibit	I	1	Disables features for duration of signal.
Clear	C	1	Clears registers. (Accompanied by S2 and B).
Non-Standard Connections			
Free bus-lines	P1, P2	2	For unspecified uses.
Patch contacts	P3 – P5	3	For unspecified interconnections. No Dataway Lines.
Mandatory Power Lines			<i>The crate is wired for mandatory and additional lines.</i>
+24V d.c.	+24	1	
+6V d.c.	+6	1	
-6V d.c.	-6	1	
-24V d.c.	-24	1	
OV	0	2	Power return.
Additional Power Lines			<i>Lines are reserved for the following power supplies.</i>
+200V d.c.	+200	1	Low current for indicators etc.
+12V d.c.	+12	1	
-12V d.c.	-12	1	
117V a.c. (Live)	ACL	1	
117V a.c. (Neutral)	ACN	1	
Clean Earth	E	1	Reference for circuits requiring clean earth.
Reserved	Y1, Y2	2	Reserved for future allocation.
TOTAL		86	

Appendix B

FASTBUS STANDARD

FASTBUS is a new data acquisition system standard developed by the U.S. NIM Committee in collaboration with the European ESONE Committee and is being published by the Department of Energy. FASTBUS meets the requirements of the next generation of physics experiments by incorporating several powerful features including:

- Modularity
- 32-bit address and data fields
- High-speed operations with block transfers capable of 32-bit word, up to 100 MBytes per second
- Multiple and parallel processor bus with multiple bus segments which operate independently but link together for passing data
- Asynchronous operations to accommodate variable speed devices using handshaking for reliability
- Synchronous non-handshake operations for transferring data at maximum speed
- Broadcast operations for initializing, clearing, etc., banks of modules throughout the system in one operation
- A structure to easily accommodate fast, simple scanning of sparse data from large detector arrays.

The Standard allows for practical implementation of diverse types of modules. Basic requirements are established for a device to be a FASTBUS module, guaranteeing compatibility with all other FASTBUS modules. In addition, many additional operating modes and features are well-defined. This organization allows a module designer to choose the most practical features for the application with minimum amount of electronics. Data acquisition modules and data communications modules, for example, can operate efficiently and fluently in the same FASTBUS

segment even though their FASTBUS interfaces are very different. To take further advantage of this versatile standard, the pc board size is approximately four times of a CAMAC board. Power supply and cooling capabilities have been increased substantially. These factors permit a significant increase in packaging density; 96 (or more) channel modules are possible. This will significantly lower the "per channel cost" of data acquisition systems.

Auxiliary circuit board mounting is accommodated at the rear of the backplane. Connector pins are installed in the backplane and allow for a direct connection between a module in a normal slot and an auxiliary board behind the backplane. Each FASTBUS slot may be associated with an auxiliary circuit board. Although the mechanics of the auxiliary circuit cards are well defined, the electrical characteristics of the auxiliary circuit connections have no restrictions whatsoever and there is no busing of connections between contacts in the auxiliary connector area. Use of the

auxiliary slot will include such things as trigger logic, analog signal, outputs, custom I/O, etc.

During the development of FASTBUS special emphasis was placed on standard software for system initialization and diagnostics and subroutine calls for data taking. Every effort was made to provide hardware "hooks" to software diagnose system failures, thus helping to minimize experiment down-time.

Architecture

The following figure illustrates a typical system architecture for a large detector data acquisition system implemented with FASTBUS:

The ANC, ATC, and GAC modules are ANCillary logic modules which are required at the ends of every crate segment and are mounted on the backside of the bus. These modules provide for such functions as bus terminations, arbitration logic, geographical addressing logic, bus arbitration inhibiting and broadcast message system handshake logic.

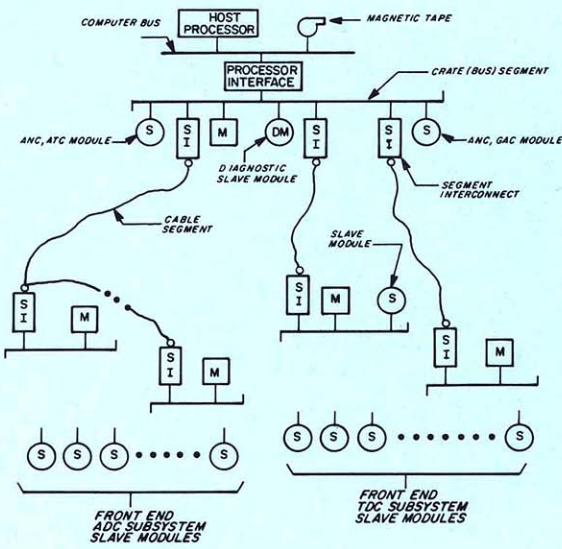


Figure 1

Crate and Cable Segment Signal and Power Lines

Group	Symbol Name	Number	Description	Driven by
1	AS	Address Sync	1 Valid Address Strobe (Address Recognized Strobe)	M S
1	EG	Enable Geographic	1 Geographical Address Specifier Delayed Geographical Address Specifier	M ANC (GAC)
1	GA*	Geographical Address	5 Encoded Geographical Address Device Slot Position	ANC (GAC)
1, 2	MS	Mode Select	3 Operation Type Specifier	M
1, 2	RD	Read	1 Read/Write Cycle Specifier	M
1, 2	AD	Address/Data	32 Multiplexed Address and Data	M, S
1, 2	PA	Parity	1 Odd Parity on AD Signals	M, S
1, 2	PE	Parity Enable	1 Odd Parity Being Generated Signal	M, S
1, 2	SS	Slave Status	3 Status of Attempted Cycle	S
1, 2	WT	Wait	1 Temporarily Delays Response for Diagnostics	S
1, 2	.DS	Data Sync	1 Valid Data or Data Request Signal	M
1, 2	DK	Data Acknowledge	1 Data Accepted or Valid Data Strobe System Broadcast Data Received Strobe	S ANC (ATC)
1, 2	TP*	T Pin	1 Broadcast Operation Device Select Line Broadcast Operation Data Return Line	M S
3	AR	Arbitration Request	1 Request for Bus Mastership	M
3	AG	Arbitration Grant	1 Arbitration in Progress/Granted Signal	ANC (ATC)
3	AL	Arbitration Level	6 Device Priority Level	M
3	AI	Arbitration Inhibit Request	1 New Arbitration Request Signal	ANC (ATC)
3	GK	Grant Acknowledge	1 Bus Mastership Signal	M
4	SR	Service Request	1 Asynchronous Interrupt Line	M, S
4	RB	Reset Bus	1 Bus Initialization Line	M, SI
4	BH	Bus Halted	1 Bus Activity Inhibited Line	ANC (ATC)
4	DA*	Daisy Chain A	3 User Daisy Chain Lines	M, S
4	DB*	Daisy Chain B	3 User Daisy Chain Lines	M, S
4	TX*	Serial Line Transmit	1 System Diagnostic Line	M, S
4	RX*	Serial Line Receive	1 System Diagnostic Line	M, S
5	TR*	Terminated Restricted	8 (Digital) Terminated Restricted Use Lines	M, S
5	UR*	Unterminated Restricted	2 (Analog) Unterminated Restricted Use Lines	M, S
6	R*	Reserved	9 Reserved Lines	
7	+ 5.0 V	+ 5.0* Volt Bus	6	
7	- 5.2 V	- 5.2 Volt Bus	7	
7	- 2.0 V	- 2.0 Volt Bus	3	
7	0 V	Power Return	16	
7	+ 15V	+ 15 Volt Bus	1	
7	- 15V	- 15 Volt Bus	1	
7	OVA	Clean Earth	1	
7	+ 28V	+ 28 Volt Bus	2 (Optional)	

130

Group Use

- 1 Address Cycle Lines
- 2 Data Cycle Signals Lines
- 3 Bus Arbitration/Mastership Lines
- 4 Miscellaneous Bus Lines
- 5 User Restricted Use Lines (intended for front end devices)
- 6 Reserved Lines for future system use
- 7 Power Supply and Return Lines

Addressing Modes

FASTBUS provides three primary addressing modes and one secondary or extended addressing mode:

Geographical

- Dependent on the physical position of a device
- Used for device initialization and simple module addressing

Logical

- Independent of the physical position of a device
- Loaded at system initialization time
- Optional addressing mode

Broadcast

- Independent of the physical position of a device
- Non-handshake (by slave) addressing mode
- Intended for synchronization and initialization (*i.e.*, clearing, etc.) of banks of devices in one or several segments in one operation

Secondary

- Extension of any of the primary addressing modes
- Normally used to access a specific CSR register in a device

Geographical Addressing

GA: Encoded Crate Slot Number

SN: Segment Number; pre-loaded into CSR #3 of ANC GAC module



Figure 2

Logical Addressing

IA: Device Internal Address
DA: Device Address

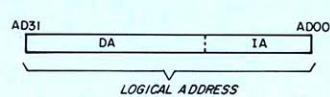


Figure 3

Example:

A 4096 word memory module with each word individually addressable (*i.e.*, RAM) would have a 20-bit DA and a 12-bit IA field.

Broadcast Addressing

GP: Group Field (*i.e.*, partial address used by master to route broadcast operation through SI's

SEL: Routing, device selection and broadcast operation type bits



Figure 4

T PINS: In conjunction with broadcast addressing, the T pins allow selective addressing and scanning of modules. As a third level of multiplexing of the "AD" lines, the T pins could be described as bi-directional LAM lines. Uses include "sparse data scan" which allows modules with data to identify themselves, and

"Pattern Select" which addresses only selected modules to respond to ensuing FASTBUS cycles.

Secondary Addressing

FASTBUS addressing is divided into control and data space as determined by the MS lines at address cycle time. For example, control (CSR) space registers are accessed only through secondary addressing.



Figure 5

Interpretation of Mode Select (MS) and Slave Status (SS) Lines

Mode Select (MS)

The Mode Select (MS) signals accompany AD information at AS₁ and DS₁ time to further identify the address or data cycle being performed as given below:

Mode Select

Address Cycle MS <02:00>	Data Cycle MS <02:00>	Function
000	000 001 010 011 1XX	Data space operation to one slave Single word transfer Block transfer with handshake Secondary address cycle Block transfer without handshake Reserved
001	000 001 010 011 1XX	Control space operation to one slave Single word transfer Block transfer with handshake Secondary address cycle Block transfer without handshake Reserved
010	000 001 010 011 1XX	Broadcast, data space operation to multiple slaves Single word transfer, system (<i>i.e.</i> , ANC) handshake Block transfer with system handshake Secondary address cycle, system handshake Block transfer without system handshake Reserved
011	000 001 010 011 1XX	Broadcast, control space operation to multiple slaves Single word transfer, system handshake Block transfer with system handshake Secondary address cycle, system handshake Block transfer without system handshake Reserved
10X		Reserved for operations to one slave
11X		Reserved for operations to multiple slaves

Slave Status (SS)

The Slave Status (SS) signals are returned to the master by a slave at AK1 or DK1 time or SI at AK1 time to indicate the status of the attempted address or data cycle as given below:

Slave Status

Address Cycle

SS<02:00> Function

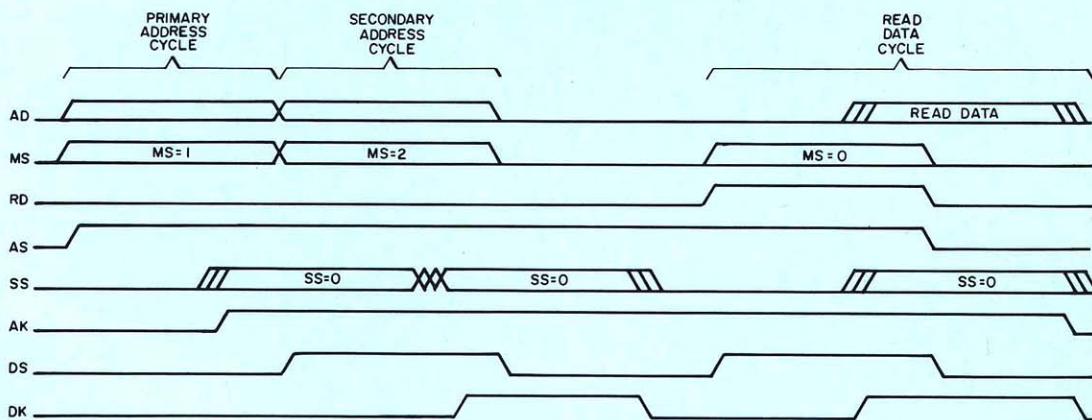
000	Address recognized
001	Network Busy; returned by SI when downstream SI is blocked by other traffic
010	Network Failure; returned by SI when downstream SI does not respond
011	Network Abort; returned by SI when higher priority downstream device requests the bus before the SI has made a connection
10X	Reserved
110	Slave was sent an invalid Internal Address (IA); data rejected
111	Slave was sent an invalid IA; data accepted

Data Cycle

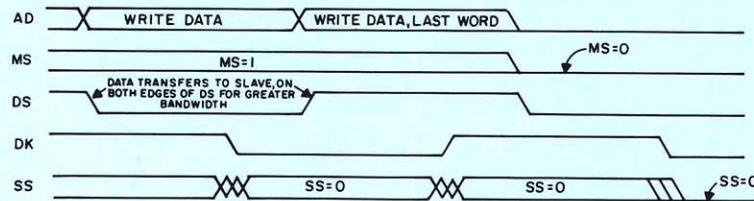
SS<02:00> Function

000	Successful cycle
001	Slave is Busy; try again later, data is neither accepted nor asserted by slave
010	End of Block; block transfer termination by slave; no data transferred on this cycle
011	Reserved
100	Reserved
101	User Defined
110	Error; data is neither accepted nor asserted by slave
111	Error; data is accepted or asserted by slave

TIMING EXAMPLES OF BASIC FASTBUS OPERATIONS.



TIMING DIAGRAM AS SEEN AT MASTER FOR A SINGLE CYCLE, CSR SPACE READ OPERATION USING SECONDARY ADDRESSING.



PARTIAL TIMING DIAGRAM AS SEEN AT MASTER FOR A HANDSHAKE WRITE BLOCK TRANSFER OPERATION TERMINATED BY THE MASTER

FASTBUS Module Connector Pin-Outs

No.	Mne-monic	Function	No.	Mne-monic	Funtion
B01	0 V	Power return	A01	0 V	Power return
B02	+ 28 V	+ 28 volt bus	A02	AL00	Arbitration Level 0
B03	+ 28 V	+ 28 volt bus	A03	AL01	Arbitration Level 1
B04	+ 15 V	+ 15 volt bus	A04	AL02	Arbitration Level 2
B05	- 15 V	- 15 volt bus	A05	0 V	Power return
B06	Ova	Clean Earth	A06	AL03	Arbitration Level 3
B07	- 5.2 V	- 5.2 volt bus	A07	AL04	Arbitration Level 4
B08	- 5.2 V	- 5.2 volt bus	A08	AL05	Arbitration Level 5
B09	- 5.2 V	- 5.2 volt bus	A09	AR	Arbitration Request
B10	AG	Arbitration Grant	A10	0 V	Power return
B11	AI	Arbitration Inhibit	A11	GK	Grant Acknowledge
B12	SS0	Slave Status 0	A12	DK	Data Acknowledge
B13	- 2.0 V	- 2.0 volt bus	A13	AK	Address Acknowled
B14	+ 5.0 V	+ 5.0 volt bus	A14	WT	Wait
B15	+ 5.0 V	+ 5.0 volt bus	A15	0 V	Power return
B16	SS1	Slave Status 1	A16	AS	Address Sync
B17	SS2	Slave Status 2	A17	DS	Data Sync
B18	RD	Read	A18	MS0	Mode Select 0
B19	MS2	Mode Select 2	A19	MS1	Mode Select 1
B20	B20R	Reserved	A20	0 V	Power return
B21	EG	Enable Geog. Address	A21	AD00	Address/Data, LSB
B22	+ 5.0 V	+ 5.0 volt bus	A22	AD01	Address/Data
B23	SR	Service Request	A23	AD02	Address/Data
B24	RB	Reset Bus	A24	AD03	Address/Data
B25	BH	Bus Halted	A25	0 V	Power return
B26	R51	Reserved	A26	AD04	Address/Data
B27	GA00	Geog. Address 0	A27	AD05	Address/Data
B28	GA01	Geog. Address 1	A28	AD06	Address/Data
B29	GA02	Geog. Address 3	A29	AD07	Address/Data
B30	GA03	Geog. Address 3	A30	0 V	Power return
B31	GA04	Geog. Address 4	A31	AD08	Address/Data
B32	- 2.0 V	- 2.0 volt bus	A32	AD09	Address/Data
B33	DLA ¹	Daisy Chain Out Left	A33	AD10	Address/Data
B34	DRA ¹	Daisy Chain In Right	A34	AD11	Address/Data
B35	DLB ¹	Daisy Chain In Left	A35	0 V	Power return
B36	DRB ¹	Daisy Chain Out Right	A36	AD12	Address/Data
B37	DAR	Daisy Chain A Return	A37	AD13	Address/Data
B38	DBR	Daisy Chain B Return	A38	AD14	Address/Data
B39	B39R	Reserved	A39	AD15	Address/Data
B40	B40R	Reserved	A40	0 V	Power return
B41	B41R	Reserved	A41	TP	T pin
B42	- 5.2 V	- 5.2 volt bus	A42	A42R	Reserved
B43	B43R	Reserved	A43	PE	Parity Enable
B44	B44R	Reserved	A44	PA	Parity
B45	B45R	Reserved	A45	0 V	Power return
B46	TR0	Terminated Restricted	A46	AD16	Address/Data
B47	TR1	Terminated Restricted	A47	AD17	Address/Data
B48	TR2	Terminated Restricted	A48	AD18	Address/Data
B49	TR3	Terminated Restricted	A49	AD19	Address/Data
B50	TR4	Terminated Restricted	A50	0 V	Power return
B51	TR5	Terminated Restricted	A51	AD20	Address/Data
B52	+ 5.0 V	+ 5.0 volt bus	A52	AD21	Address/Data
B53	TR6	Terminated Restricted	A53	AD22	Address/Data
B54	TR7	Terminated Restricted	A54	AD23	Address/Data
B55	UR0	Unterm. Restricted	A55	0 V	Power return
B56	UR1	Unterm. Restricted	A56	AD24	Address/Data
B57	TX	Transmit Serial	A57	AD25	Address/Data
B58	RX	Receive Serial	A58	AD26	Address/Data
B59	- 5.2 V	- 5.2 volt bus	A59	AD27	Address/Data
B60	- 5.2 V	- 5.2 volt bus	A60	0 V	Power return
B61	- 5.2 V	- 5.2 volt bus	A61	AD28	Address/Data
B62	- 2v	- 2 volt bus	A62	AD29	Address/Data
B63	+ 5.0 V	+ 5.0 volt bus	A63	AD30	Address/Data
B64	+ 5.0 V	+ 5.0 volt bus	A64	AD31	Address/Data, MSB
B65	0 V	Power return	A65	0 V	Power return

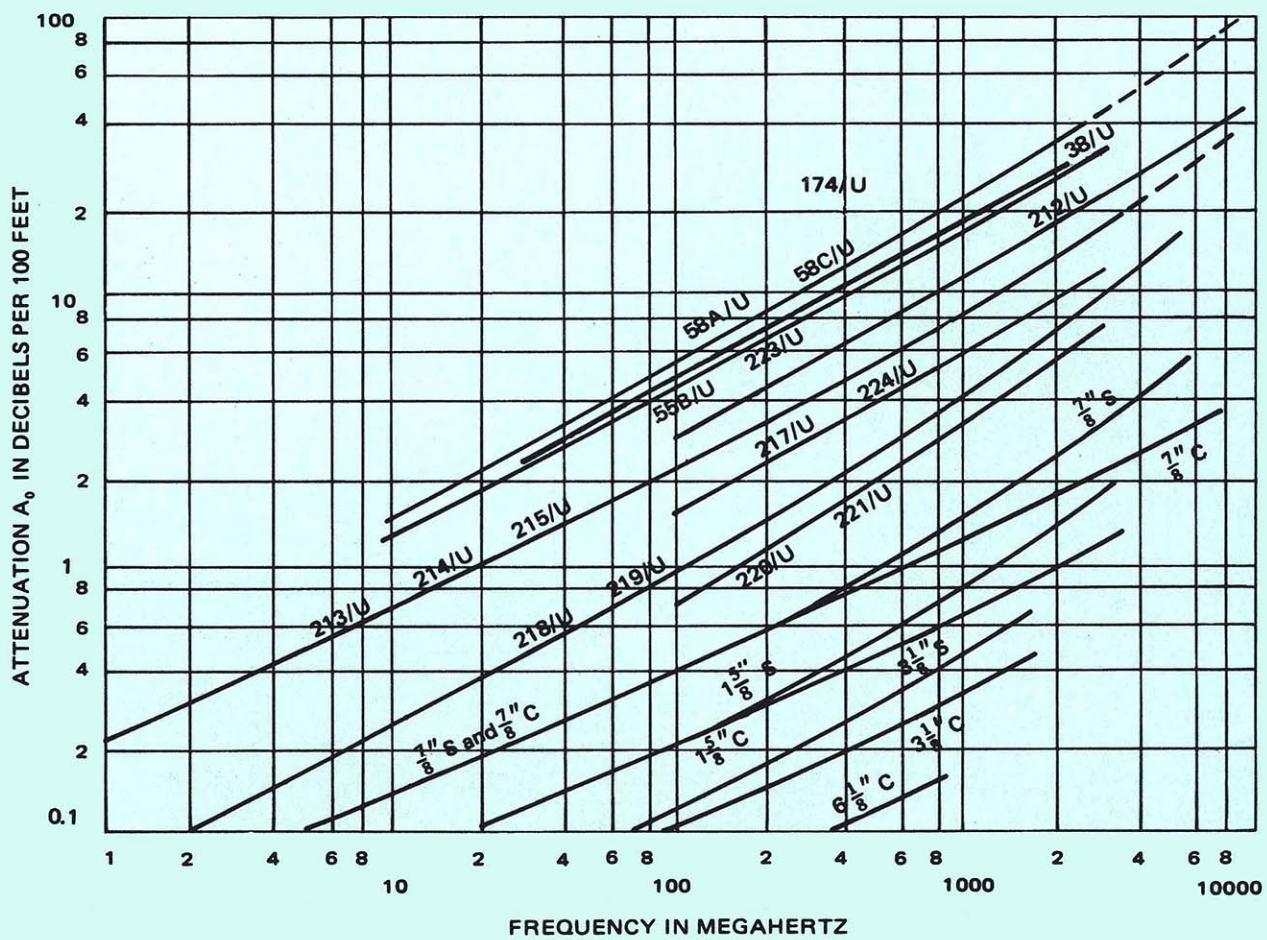
¹Module Circuit Boards shall short DLA to DRA and DLB to DRB if not used.

Arranged in order of contact number as viewed from front of crate.

Based on Oct. 1982 Preprint Standard.

Appendix C

Attenuation of Cables



S = Semi-rigid 50Ω.
C = Rigid copper coax.

Attenuation of Cables

Class of Cables	JAN Type RG-	Inner Conductor	Propagation Delay V/C at 1 MHz	Nominal Diameter of Dielectric (in.)	Nominal Capacitance (pF/ft)	Maximum Operating Voltage (rms)	Remarks
High temp.:							
Single braid	178B/U	7/0.004" silvered copper covered steel	.7071	0.034	29.0	1,000	Z = 50 ohms
	179B/U	Same as above	.7071	0.063	20.0	1,200	
	196A/U	Same as above	.7071	0.034	—	1,000	Miniaturized cable. Z = 50 ohms. Teflon dielectric.
	211A/U	0.190" copper	.7071	0.620	29.0	7,000	Semiflexible cable operating at -55° C to +200° C (formerly RG-117A/U). Z = 50 ohms. 0.450 lb/ft.
	228A/U	0.190" copper	.7071	0.620	29.0	7,000	Same as RG-211A/U, but with armor (formerly RG-118A/U). Z = 50 ohms. 0.600 lb/ft.
	303/U	0.039" silvered copper-covered steel	.7071	0.116	28.5	1,900	Z = 50 ohms
	304/U	0.059" silvered copper-covered steel	.7071	0.185	28.5	3,000	Z = 50 ohms
	316/U	7/0.0067" annealed silvered copper-covered steel	.7071	0.060	—	1,200	Miniaturized cable. Z = 50 ohms.
High temp.:							
Double braid	115/U	7/0.028" silvered copper	.7071	0.250	29.5	5,000	Medium-size cable for use where expansion and contraction are a major problem. Z = 50 ohms
	142B/U	0.039" silvered copper-covered steel	.7071	0.116	28.5	1,900	Small-size flexible cable. Z = 50 ohms
	225/U	7/0.0312" silvered copper	.7071	0.285	29.5	5,000	Semiflexible cable operating at -55° C to +200° C (formerly RG-87A/U). Z = 50 ohms. 0.176 lb/ft.
	227/U	7/0.0312" silvered copper	.7071	0.285	29.5	5,000	Same as RG-225/U, but with armor (formerly RG-116/U). Z = 50 ohms. 0.224 lb/ft.
High attenuation:							
Single braid	301/U	7/0.0203" Karma wire	.7071	0.185	29.0	3,000	High-attenuation cable. Z = 50 ohms
50 ohms:							
Single braid	58/U	1/0.032" copper	0.649	0.121	28.5	1,900	0.024 lb/ft.
	58A/U	19/0.0071" copper	0.649	0.120	29.5	1,900	0.025 lb/ft.
	58C/U	19/0.0071" tinned copper	0.65938	0.116	28.5	1,900	Small-size flexible cable. 0.029 lb/ft.
	213/U	7/0.0296" copper	0.65938	0.285	29.5	5,000	Medium-size flexible cable (formerly RG-8A/U). 0.120 lb/ft.
	215/U	7/0.0296" copper	0.65938	0.285	29.5	5,000	Same as RG-213/U, but with armor (formerly RG-10A/U). 0.160 lb/ft.
	218/U	0.195" copper	0.65938	0.680	29.5	11,000	Large-size low-attenuation high-power transmission line (formerly RG-17A/U). 0.491 lb/ft.
	219/U	0.195" copper	0.65938	0.680	29.5	11,000	Same as RG-218/U, but with armor (formerly RG-18A/U). 0.603 lb/ft.
	220/U	0.260" copper	0.65938	0.910	29.5	14,000	Very-large low-attenuation high-power transmission cable (formerly RG-19A/U). 0.745 lb/ft.
	221/U	0.260" copper	0.65938	0.910	29.5	14,000	Same as RG-220/U, but with armor (formerly RG-20A/U). 0.925 lb/ft.
50 ohms:							
Double braid	55B/U	0.032" silvered copper	0.65938	0.116	28.5	1,900	Small-size flexible cable. 0.032 lb/ft.
	212/U	0.0556" silvered copper	0.65938	0.185	28.5	3,000	Small-size microwave cable (formerly RG-5B/U). 0.093 lb/ft.
	214/U	7/0.0296" silvered copper	0.65938	0.285	30.0	5,000	Special medium-size flexible cable (formerly RG-9B/U). 0.158 lb/ft.
	217/U	0.106" copper	0.65938	0.370	29.5	7,000	Medium-size power transmission line (formerly RG-14A/U). 0.236 lb/ft.
	223/U	0.035" silvered copper	0.65938	0.116	28.5	1,000	Small-size flexible cable (formerly RG-55A/U). 0.036 lb/ft.
	224/U	0.106" copper	0.65938	0.370	29.5	7,000	Same as RG-217/U, but with armor (formerly RG-74A/U). 0.282 lb/ft.
MISC.							
	174/U	7/0.0063" copper covered steel	0.649	0.060	30.0	1,500	Miniature cable. 0.007 lb/ft.
	59/U	1/0.0253" copper covered steel	0.649	0.150	21.0	2,300	High voltage. Z = 73 ohms.
	59B/U	1/0.023" copper covered steel	0.649	0.150	20.5	2,300	High voltage. Z = 75 ohms.
	62/U	1/0.025" copper covered steel	0.833	0.250	13.5	750	Z = 93 ohms.
	62A/U	1/0.025" copper covered steel	0.833	0.249	13.5	750	Z = 93 ohms.

Appendix D

Conventions

POWERS OF 2	DECIBEL EQUIVALENTS	OCTAL	DECIMAL	HEXADECIMAL
$2^0 = 1$	0 dB = 1.0000	100	64	40
$2^1 = 2$	1 dB = 1.1220	1,000	512	200
$2^2 = 4$	2 dB = 1.2589	2,000	1,024	400
$2^3 = 8$	3 dB = 1.4125	3,000	1,536	600
$2^4 = 16$	4 dB = 1.5849	4,000	2,048	800
$2^5 = 32$	5 dB = 1.7783	5,000	2,560	A00
$2^6 = 64$	6 dB = 1.9953	6,000	3,072	C00
$2^7 = 128$	7 dB = 2.2387	7,000	3,584	E00
$2^8 = 256$	8 dB = 2.5119	10,000	4,096	1,000
$2^9 = 512$	9 dB = 2.8184	20,000	8,192	2,000
$2^{10} = 1,024$	10 dB = 3.1623	30,000	12,288	3,000
$2^{11} = 2,048$	11 dB = 3.5481	40,000	16,384	4,000
$2^{12} = 4,096$	12 dB = 3.9811	50,000	20,480	5,000
$2^{13} = 8,192$	13 dB = 4.4668	60,000	24,576	6,000
$2^{14} = 16,384$	14 dB = 5.0119	70,000	28,672	7,000
$2^{15} = 32,768$	15 dB = 5.6234	100,000	32,768	A,000
$2^{16} = 65,536$	16 dB = 6.3096	200,000	65,536	10,000
$2^{17} = 131,072$	17 dB = 7.0795	300,000	98,304	11,000
$2^{18} = 262,144$	18 dB = 7.9433	400,000	131,072	20,000
$2^{19} = 524,288$	19 dB = 8.9125	500,000	163,840	21,000
$2^{20} = 1,048,576$	20 dB = 10.0000	600,000	196,608	30,000
		700,000	229,376	38,000

NAME	SYMBOL	VALUE
${}_1/2MM_{c,12}$	amu	$931.5016 \text{ MeV} = 4.336 \times 10^{-28} \text{ kg}$
Proton Mass	M _p	$938.28 \text{ MeV} - 4.368 \times 10^{-28} \text{ kg}$
Electron Mass	M _e	$0.51100 \text{ MeV} = 9.1095 \times 10^{-31} \text{ kg}$
Planck's Constant	<i>h</i>	$1.0546 \times 10^{-34} \text{ Joule-sec} = 6.5822 \times 10^{-22} \text{ MeV-sec}$
	hc	197.329 MeV-Fermi
Boltzman's Constant k		$1.3807 \times 10^{-23} \text{ Joule} \cdot \text{K}^{-1}$
Electronic Charge e		$1.6022 \times 10^{-19} \text{ Coul}$
Avogadro's Number N		$6.022 \times 10^{23} \text{ mole}^{-1}$
Speed of Light c		$2.9979 \times 10^{10} \text{ cm/sec}$

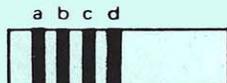
USEFUL CONVERSION FACTORS	PREFIXES
2.2046 lb/kg	Tera 10^{12}
0.2642 gal/l	Giga 10^9
0.03937 mils/ μ	Mega 10^6
57.296°/rad	Kilo 10^3
$3.1558 \times 10^7 \text{ sec/yr} \cong \pi \times 10^7 \text{ sec/yr}$	Milli 10^{-3}
	Micro 10^{-6}
	Nano 10^{-9}
	Pico 10^{-12}
	Femto 10^{-15}
	Atto 10^{-18}

COMMON TAP AND CLEARANCE DRILL SIZES

SCREW	Tap		Clearance	
	NO.	DIA. (inches)	NO.	DIA. (inches)
2-56	50	0.070	42	0.094
4-40	42	0.094	31	0.120
6-32	36	0.107	27	0.144
8-32	29	0.136	18	0.170
10-24	25	0.150	9	0.196
1/4-20	—	17/64	7	0.201

RESISTOR COLOR CODE

0	Black
1	Brown
2	Red
3	Orange
4	Yellow
5	Green
6	Blue
7	Violet
8	Gray
9	White
5%	Gold
10%	Silver
20%	No Band



$$\text{Resistance} = ab \times 10^c \pm d$$

Appendix E

Glossary

ACQUISITION TIME	— In a sample-and-hold or track-and-hold circuit, the time required after the sample or track command for the output to slew through a full scale voltage change and settle to the input voltage to within a specified error band.
ADC	— Analog-to-digital converter.
AND	— Logical designation or circuit function meaning that all inputs must be in the TRUE state for a TRUE output.
ANODE SIGNAL	— The normal negative output signal from the anode of a photomultiplier.
ANTI (COINCIDENCE)	— An input signal which suppresses the normal functioning of the unit for the duration of its application (fast inhibit, slow inhibit, veto, etc.).
APD	— See AVALANCHE PHOTODIODE.
APERTURE JITTER	— In a sample-hold or ADC, the jitter between the time of the sample (or convert) command pulse and the time the input signal is actually sampled. This jitter is usually due to thermal noise. It leads to an uncertainty in the sampled amplitude equal to $\tau \cdot dt/dt$ where τ is the aperture jitter, and dv/dt is the rate of change of the input voltage at the time of sampling. The terms aperture jitter and aperture uncertainty are often used interchangeably.
APERTURE UNCERTAINTY	— In a sample-hold or ADC, the total uncertainty in the time of the sample (or convert) command pulse and the time the input signal is actually sampled, due to all causes including noise, signal amplitude dependent delay variation (as in a flash ADC), temperature, etc. Often used interchangeably with aperture jitter, but aperture uncertainty is the more inclusive term.
AUTOMATIC THRESHOLD CONTROL	— A circuit that automatically adjusts the comparator threshold of a digital receiver to half of the peak amplitude of the input signals.
AVALANCHE PHOTODIODE	— A photodiode with photocurrent gain. Its construction takes advantage of avalanche multiplication of photo-induced hole-electron pairs (photocurrent) when operated with a reverse, near breakdown, bias voltage.
BANDWIDTH	— In normal use, the frequency range over which the gain of an amplifier or other circuit does not vary by more than 3 dB.
BASELINE SHIFT	— See DC LEVEL SHIFT.
BCD	— Binary-coded decimal.
BER	— See BIT ERROR RATE.
BINNING	— A technique for combining points in a histogram to be compatible with the resolution of the display device.
BIT	— An abbreviation of binary digit, one of the two numbers — 0 and 1 — used to encode computer data. A bit is expressed by a high or low electrical voltage.
BIT ERROR RATE	— Ratio of the number of bits of a message incorrectly received to the total number received.
BIT SLICE	— An electronic computer building block usually with from 1 to 16 bits, which is a complete micro-processor. Microprocessors of almost any number of bits may be formed by combining bit slices.
BLANKING	— Setting an output signal to its quiescent level for the duration of the blanking input signal. (Not the same as RESET.)
BRIDGED OUTPUTS	— Parallel output connections which are internally tied common from one signal source.
BURST GUARD	— An operating mode of some discriminators in which a loss of output is prevented during receipt of a high rate input burst of pulses (exceeding the DPR of the unit) by holding the output true for the duration of the burst.
BURST MODE	— A repeatable operation which carries out a preprogrammed sequence of steps upon receipt of a trigger pulse (e.g., a train of clock pulses at a programmed frequency and duration.)
BYTE	— A group of eight bits used to encode a single letter, number or symbol.

CAMAC	— Standardized two-way computer interfacing systems, electrically and mechanically conforming to the standards described by IEEE Standards 583 and 596 (original versions in ESONE Reports No. EUR-4100 and No. EUR-4600 or U.S. AEC Report No. TID-26614). Symmetric name to emphasize bi-directional communications ability between the CAMAC system and the computer.
CAMAC COMMANDS	— See Appendix A.
CAMAC FUNCTION CODES	— See Appendix A.
CAMAC HIGHWAY	— See Appendix A.
CASCADING	— Using units in series to augment a desired characteristic (e.g., amplification, number of inputs, etc.).
CCD	— Charge Coupled Device. An integrated circuit which allows the transfer of a variable amount of charge through a series of cells; an analog shift register.
CHANNEL	<ul style="list-style-type: none"> — 1. A path through an arrangement of components (modules and electrical and/or optical cabling) along which signals can be sent (e.g., a data channel, voice channel, etc.). — 2. A path through a single module often containing many identical parallel paths (e.g., a 12-channel amplifier, usually implies a module with 12 identical amplifiers). — 3. A band of amplitudes, frequencies, or time domains, as when a general region of interest is divided into many small slices (also called bins). (For example, a multichannel analyzer is an instrument that accepts a train of signals and sorts them into their appropriate bins or channels.) <p>NOTE: In referring to ADC's, there is often confusion whether definition 2 or 3 applies. A 256 channel ADC may mean 256 independent ADC's in one module or may mean a single ADC with 256 (2^8) amplitude bins or channels (usually referred to as 8-bit ADC).</p>
CHANNEL PARALLELING	— Analogous to paralleling outputs. Two or more channels give exactly the same output as a function of all the inputs to the given channels.
CHANNEL PROFILE	— A measure of intrinsic ADC or TDC noise, normally expressed as the nominal width at a defined height of the probability vs. input distribution of the channel.
CHARGE SENSITIVE	— A device in which the output is directly proportional to the total integrated charge contained in the input pulse. A nominal integrating time must be specified.
CATHODE SIGNAL	— The normally positive signal from the negative pad or wire of a wire chamber.
CLADDING	— In fiberoptic conductors, this refers to low refractive index material that jackets the fiber core and provides optical insulation and protection for the core; also called the coating.
CLADDING MODE	— Refers to the transmission of light through the cladding rather than the core of an optical fiber. This light is rapidly attenuated but can give misleading readings of the power from a source if a short test fiber is used.
CLAMPING	— Holding a circuit point to some reference level (frequently ground) by means of a low-impedance element such as a saturated transistor, FET, forward-biased diode, relay, etc.
COMMON MODE RANGE	— The maximum range (usually voltage) within which differential inputs can operate without a loss of accuracy.
COMMON MODE REJECTION RATIO	— The ratio of the common-mode input voltage to the output voltage expressed in dB. The extent to which a differential amplifier does not provide an output voltage when the same signal is applied to both inputs.
COMMON MODE SIGNAL (NOISE)	— The signal (usually noise) which appears equally, and in phase on each of the differential signal conductors to ground. See DIFFERENTIAL INPUT.
COMPLEMENTARY OUTPUT	— An output giving a signal with its quiescent state and TRUE state reversed from that of the normal output signal. For example, for NIM inputs or outputs, complementary signal refers to one with a quiescent state of -16 mA and with a TRUE state of 0 mA.

COMPLEMENTARY LOGIC	— Using complementary logic pulses to simulate an anti-function. For example, if in a coincidence unit a complementary pulse is in time coincidence with other inputs, it will inhibit the action of the other inputs; in a veto input, a complementary pulse will act as an enable.
CONVERSION CYCLE	— The entire sequence involved in changing data from one form to another, e.g. digitizing an analog quantity, changing binary data to BDC, etc.
CONVERSION GAIN	— The slope of the function relating a converter output to the input, e.g., for a linear charge ADC with no pedestal, the conversion gain is the full-scale counts, divided by the full-scale input, probably in counts/pC. Note that this is the inverse of the sensitivity of the converter, but the terms are occasionally interchanged.
CONVERSION TIME CORE	— The time required for a conversion cycle. — In a fiberoptic conductor, this refers to the central region of the optical fiber. The refractive index of the core must be higher than that of the cladding for proper transmission of light.
CROSSTALK	— Unwanted coupling of a signal from one channel to another.
DAC	— Digital-to-analog converter.
DARK CURRENT	— The current flowing in the absence of irradiation.
DATAWAY	— See Appendix A.
DATALOGGER	— An instrument which accepts input signals (usually slow analog), digitizes them, and stores the results in memory for later readout. The digital equivalent of a strip-chart recorder.
DC	— Direct current. Normally means a voltage or current which remains constant.
DC LEVEL SHIFT	— A change in the nominal DC voltage level present in a circuit.
DC OFFSET	— See DC LEVEL SHIFT. This term may indicate that the shift is intentional, for example, adjustable per control knob.
DC OVERLOAD	— An overload signal of long duration compared to the normal input pulse width or duty ratio of a circuit.
DEADTIMELESS	— See UPDATING.
DIFFERENTIAL INPUT	— A circuit with two inputs that is sensitive to the algebraic difference between the two.
DIFFERENTIAL LINEARITY	— A term often inappropriately used to mean differential non-linearity.
DIFFERENTIAL NON-LINEARITY	— 1. The percentage departure from the average of the slope of the plot of output versus input from the slope of a reference line. 2. The percentage of variation in ADC's or TDC's from the mean of the analog (or time) width of any single digital step. Usually measured by driving the input with a large number of random amplitude pulses and then measuring the relative number of events in each digital bin.
DIFFERENTIAL OUTPUT	— A circuit with two outputs supplying one normal and one complementary level of pulse.
DIFFERENTIAL PULSE PAIR	— A pair of pulses of opposite polarity coincident in time.
DOUBLE-PULSE RESOLUTION	— The minimum input pair spacing at which a discriminator (or logic unit) responds properly to the second pulse of the pair.
DPR	— See DOUBLE-PULSE RESOLUTION.
DUAL PORT MEMORY	— A memory module which has two interfaces through which data can be transferred.
DWELL TIME	— The time in a multichannel scaling unit during which a given bin or channel counts the number of pulses arriving at the unit's signal input.
DYNAMIC RANGE	— The ratio of the largest to the smallest signal which can be accurately processed by a module.
DYNAMIC RAM	— A random access memory in which the internal memory must be refreshed periodically.
DYNODE SIGNAL	— A photomultiplier tube signal taken from the last secondary-emitting electrode. The pulse is positive and about a factor of four smaller than the anode pulse.

ECL	— Emitter-coupled logic, an unsaturated logic performed by emitter-coupled transistors. Normally, ECL LOGICAL 1 = - 1.6 V and LOGICAL 0 = - 0.8 V.
EMI	— Electromagnetic interference caused by current or voltage induced into a signal conductor by an electromagnetic field in the conductor's environment.
FALLTIME	— Unless otherwise defined, the time required for a pulse to go from 90% to 10% of full amplitude. Can also refer generally to the trailing edge of a pulse.
FAN-IN	— The mixing of more than one input signal to obtain one of the following outputs: 1. Linear — a circuit which linearly adds the amplitudes of more than one input signal and creates an output signal equal to the algebraic sum of the inputs; or 2. Logic — a circuit with more than one input which gives a logic output signal whenever a logical signal appears in any input. (Equivalent to a logical OR function.)
FAN-OUT	— The reproduction of an input signal at more than one output.
FEEDTHROUGH	— Unwanted signal which passes a closed gate, or disabled input.
FIFO	— First-in, first-out shift registers (sometimes called first-in, first-out memory).
FLASH ADC	— A very fast analog-to-digital converter in which the analog signal simultaneously is compared to $2^n - 1$ different reference voltages, where n is the ADC resolution. Also called a parallel converter. A very fast analog-to-digital convertor usually consisting of a large set of fast comparators and associated logic.
FWHM	— Full-Width-Half-Maximum; the width at 50% amplitude used to measure the duration of a signal.
GATE	— 1. A circuit element used to provide a logical function (e.g., AND, OR). 2. An input control signal or pulse enabling the passage of other signals.
GROUND LOOP	— A long ground connection along which voltage drops occur due either to heavy circuit current or external pick-up, with the result that circuit elements referred to different points along it operate at different effective ground references.
HARDWARE OPTION	— An option available by soldering an appropriate connecting wire into the circuit.
HISTOGRAM	— A representation of a frequency distribution by means of a rectangle whose widths represent intervals and whose heights represent corresponding frequencies.
HYBRID CIRCUIT	— A small, self-contained high-density circuit element, usually consisting of screened or deposited conductors, insulating areas, resistors, etc., with welded or bonded combinations of bare discrete circuit elements and integrated circuit chips.
IC	— Integrated Circuit. A self-contained multiple element circuit as a monolithic or hybrid.
IMPORTANCE SAMPLING	— Increasing the sample rate during certain periods of recording to obtain denser sampling information. (A technique often used with transient recorders to optimize use of memory areas.)
INHIBIT	— A signal or switch which prevents a unit from operating or responding to inputs; also called veto in fast logic.
INTEGRAL LINEARITY	— A term often used inappropriately to mean integral non-linearity.
INTEGRAL NON-LINEARITY	— Deviation of ADC response from an appropriate straight line fit. The specification is sometimes defined as maximum deviation expressed as a fraction of full scale. More recent ADC's have a specification expressed as a percent of reading plus a constant.
INTERCHANNEL DEAD TIME	— The time required to switch from one circuit path to another. In a multi-channel scaler, the time from the completion of one counting operation for a given channel and the availability to start the next.
INTERLEAVED CLOCKING	— Supplying clock pulses of equal frequency but different phases to different identical circuits or instruments in order to increase the system sample rate. For example, use of two transient recorders with inputs in parallel but complementary clocks to allow operation at twice the maximum rate of single unit.

JITTER	— Short-term fluctuations in the output of a circuit or instrument which are independent of the input.
JUNCTION (C _j)	— An effective capacitor is formed at the P-N junction of a silicon strip detector or silicon photo diode. Its capacitance is termed the junction capacitance. It is the major factor in determining the response speed of the silicon strip detector or photo diode.
LATCH	— To transfer data from an active circuit to a memory register; or, the memory register itself.
LEADING-EDGE INHIBIT	— Only the leading edge of the input must be overlapped by the inhibit pulse to prevent response of the unit.
LED	— Light Emitting Diode.
LIMITER	— A circuit element which limits the amplitude of an input (used for input protection, pulse standardizing, etc.).
LOGICAL 1	— A signal level indicating the TRUE state; corresponds to the unit being set (<i>i.e.</i> if interrogated, the answer is yes).
LOGICAL 0	— A signal level indicating the FALSE state; corresponds to the unit NOT being set (<i>i.e.</i> if interrogated, the answer is no).
LONG-TERM STABILITY	— Refers to stability over a long time, such as several days or months.
MAJORITY LOGIC	— An output is generated when the number of inputs in coincidence is equal to or greater than some specified number. Which inputs are in coincidence is irrelevant.
MAJORITY LOGIC UNIT	— A module which accepts a large number of inputs and reports how many of those inputs had a signal present within a specified time interval.
MASS TERMINATE	— The ability to attach a single multipin connector to multiconductor ribbon cable or coax, usually with a simple few-step process.
MATERIAL DISPERSION	— That part of the total dispersion attributable to the fact that the material in question (glass, in the case of the glass fiber wave guide) has electrical properties which change with frequency.
MCA	— Multichannel Analyzer (for example, pulse height analyzer).
MCS	— Multichannel Scaler.
MONOLITHIC IC	— An integrated circuit whose elements (transistors, diodes, resistors, small capacitors, etc.) are formed <i>in situ</i> upon or within a semiconductor substrate.
MONOSTABLE	— A logic element with a stable and an unstable state. If triggered into the unstable state, it will return after a preset length of time. (Also called a monovibrator or a univibrator.)
MULTIVIBRATOR	
MONOTONIC	— A function with a derivative that does not change sign.
MULTICONVERTER	— A module capable of performing several measurements on the same input signal including time interval measurements, total pulse area measurements, etc.
MULTIPLE PULSING	— More than one serial output from a single input.
MULTIPLICITY LOGIC	— A majority logic unit for a large number of inputs.
MUX	— A device used to selectively switch a number of signal paths to one input or output.
MULTIMODE FIBER	— An optical fiber which will allow more than one mode to propagate.
MWPC	— Multiwire proportional chamber.
NAND	— An AND circuit, except with a complementary (negative true) output.
NIM	— Nuclear Instrumentation Module, conforming to the mechanical and electrical standards outlined in AEC Report No. TID-20893.
NIM BIN AND POWER SUPPLY	— The rack-mountable housing that powers NIM-standard modules, supplying a minimum of 2 A of + 12 V, 1 A of + 24 V, and 5 A of + 6 V. (Higher current is required on + 6 V for full bins of present-day modules.)

NIM LOGIC LEVELS	<ul style="list-style-type: none"> — Often used interchangeably with fast NIM levels, which are defined as follows: For input: LOGICAL 1 = -12 mA to -32, or -700 mV to -1.6 V into 50Ω. LOGICAL 0 = $< +2 \text{ mA}$ or 100 mV, into 50Ω. For outputs: LOGICAL 1 = -14 mA to -32, or -700 mV to -1.6 V into 50Ω. LOGICAL 0 = $< +2 \text{ mA}$ or 100 mV, into 50Ω.
NOISE EQUIVALENT POWER	— NEP (W); the rms value of optical power which is required to produce unity rms signal-to-noise ratio.
NOR	— An OR circuit, except with a complementary (negative true) output.
NRZ	— Nonreturn to zero. A serial data format in which successive bits are not separated by a momentary return to the zero state.
NUMERICAL APERTURE	— NA; the meridinal acceptance angles of a fiber, defined as the square root of $(N^2 - n^2)$ when N and n are, respectively, the refractive index of the core and the cladding. When skew rays are included, the numerical aperture increases.
OFFSET	— The amount by which an analog or digital output or input baseline is shifted with respect to a specific reference value (usually zero).
OR	— A logic circuit having the property that if at least one input is true, the output is true.
PARALLEL CONVERTER	— A technique for analog-to-digital conversion in which the analog signal is simultaneously compared to $2^n - 1$ different reference voltages, where n is the ADC resolution.
PEAK SENSING ADC	— An analog-to-digital converter which digitizes only the peaks of waveforms.
PEDESTAL	— The response of a digitizing circuit (in counts or input units) when gated with no input signal applied. The value normally depends upon the gate width. For change digitizers, the relation is generally linear and corresponds to an input offset current.
PHA	— Pulse Height Analyzer. A device that gives a measure of the amplitude of a signal applied to its input.
PHOTOMULTIPLIER	— An electron tube that contains a photo-cathode, several dynodes, and an output anode. Photons cause electrons to be emitted from the cathode which are amplified by secondary emission from each of the dynodes. The original electron emission is cascaded by the secondary effects. Used to convert low level, high speed light pulses to usable electrical pulses.
PHOTON	— A quantum of electromagnetic energy. The energy of a photon, is $h\nu$, where h is Planck's constant, and ν is frequency.
PISO	— Parallel-In, Serial-Out shift register.
PLANCK'S LAW	— The fundamental law of quantum theory. According to this law, the quantum of energy associated with an electromagnetic field of frequency is $E = h\nu$, where h is Planck's constant ($h = 6.626 \times 10^{-34} \text{ joules/sec}$) and E is the photon energy.
POSITION SENSITIVE DETECTOR	— Any particle detector giving as output information, the position of the detected particle.
POST-TRIGGER SAMPLING	— A design concept frequently used in transient recording in which sampling continues after assertion of a stop trigger for a predetermined interval.
PRETRIGGER SAMPLING	— A design concept used in transient recording in which a predetermined number of samples taken before a stop trigger are preserved.
PROGRAMMABLE LOGIC UNIT	— A module which accepts a number of inputs and generates almost any logic combination of the inputs under pre-loaded or programmed control.
PROM	— Programmable read-only memory. An integrated circuit memory array that is manufactured with a pattern of either all logical zeros or ones and has a specific pattern written into it by the user by a special hardware programmer.
QUASI DIFFERENTIAL INPUT	— An input which accepts single ended signals, yet its isolated ground return offers common mode rejection properties similar to a fully differential input. In general, the common mode rejection is effective only for low frequencies.
RAM	— Random Access Memory. A memory that can be written into or read by locating any data address. That is, a memory which may be written to, or read from, any address at any time.

REAL TIME	— A process that occurs without having to pause for internal conversions and references. Real time processes usually have little or no intrinsic deadtime and are able to proceed at a rate which permits almost simultaneous transitions from inputs to outputs.
REFRACTIVE INDEX	— The ratio of the velocity of light in vacuum to the velocity of light in the specified medium.
RF REFLECTION COEFFICIENT	— Radio Frequency. Normally in the megahertz range.
RESPONSIVITY	— The amount of signal amplitude that is reflected from an input, expressed as a percentage of the original input signal.
RESOLUTION	— The ratio of the rms value of the output current or voltage to the rms value of the incident monochromatic optical power. (Sometimes called sensitivity).
REVERSE TERMINATION	— The minimum measurable increment, as one bit level of an ADC.
RFI	— An output so constructed that pulses reflected back from the rest of the system meet a matching impedance and are absorbed.
RISETIME	— Radio Frequency Interference. A special case of EMI wherein the field causing the induced signal falls into the radio portion of the electromagnetic spectrum.
ROM	— Unless otherwise defined, the time required for a pulse to go from 10% to 90% of full amplitude. Can also refer generally to the leading edge of a pulse.
RUNDOWN	— Read only memory is any type of memory which cannot be readily rewritten. The information is stored on a permanent basis and used repeatedly. Usually randomly accessible.
RZ	— The discharge of a capacitor at a measured rate.
SAMPLE AND HOLD	— Return to zero. See NRZ.
SCA	— A circuit that on command stores on a capacitor the instantaneous amplitude of an input signal.
SCALING	— Single channel analyzer. A circuit which responds only to input signals falling between an upper and lower amplitude level.
SENSITIVITY	— The accumulation of events or clock pulses into a counter. — 1. The minimum signal input capable of causing an output signal with the desired characteristics. — 2. The ratio of the magnitude of the instrument response to the input magnitude (e.g., a voltage ADC has a sensitivity that is probably measured in counts/mV). Note that often sensitivity is referred to the input and is therefore stated as the inverse (e.g., input sensitivity is in units of mV/count in above example).
SENSITIVE AREA	— This parameter affects both the sensitivity and the signal resolution of solid state detectors. A smaller detector gives much better resolution. Selecting the right detector area requires a compromise between the sensitivity and the resolution.
SENSITIVE DEPTH	— In energy spectroscopy where solid state detectors are used, the sensitive depth must be sufficient to completely absorb all the particle energy. If the sensitive depth increases, the signal increases and the capacitance decreases. With the capacitance decrease, there is less preamp noise.
SHIFT REGISTER SCANNER	— A circuit that converts parallel inputs (DC levels) into serial outputs, with a given frequency.
SHOT NOISE	— Noise caused by current fluctuations, due to the discrete nature of charge carriers and random emission of charged particles from an emitter. Many refer to shot noise loosely, when speaking of the mean square shot noise current (amps) rather than a noise power (watts).
SINGLE-MODE FIBER	— A fiber waveguide on which only one mode will propagate.
SIPO	— Serial-In, Parallel-Out shift register.
SKEW RAYS	— A ray which is skew to the fiber axis. If the fiber waves guide is straight, a skew ray traverses a helical path along the fiber, not crossing the fiber axis. A skew ray is not confined to the meridian plan.

SLOW GATE	— Normal terminology for a gate that responds in approximately 20 nsec or more, as opposed to, about 2 nsec. Required slow gate levels in LeCroy circuits are usually TTL signals or a clamp-to-ground from + 5V (e.g. bin gate; Pin W inhibit, etc.).
SNR	— Signal-to-noise ratio is the ratio of the magnitude of the signal to that of the noise.
STAGE DELAY	— The time delay in circuit between input and output, usually measured between the front edges (half maximum) of the respective signals.
STEP INDEX PROFILE	— An optic fiber construction in which the refractive index changes abruptly from the value N1 to N2 at the core-cladding interface (see NUMERICAL APERATURE).
STOP TRIGGER	— A pulse, usually TTL or NIM, which is used to stop a transient recording or similar sequence.
STROBE	— A digital signal used to read or write data or initiate a conversion cycle at a controlled time.
TDC	— Time-to-digital converter.
TERMINATE	— Normally, to provide a matching impedance at the end of coaxial cable to prevent reflections.
THRESHOLD	— The voltage or current level at which a circuit will respond to a signal at its input. Also referred to as trigger level.
TRACK AND HOLD	— A circuit that precedes an analog-to-digital converter which has the ability on command to store instantaneous values of a rapidly varying analog signal. Allows the ADC to accurately digitize within tighter time domains.
TRANSIENT RECORDER	— See Waveform Digitizer.
TRANSRESISTANCE AMPLIFIER	— A type of amplifier which accepts an input current and produces a proportional output voltage.
TTL	— Transistor-transistor logic. Signal levels defined as follows: LOGICAL 0 = 0 to 0.8 V LOGICAL 1 = 2.0 to 5.0 V
TWISTED PAIR	— Cable composed of two isolated wires twisted together. It features high noise immunity because the same amount of noise is induced on both wires. It is suitable for differential pulse pair transmission.
UPDATING	— If an output resulting from one input signal is still present when a second input signal enters at a time greater than the double-pulse resolution of the circuit, an updating circuit will extend the output pulse, such that the pulse length measured from the second input pulse is equal to the preset width.
USEFUL OUTPUT POWER	— The optical power from a laser diode or LED that is available from an output fiber after the removal of most cladding modes.
VETO	See INHIBIT.
WAVEFORM DIGITIZER	— An instrument which samples an input waveform at specified intervals, digitizes the analog values at the sampled points and stores the results in a digital memory. These units can usually be started or stopped at a given time following a trigger pulse so any specific segment of an input waveform or transient may be selected for recording. All units have facilities for reading the digital data out of the memory for processing and some allow display of the waveform on a CRT by recirculating the data to the inputs of a DAC.

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